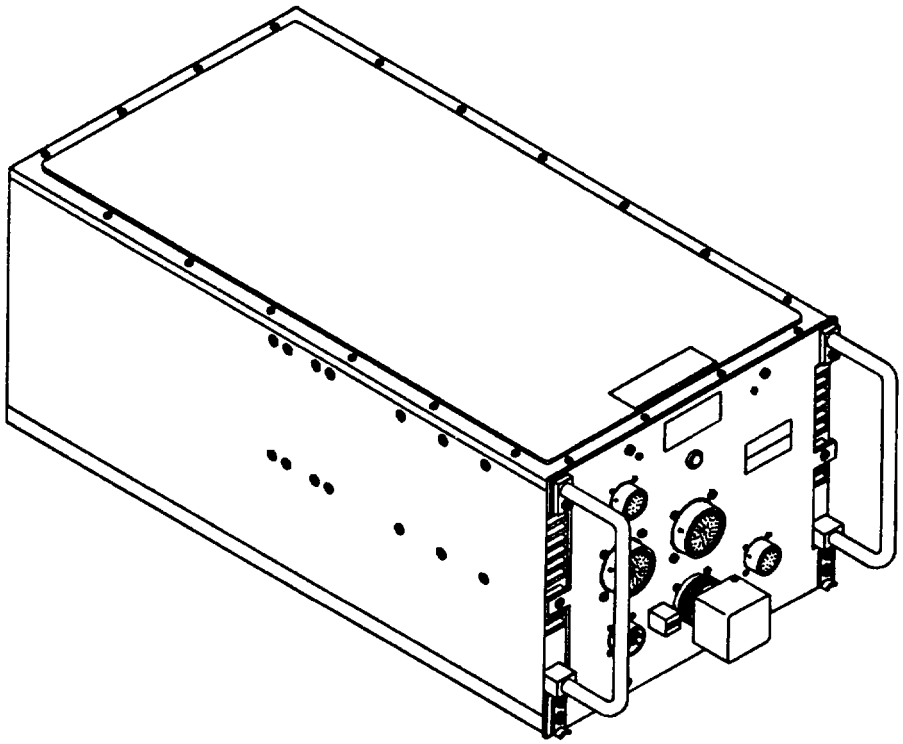
ARMY TM 11-5895-1308-24
NAVY EE610-HD-MMI-010/W11 0-UYK-42(V)4
AIR FORCE TO 31S5-2UYK42-52

UNIT, INTERMEDIATE DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL



COMPUTER, DIGITAL
AN/UYK 42(V)4
(NSN 5895-01-205-6149) (EIC: N/A)

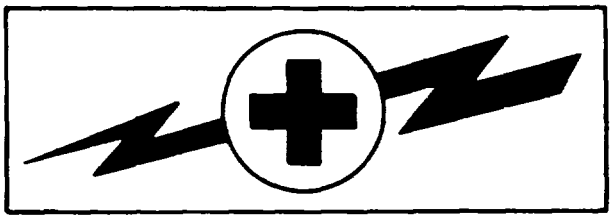
DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

1 NOVEMBER 1994

5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH OR LIFT THE PERSON TO SAFETY USING A DRY WOODEN POLE OR A DRY ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING



HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technicians are aided by operators, they must be warned about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections or 120 volt ac input connections when installing or operating this equipment.

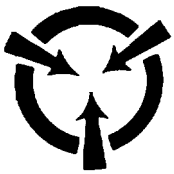
Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through the body.

WARNING

DO NOT BE MISLED BY THE TERM "LOW VOLTAGE". POTENTIALS AS LOW AS 50 VOLTS MAY CAUSE DEATH UNDER ADVERSE CONDITIONS.

For Artificial Respiration, refer to FM 21-11. Air Force personnel refer to AFOSH 127-50 and AFOSH 127-66, Chapter 10.

CAUTION



This equipment contains certain static-sensitive solid state devices which are subject to damage from electrostatic discharge. Effective control of electrostatic discharge is maintained only through continuous strict observance of the following maintenance procedures:

- Any maintenance requiring disassembly of the equipment must be performed at an approved work station. The work station must include a grounded surface and grounded wrist strap in accordance with DOD-HDBK-263.

- All maintenance personnel must have completed training in the handling of static sensitive devices before working on this equipment. Maintenance personnel must wear the grounded wrist strap and be at an approved work station when performing maintenance.

- The static-sensitive subassemblies or circuit cards must be stored in approved electrostatic free material when not installed in the equipment.

NOTE

A faulty or suspected bad CPU unit that has been previously loaded with operational program tapes and cannot be zeroized , is presumed to contain classified data, and therefore must be treated as a sensitive item. Follow local site procedures to store, handle, and transport a classified unit.

D

Technical Manual
No. 11-5895-1308-24
Technical Manual
No. EE160-HD-MMI-010/Wll0-UYK42(V)4
Technical Order
No. 31S5-2UYK42-52

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE

Washington, DC, 1 November 1994

Unit, Intermediate Direct Support And
General Support Maintenance Manual

COMPUTER, DIGITAL AN/UYK42(V)4
(NSN 5895-01-205-6149) (EIC: N/A)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-LM-LT, Fort Monmouth, New Jersey 07703-5007.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, TO 00-5-1. Forward direct to prime ALC/MST.

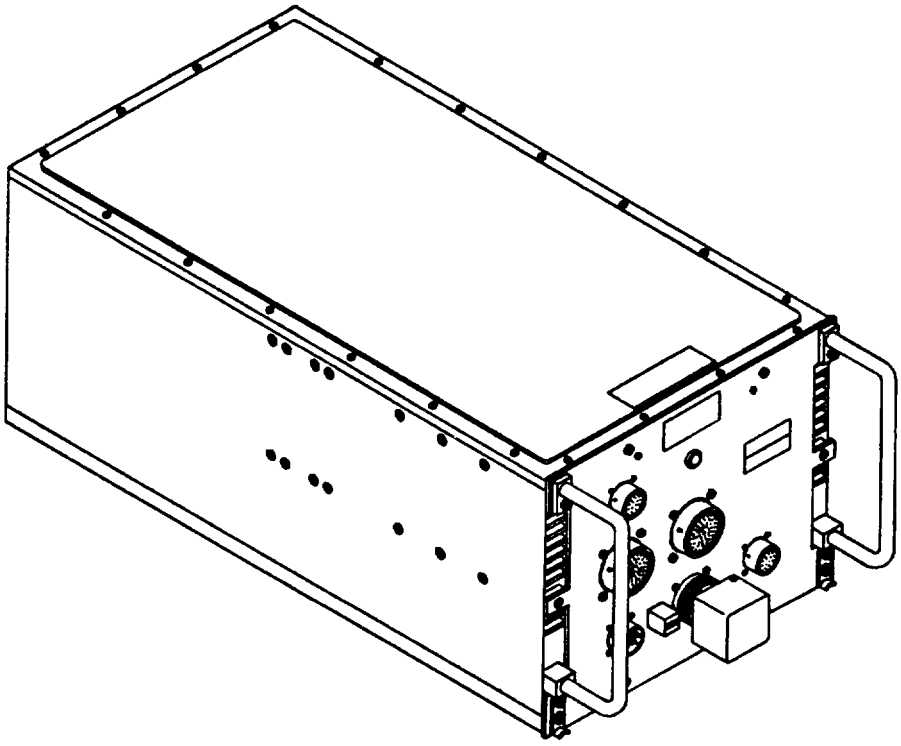
For Navy, mail comments to the Commander, Space and Naval Warfare Systems Command, ATTN: SPAWAR 8122, Washington, DC 20363-5100.

In any case a reply will be furnished direct to you.

Page

HOW TO USE THIS MANUAL

- The front cover index identifies frequently used information. Each item is boxed and identified by topic and page number.
- The first page containing the information you are looking for has a black box on the edge of the page.
- Bend the manual in half and follow the margin index to the page with the black edge marker.
- Topics in the table of contents which are the same as topics on the front cover are also boxed.
- A complete alphabetical subject index is located in the back of the manual. Use the index to locate specific information.
- The glossary contains an explanation of technical terms and acronyms.



COMPUTER, DIGITAL AN/UYK-42(V)4

1-0

CHAPTER 1
INTRODUCTION

Section I. GENERAL INFORMATION

1-1. SCOPE

a. Type of Manual. Unit, Intermediate Direct Support and General Support Maintenance Manual.

b. Equipment Name and Model Number. Computer, Digital AN/UYK-42(V)4 generally referred to as CPU.

c. Purpose of Equipment. The AN/UYK-42(V)4 is a real-time, militarized, digital processor. It controls all automated functions within Regency Net by sending control signals to radios, modems, and Input-Output Units (I/O). Its program is loaded via magnetic tape from the MU-859/U Magnetic Tape Unit.

d. Maintenance Category Cross-Reference. Army maintenance categories are referenced in this manual. Navy and Air Force personnel will contact their same-level maintenance group. Refer to the following cross-reference list.

Army	Navy	Air Force
Unit	Organizational	Organizational

1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update. Air Force personnel will use AFR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol 3 and unsatisfactory material/conditions (UR) IAW OPNAVINST 4790.2, Vol 2, chapter 17.

b. Reporting of Item and Packaging Discrepancies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 73511-2/DLAR 4140.55/SECNAVINST 4355.18/AFR 400-54/MCO 4430.3J.

c. Transportation Discrepancy Report (TDR) (SF 361). Fill out and forward Transportation Discrepancy Report (TDR) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

1-3. CONSOLIDATED INDEX OF PUBLICATIONS AND BLANK FORMS

a. Army. Refer to the latest issue of DA Pam 25-30 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. Navy. Navy personnel refer to NAVSUP 2002.

c. Air Force. For technical publications, Air Force personnel refer to Numerical Index and Requirement Table (NI & RT). For nontechnical publications refer to AFR 0-2. For forms, refer to AFR 0-9.

1-4. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIRs)

a. Army. If your equipment needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design or performance. Put it on an SF 368 (Product Quality Deficiency Report). Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-LC-ED-CFO, Fort Monmouth, New Jersey 07703-5023. We'll send you a reply.

b. Navy. Navy personnel are encouraged to submit EIR's through their local Beneficial Suggestion Program.

c. Air Force. Air Force personnel are encouraged to submit EIR's in accordance with AFR 900-4.

1-5. DESTRUCTION OF ELECTRONICS MATERIEL TO PREVENT ENEMY USE

a. Army. Destroy the Computer in accordance with the procedures in TM 750-244-2 to prevent enemy use.

b. Navy. Navy personnel will comply with the local Command Materiel Destruction Plan.

c. Air Force. Air Force personnel comply with AF REG 56-5 or with the local emergency destruction plan.

1-6. PREPARATION FOR STORAGE OR SHIPMENT

a. Army. Prepare the Computer for storage in accordance with the procedures in TM 740-90-1.

b. Navy. Refer to NAVSUP PUB 503.

c. Air Force. Refer to AFM 66-267 (storage) and AFR 67-31 (shipment).

1-7. OFFICIAL NOMENCLATURE, NAMES AND DESIGNATIONS

COMMON NAME	OFFICIAL NOMENCLATURE
Computer/CPU	Computer, Digital AN/UYK-42(V)4, P/N A3023763
Console I/F	Console I/F Module Circuit Card Assembly A1A13, P/N 109D04302-202
Console I/F*	Console I/F Module Circuit Card Assembly A1A13, P/N 109D04302-201*
Multifunction	Module Assembly I/F AlA12, P/N 109D04670-201
	Multifunction A Circuit Card Assembly A1A12A1, P/N 109D04512-103, or P/N 109D04512-102*
	Multifunction B Circuit Card Assembly A1A12A2, P/N 109D04513-102
Control	Control Module Assembly A1A11, P/N 109D04304-202
	Control A Circuit Card Assembly A1A11A11 P/N 109D04366-203
	Control B Circuit Card Assembly AlAl1A2, P/N 109D04492-105
Control*	Control Module Assembly A1A11, P/N 109D04304-102*
	Control A Circuit Card Assembly A1A1A1, P/N 109D04366-103*, or P/N 109D04366-202*, or P/N 109D04366-102*
	Control B Circuit Card Assembly A1AllA2, P/N 109D04492-204*
Data Path	Data Path Circuit Card Assembly AlA10, P/N 109D04480-401
	Data Path A Circuit Card Assembly AlAlOA1, P/N 109D04482-301
	Data Path B Circuit Card Assembly A1A1OA2, P/N 109D04483-102

* Alternate configuration

1-7. OFFICIAL NOMENCLATURE, NAMES AND DESIGNATIONS (Cont.)

COMMON NAME	OFFICIAL NOMENCLATURE
Data Path*	Data Path Circuit Card Assembly A1A10, P/N 109D04480-301*
	Data Path A Circuit Card Assembly A1A10A1, P/N 109D04482-301*
	Data Path B Circuit Card Assembly A1A10A2, P/N 109D04483-201*
Cache	Cache Circuit Card Assembly AlA9, P/N 109D04520-201
	Cache Circuit Card Assembly A A1A9A1, P/N 109D04522-102
	Cache Circuit Card Assembly B A1A9A2, P/N 109D04523-103, or P/N 109D04523-202*
UNIBUS IF	UNIBUS IF Module A1A8, P/N A3028411
	UNIBUS A Circuit Card Assembly A1A8A1,P/N 109D04370-103, or P/N 109D04370-302*, or P/N 109D04370-401*
	UNIBUS B Circuit Card Assembly A1A8A2, P/N 109D04368-102
SMI	Communications Card Assembly A1A7, P/N A3028350
SMA	SMA Circuit Card Assembly A1A6, P/N A3028351
SMS	SMS Circuit Card Assembly AlA5, P/N A3028352
Memory I/F	Memory I/F Circuit Card Assembly A1A4, P/N 109D04460-103
Memory I/F*	Memory I/F Circuit Card Assembly A1A4, P/N 109D04460-302*
256K Word Memory 1, 2	MOS Memory Circuit Card Assembly A1A3, A1A2, P/N 109D04878-201
MOS Memory Circuit Card Assembly A12A1, A1A3A1	P/N 109D04592-102
MOS Memory Circuit Card Assembly A1A2A2, A1A3A2	P/N 109D04593-305, or P/N 109D04593-404*

* Alternate configuration

1-7. OFFICIAL NOMENCLATURE, NAMES AND DESIGNATIONS (Cont.)

COMMON NAME	OFFICIAL NOMENCLATURE
Power Supply	Power Supply, Module A1AlPS1, P/N A3028415
P/S Backplane	Backplane Assembly A1A1PS1A3, P/N A3086890
P/S Backplane*	Backplane Assembly A1A1PS1A3, P/N A3028418*
Master Module	Master Module A1A1PS1A2, P/N A3028416
Input Module	Input Module A1A1PS1A1, P/N A3028417
Housing	Housing Assembly A1A1, P/N A3086889
Housing*	Housing Assembly A1Al,P/N A3028370*
GMB	Grandmother Circuit Card Assembly A1A1A1, P/N A3086887
GMB*	Grandmother Circuit Card Assembly A1A1A1,P/N A3028354*
Computer/CPU	Central Processing Unit Assembly Al, P/N A3028400
UNIBUS Terminator(UBT)	UNIBUS Terminator A2, P/N 109D00320-203

* Alternate configuration

Section II. EQUIPMENT DESCRIPTION AND DATA

1-8. EQUIPMENT CHARACTERISTICS, CAPABILITIES AND FEATURES

a. Characteristics

The AN/UYK-42(V)4 is a fully militarized, medium range, general purpose computer based on the computer architecture of Digital Equipment Corporation's (DEC) PDP-11/44. It operates with 16-bit data words and provides 22 bits for memory addressing. The computer is housed in a single full ATR chassis using MOS memory and consisting of plug-in modular circuit assemblies. During operation, provision must be made to supply external forced air to the computer for cooling. All power and interface connectors as well as indicators are on the front panel.

The AN/UYK-42(V)4 includes 8K Bytes of parity cache memory, a line frequency clock, an automatic diagnostic/bootstrap loader, a microprocessor-controlled ASC II console interface, two multiplexed serial line ports providing the capability to interface 8 Asynchronous and 4 Synchronous I/O channels, a power-fail/auto restart capability, and a modular power supply. Main memory consists of 1M Bytes(512K word).

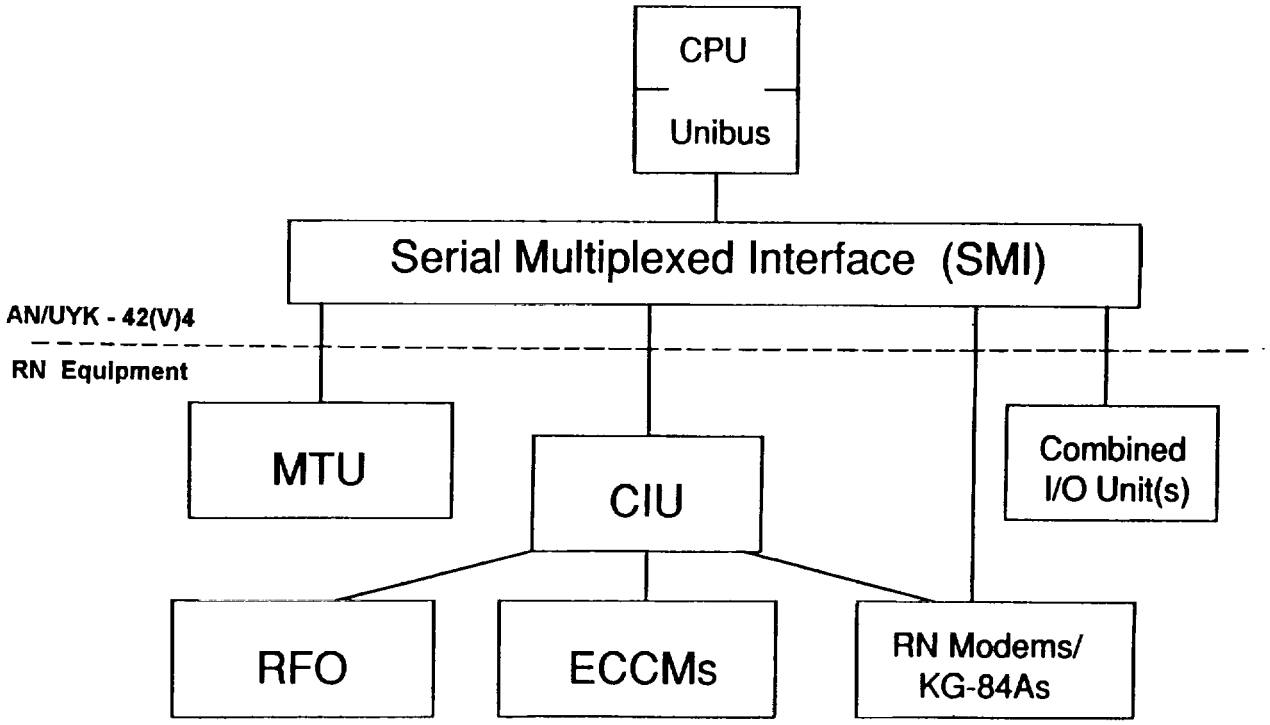
b. Capabilities and Features

- Mid-range Militarized DEC PDP-11/44 Computer.
- Speed - 500 KOPS
- Capable of 1.5M Bytes of NMOS ECC memory. 1.OM Bytes (512K word) standard.
- Two Multiplexed Serial line ports providing a total of:
  - 4 Synchronous I/O Channels
  - 8 Asynchronous I/O Channels
- 8K Byte cache memory
- External power for internal memory provision.
- Memory Management
  - 3 modes of Operation (Kernal, User, Supervision)
  - INST/DATA Space
  - 16, 18, 22 bit addressing
- Asynchronous Bi-directional BUS (UNIBUS)

1-8. EQUIPMENT CHARACTERISTICS, CAPABILITIES AND FEATURES (Cont.)

c. Relationship to Regency Net (RN)

The AN/UYK-42(V)4 is a component of Communications Terminals AN/TRC-179(V)1 and (V)3. It controls all automated functions within the Terminals by sending control data signals to radios, modems, and other HF equipment. It provides for operator message interface through the I/O's. The programs and system parameters are downloaded via magnetic tape cassette from the MU-859/U Magnetic Tape Unit. Data enters or leaves the CPU by any of 12 serial data ports. The data is worked on by the processor program. RN software permits the Terminal to act as a message switch performing network and connectivity management, message security and integrity, as well as Terminal configuration and maintenance. Refer to TM 11-5895-1218-12 for additional system information.

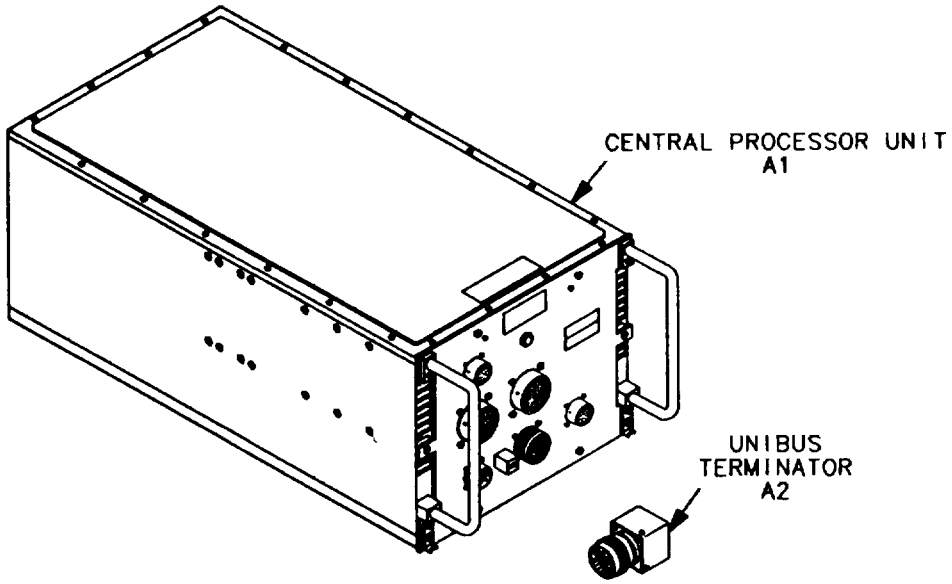


RN-CPU Interface

1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS

1. General. The AN/UYK-42(V)4 is made up of a single chassis and one piece of ancillary equipment:

- Central Processor Unit (CPU) (A1)
-
- UNIBUS Terminator (A2)



2. AN/UYK-42(V)4 Overview
   - Housing Assembly

- Front Panel
  - Connectors J1 through J6 with attached transition harnesses.
  - Elapsed time indicator
  - Power On indicator

- Power Supply
  - Provides regulated DC power to the chassis & modules.
  - Master & Input Modules

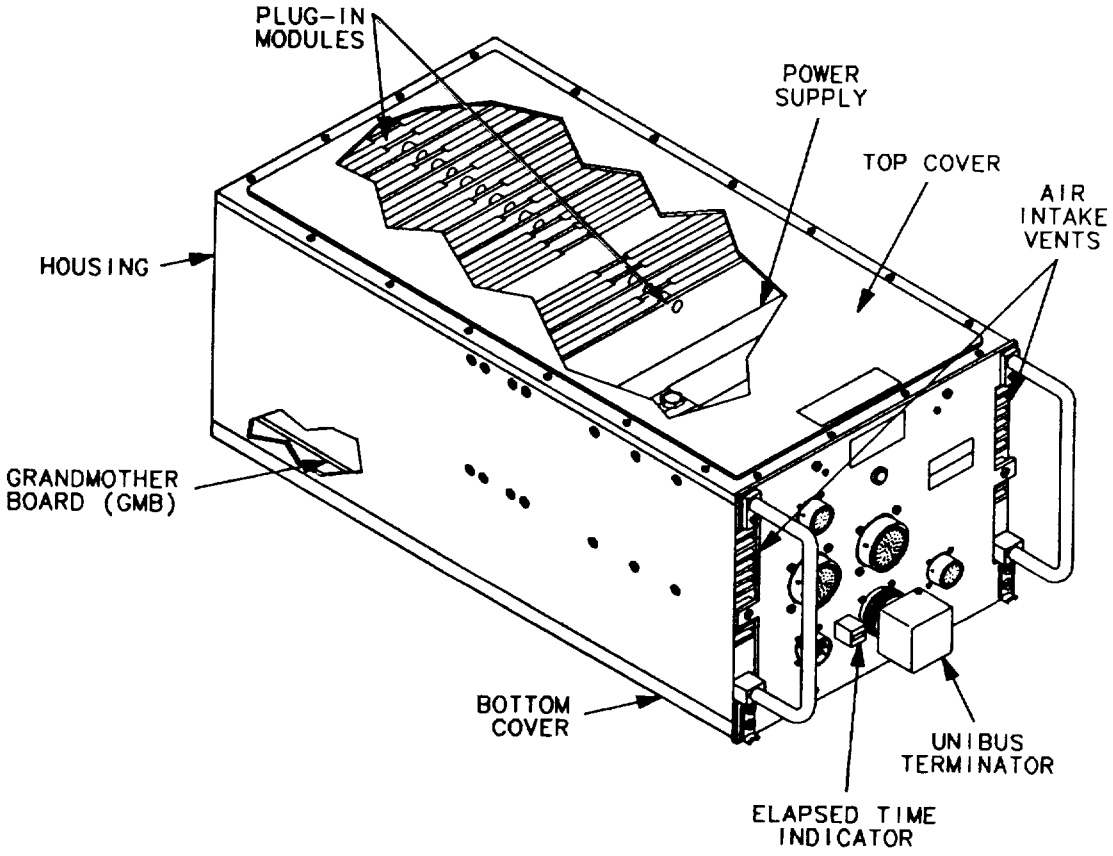
- Grandmother board (GMB)

- Cooling system (Air intake vents)

- Transition Harnesses

1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS (Cont.)

2. AN/UYK-42(V)4 Overview (Cont.)



- Plug-in modules/CCA's (12)
  - Provides the necessary electronics to store, manipulate, & transfer data.

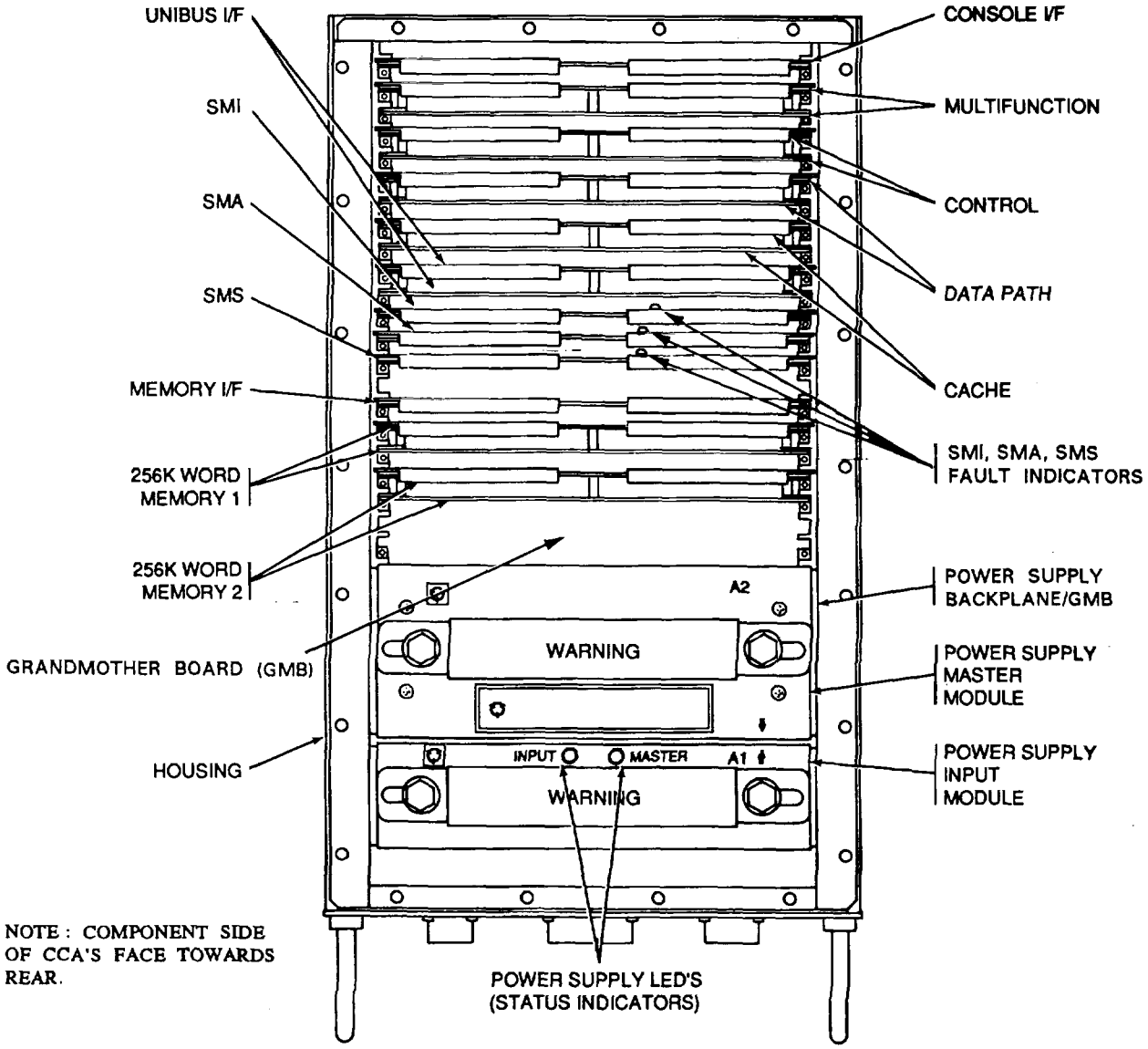
- Top Cover assembly provides:
  - Access to plug-in modules
  - Partial access to transition harnesses
  - Access to power supply

- Bottom Cover assembly provides:
  - Access to Grandmother board (GMB)
  - Access to power supply backplane assembly
  - Partial access to transition harness

- The UNIBUS Terminator is a piece of ancillary equipment that terminates the UNIBUS.

1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS (Cont.)

3. AN/UYK-42(V)4 Description. The AN/UYK-42(V)4 contains circuitry which provides arithmetic and logic functions, instruction decoding, memory management, and data transfer control. It contains 12 plug-in modules identified in the illustration below. These modules slide into card guides located on the wall of the housing, and mount onto the Grandmother Board (GMB) located at the bottom. Seven (7) of the modules are the 2-board type. Five (5) are single board modules. One single-type and one double-type slot are vacant in the current configuration. The power supply consists of two modular subassemblies mounted on a separate GMB/Backplane. The power supply incorporates two LED status indicators, both located on the Input Module of the



COMPUTER TOP VIEW (COVER REMOVED)

1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS (Cont.)

3. AN/UYK-42(V)4 Description (Cont.)

power supply. The SMI, SMA, and SMS modules have LED fault indicators. The following provides a brief description of the major components in the CPU:

a. Housing (A1A1). Provides mechanical support required to house all other assemblies. Cooling ducts are built into the sides.

b. Power Supply (LVPS) (A1AlPS1A1-A3). Power supply consists of three assemblies; the Input Basic Module, the Master Module, and the Backplane Assembly. Provides +5, -12, and +15 volts regulated dc power to the chassis and plug-in modules. Informs the processor in the event of prime power interruption so that the CPU and memories can initiate certain routines to simplify start-up when power is restored.

c. Grandmother Board (GMB) (A1A1A1). Provides connections and internal wiring between modules.

d. Transition Harnesses (AlA1W1-W6). Provides internal wiring between front panel connectors and GMB.

e. Console I/F (A1A13). Links the central processor to console terminal for software development, to a diagnostic unit, or the DEC TU-58 tape drives. Signals between the processor and these units are buffered to provide noise and static immunity and are converted to the proper voltage levels. Also contains voltage monitoring circuitry which can detect over or under voltage conditions of the power supply at the processor backplane.

f. Multifunction (AlA12). Two-board module containing an 8085 microprocessor, two serial line ports, a line clock, and related logic. The microprocessor allows a system terminal to be used as a programmer's console. The 8085 software routines enable the execution of the console commands discussed in Appendix H of TM116625-3268-14&P. The serial line port used for the system terminal also serves as a diagnostic serial port. The second serial line port is available for another serial device such as a tape unit.

g. Control (A1A11). Two-board module containing microcode firmware and associated logic to decode and execute instructions. It also contains the system clock, power-fail/autorestart logic, boot control logic, and trap handling logic.

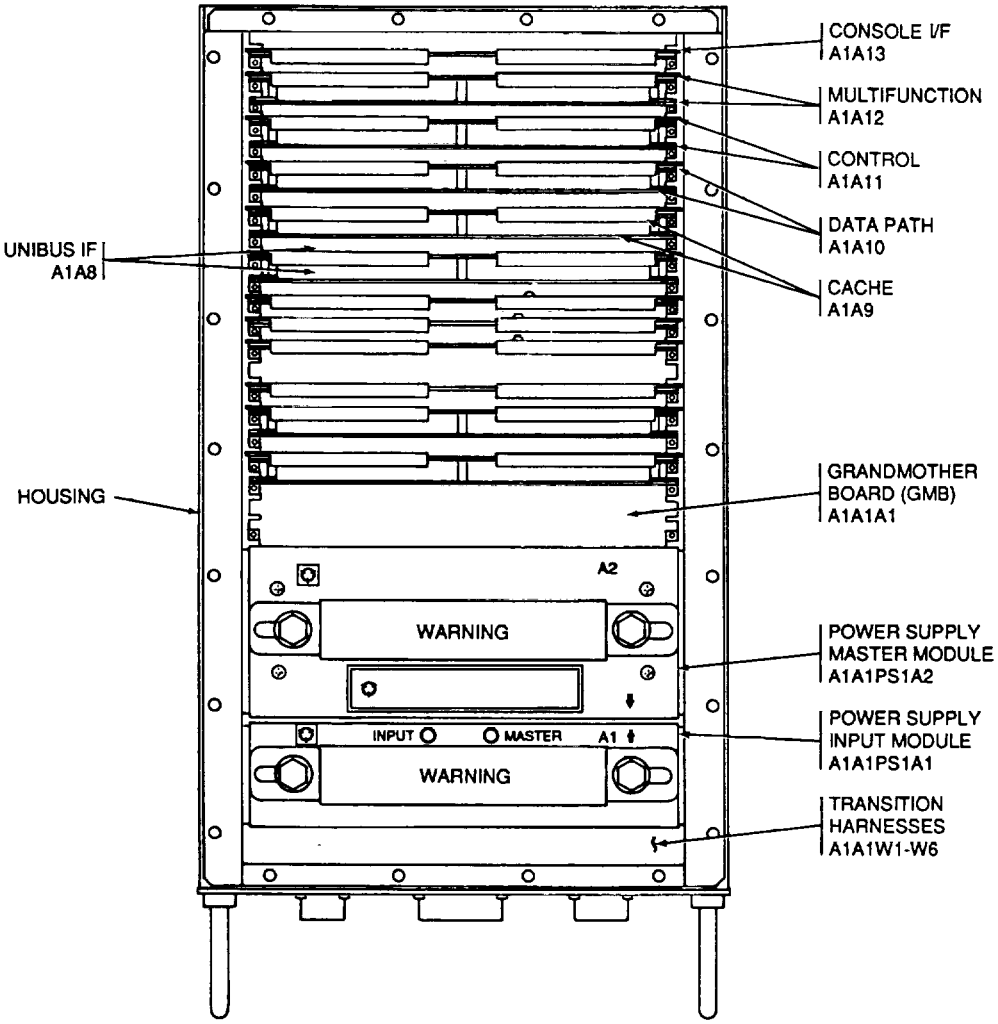
h. Data Path (AlA10) Two-board module containing the data path logic and the memory management logic. The data path performs arithmetic and logic processing, shifting of 8-, 16-, and 32-bit data formats, byte swapping and sign extension of data, storage of general register data, and storage of status information. The memory management section of this module performs address relocation and contains several of the memory management registers.

1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS (Cont.)

3. AN/UYK-42(V)4 Description (Cont.)

i. Cache (A1A9). Two-board module containing 8K-bytes of high-speed RAM which is used to store the most commonly accessed memory locations. The cache increases system performance by decreasing processor to-memory read access time. It is organized as a directly mapped cache with a write-through facility.

j. UNIBUS I/F (A1A8). Two-board module containing the logic which enables the processor to access the UNIBUS. It also includes bus arbitration logic for interrupts and NPRs, the boot circuits which allow booting of up to four devices, and buffers for the PAX data lines to and from the processor. The UNIBUS I/F also controls the operations of the EUB.



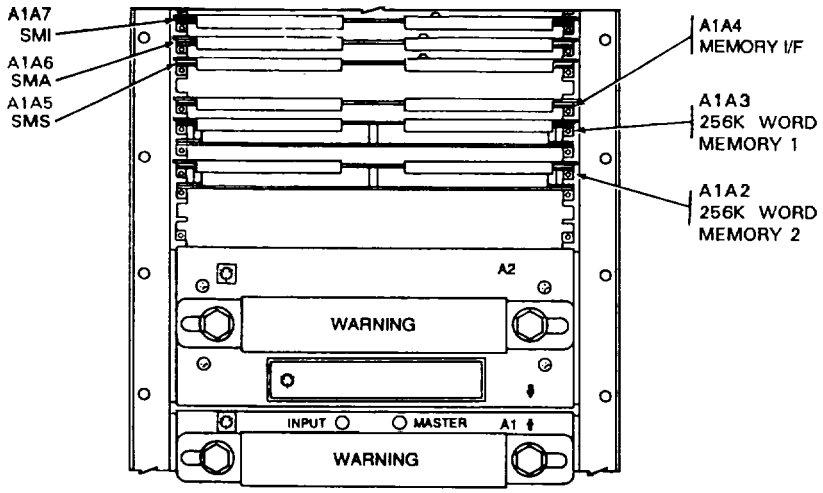
COMPUTER TOP VIEW
(COVER REMOVED)

1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS (Cont.)

3. AN/UYK-42(V)4 Description (Cont.)

k. Memory I/F (A1A4). Links the memory system to the UNIBUS/EUB and central processor. Contains interface, control, and status circuits and provides address interleaving for improved speed of operation.

l. MOS Memory (A1A3-A2). Two 2-board modules, each providing 256K words of MOS memory. Each memory module contains timing and control logic, error correcting code (ECC) logic, and a MOS storage array. The module also contains circuitry for ECC initialization and memory refresh.



COMPUTER TOP VIEW-COVER REMOVED

m. Serial Multiplexed Interface (SMI) (A1A7). Single board module containing an 80186 microprocessor and associated logic that provides interfacing between the SMA, SMS, and the processor via the UNIBUS. The SMI also contains UVEPROM for 80186 microcode firmware storage, scratch pad RAM for transfer of information between the UNIBUS and the SMA and SMS.

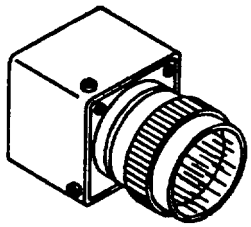
1-9a. LOCATION AND DESCRIPTION OF MAJOR COMPONENTS (Cont.)

3. AN/UYK-42(V)4 Description (Cont.)

n. Serial Multiplexed Asynchronous (SMA) (A1A6). Single board module containing an 80186 microprocessor and associated logic which provides interfacing between up to eight (8) serial asynchronous communition channels. The SMA also contains 8530 type serial communication controllers, UVEPROM for 80186 microcode firmware storage, scratch pad RAM and dual port RAM for the transfer of information between the SMA and the SMI. In Regency Net, the eight channels correspond to the six I/O's, the CPU-CIU link, and the CPU-MTU link. The I/O's operate at 1200 baud, the CIU and MTU at 9600.

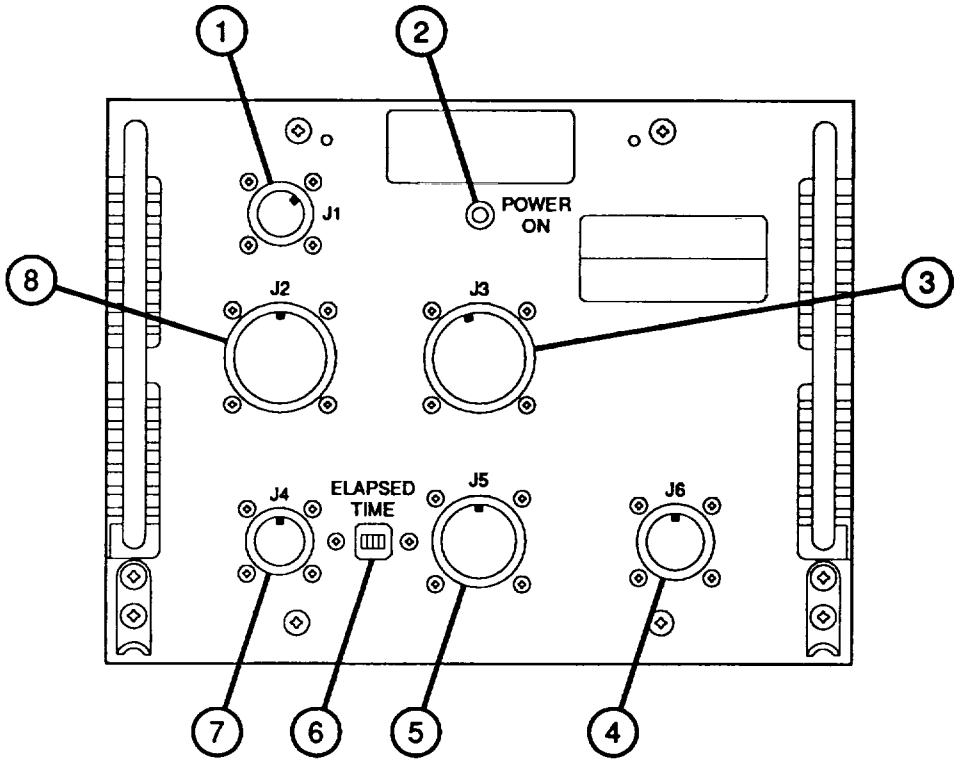
o. Serial Multiplexed Synchronous (SMS) (AlA5). Single board module containing an 80186 microprocessor and associated logic which provides interfacing between up to four (4) serial synchronous communication channels. The SMS also contains 8530 type serial communication controllers, UVEPROM for 80186 microcode firmware storage, scratch pad RAM and dual port RAM for the transfer of information between the SMS and the SMI. In Regency Net, the four channels interface the KG/modem equipment operating at 9600 baud.

p. UNIBUS Terminator (A2). Contains logic and terminating resistors for the UNIBUS lines.



UNIBUS TERMINATOR (A2)

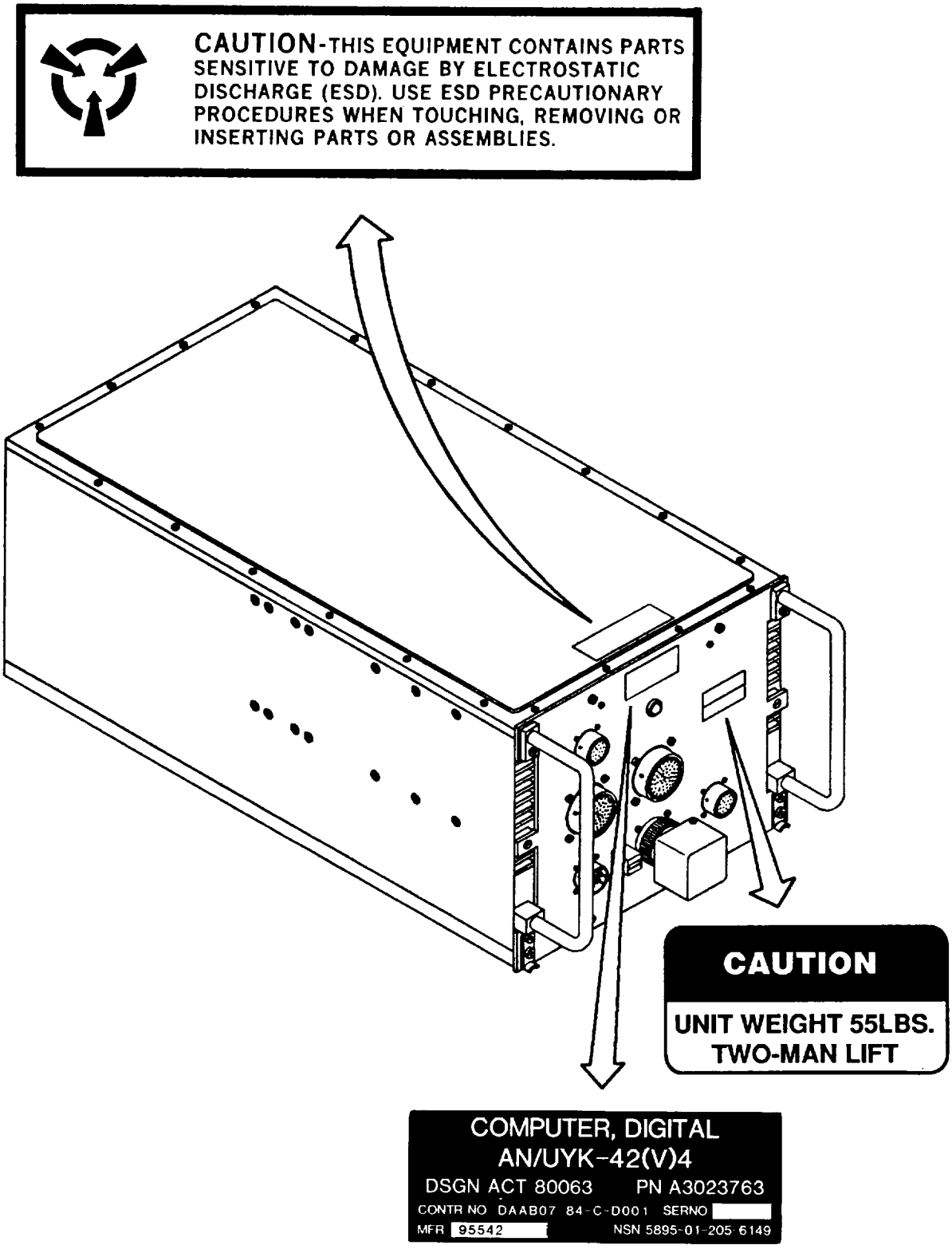
1-9b. FRONT PANEL CONTROL AND INDICATORS



FRONT PANEL

(1) J1 - Console input connection for maintenance purposes only.
(2) POWER ON - Indicator lights green when ac power is applied.
(3) J3 - Synchronous data connector.
(4) J6 - 5.2 Vdc input connection for back-up CPU memory retention.
(5) J5 - UNIBUS Connector - Provides proper bus termination.
(6) ELAPSED TIME Counter - Indicates hours equipment has been used.
(7) J4 - Power-in connector for 115 Vac.
(8) J2 - Asynchronous data connector

1-10. IDENTIFICATION AND INSTRUCTION PLATES



1-11. EQUIPMENT DATA

a. Electrical Specifications:

Voltage (Nominal)	115 Vac, 47-400 Hz, single phase
Current (Nominal)	3 Amperes
Power	(Nominal) 330 Watts
(Maximum)	550 Watts

b. Physical Specifications:

Height (max)	7.89 in (20.04 cm)
Width (max)	10.22 in (25.96 cm)
Length (max overall)	17.45 in (44.32 cm)
Volume	0.81 cu ft (0.023 cu m)
Weight	59 lb (26.76 kg)
Cooling	External Forced Air (Air Flow 75 cu ft/min)
I/O Assembly Slots	12 in use; 1-single & 1-double type available.

c. Environmental Specifications (Operating):

Temperature	-6°F to +131°F (-210C to +550C)
Altitude	15,000 feet (4575 meters)
EMI	Comply with applicable portions of MIL-STD-401A, Notice 3; Test per MIL-STD-462.
Tempest	Comply with applicable requirements of NACSIM 5100A.

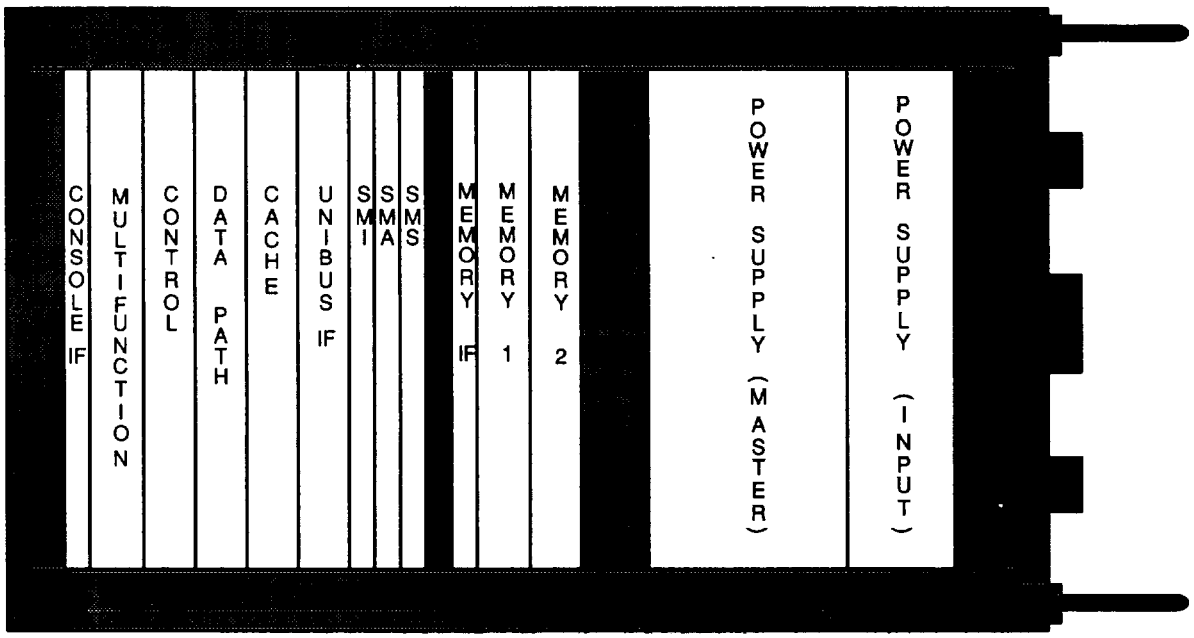
d. Performance Specifications:

Speed (typical)	500 KOPS
Memory Capacity	1 M Bytes/512K word RAM standard; 512K Byte/256K word expansion slot.

1-11. EQUIPMENT DATA (Cont.)

d. Performance Specifications:(Cont.)

Interface	2 serial multiplexed ports providing 12 RS-232C compatable I/O channels. - 8 asynchronous ports. - 4 synchronous ports.
Instruction Timing (TYPICAL)	Memory to Register
Move:	1.19 μsec
Add:	1.01 μsec
Multiply:	6.38 μsec
Divide:	10.76 μsec
Memory Timing (TYPICAL)	
Cycle Time	930 nsec
Read Access	760 nsec
Input/Output	I/O transfer rates up to 1.1 Mwds/sec



AN/UYK-42(4 Chassis Layout (Top View)

1-12. SAFETY, CARE, AND HANDLING

WARNING

To avoid injury to personnel and damage to equipment, two persons are required to carry the Computer.

CAUTION

Prior to removing or installing a component, ensure that power to the component has been turned off. Cables disconnected with voltage present may arc or short. This can produce damage to the connector.

Make all cable connections by hand. Do not use tools. When tools are used to make connections, connectors may be overtightened and damage to the connector and pins may occur.

CAUTION

The Computer contains certain static-sensitive solid state devices which are subject to damage from electrostatic discharge (ESD). Effective control of electrostatic discharge is maintained only through continuous strict observance of the following maintenance procedures:

- **Any maintenance requiring disassembly of the equipment must be performed at an approved work station. The work station must include a grounded surface and grounded wrist strap in accordance with DOD-HDBK-263.**

- **All maintenance personnel must have completed training in the handling of static-sensitive devices before working on this equipment. Maintenance personnel must wear the grounded wrist strap and be at an approved work station when performing maintenance.**

1-12. SAFETY, CARE, AND HANDLING (Cont.)

CAUTION

The static sensitive subassemblies or circuit cards must be stored in approved electrostatic free material when not installed in the equipment.

Section III. PRINCIPLES OF OPERATION

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER

a. General

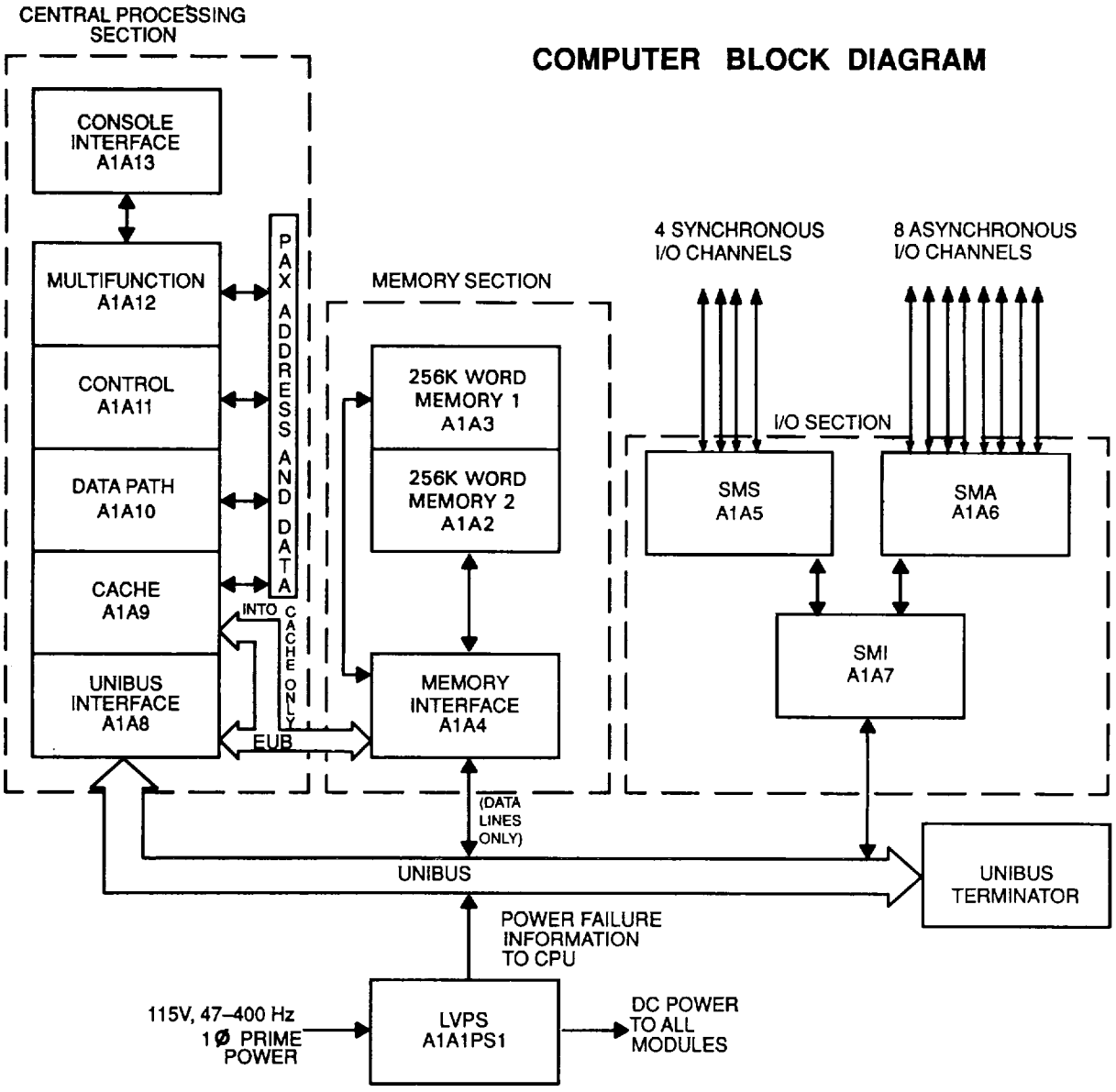
The AN/UYK-42(V)4 is a medium range, general purpose mini-computer which consists of the three functional entities that make up any computer: Central Processor Unit (CPU), Memory, and Input/Output (I/O) section. The computer operates with 16-bit data words and provides 22 bits for memory addressing. The current configuration of the AN/UYK-42(V)4 includes a total of 1.0 megabyte (512K word) of main memory.

The three elements of the computer are all interconnected by a high-speed bus known as the UNIBUS. It allows a variety of information to flow back and forth on the same 56-line bus such as addresses, data, and control signals. A UNIBUS terminator consisting of terminating resistors and logic is placed at the end of the UNIBUS furthest from the processor.

The AN/UYK-42(V)4 central processor uses Schottkly logic. It has 10 general purpose registers which can be used as accumulators, index registers, or as stack pointers. Stacks are extremely useful for nesting programs, creating reentrant coding, and as temporary storage where a Last-In/First-Out structure is desirable. The central processor operates at any of eight levels of priority. The main memory of the AN/UYK-42(V)4 is addressed by a 22-bit Physical Address Extension (PAX) bus which can provide access to over 4 million bytes. In addition, the AN/UYK-42(V)4 processor enables memory to be placed on the UNIBUS. This memory resides in the top 124K words of physical address space. The processor can perform transfers to and from the UNIBUS memory independently of main memory transfers. DMA devices making a reference to an address allocated to UNIBUS memory will never access main memory and, therefore, such transfers are not cached.

The AN/UYK-42(V)4 includes an 8K-Byte high-speed cache memory that buffers words between the processor and main memory. The cache

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)



stores those memory locations that will most likely be accessed by the executing program. The program can be executed quickly by accessing the high-speed cache and must slow down only occasionally for main memory operations.

The internal communication of the AN/UYK-42(V)4 processor is through a 16-bit data bus and a 22-bit PAX bus. Communication between the processor and main memory is through the extended UNIBUS (EUB) and the data lines of the UNIBUS. The UNIBUS provides the path for

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

a. General (Cont.)

transfers between the processor and its associated main memory, the peripherals, or the memory on the UNIBUS. The UNIBUS interface module (UBI) controls the information transfers to and from the PAX bus, the EUB, and the UNIBUS.

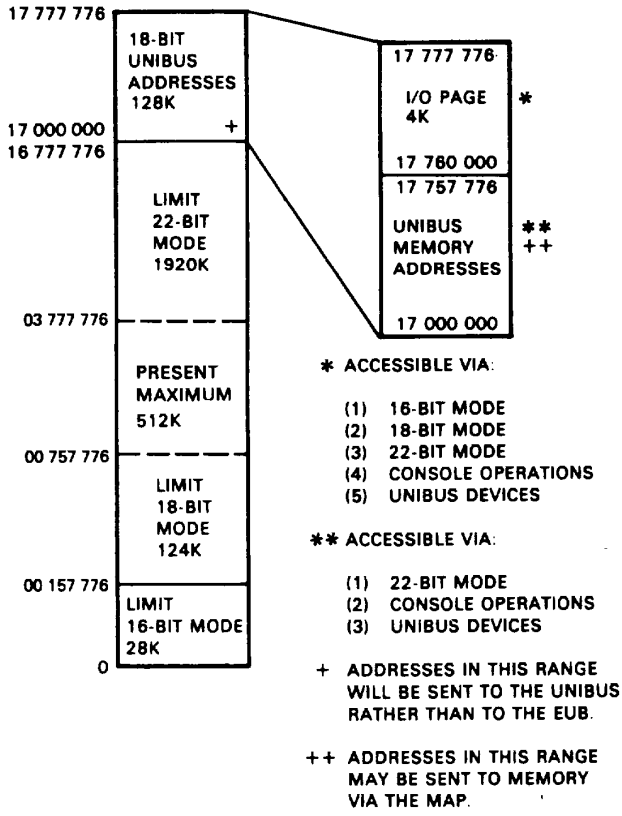
The Multifunction module (MFM) consists of an 8085 micro-processor and the logic necessary to enable the execution of the console command set in the CPU. The 8085 software contains diagnostic programs to test logic and data paths.

The I/O section provides the capability to interface up to 12 I/O channels through two MIL-type circular bulk head connectors. One port provides 8 full-duplex Asynchronous channels whose baud rate is software selectable; the 2nd provides 4 full-duplex Synchronous channels at 9600 baud.

b. AN/UYK-42(V)4 Registers

The upper 4K of the physical address space is assigned to the CPU registers and I/O device registers. The table on the next page lists some of the registers and their associated address.

AN/UYK-42 (V) 4
Physical Address Space



1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

Address	Register
17 777 776	Processor Status Word (PSW)
17 777 772	Program Interrupt Request (PIRQ)
17 777 766	CPU Error
17 777 744, 46, 50, 52, 54	Cache Registers
17 777 707 - 17 777 700	CPU General Registers
17 777 676 - 17 777 660	User Data PAR, Reg. 0-7
17 777 656 - 17 777 640	User Instruction PAR, Reg. 0-7
17 777 636 - 17 777 620	User Data PDR, Reg. 0-7
17 777 616 - 17 777 600	User Instruction PDR, Reg. 0-7
17 777 576	MM Status Register 2 (SR2)
17 777 574	MM Status Register I (SRI)
17 777 572	MM Status Register 0 (SRO)
17 777 566 - 17 777 560	Console Terminal SLU
17 77x xx0 - 17 76x xx0	TU58 DECtape SLUs
17 777 570	Switch Register
17 777 516	MM Status Register 3 (SR3)
17 772 376 - 17 772 360	Kernel Data PAR, Reg. 0-7
17 772 356 - 17 772 340	Kernel Instruction PAR, Reg. 0-7
17 772 336 - 17 772 320	Kernel Data PDR, Reg. 0-7
17 772 316 - 17 772 300	Kernel Instruction PDR, Reg. 0-7
17 772 276 - 17 772 260	Supervisor Data PAR, Reg. 0-7
17 772 256 - 17 772 240	Supervisor Instruction PAR, Reg. 0-7
17 772 236 - 17 772 220	Supervisor Data PDR, Reg. 0-7
17 772 216 - 17 772 200	Supervisor Instruction PDR, Reg. 0-7
17 770 372 - 17 770 200	Map Registers

AN/UYK-42(V)4 Register Addresses

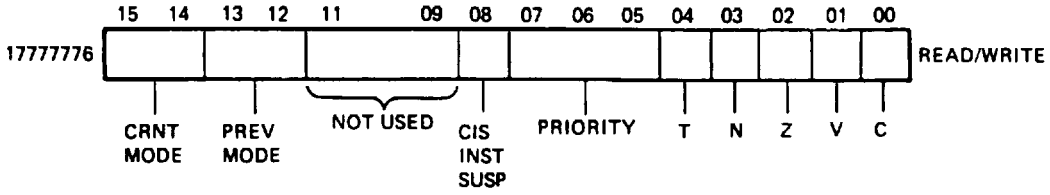
1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

(1) CPU Registers

The CPU contains several registers which can be used to store processor status information, error information and interrupt requests. Ten general purpose registers are also included to be used as accumulators, counters, index registers, or for other programming functions. A brief overview of the CPU registers follows.

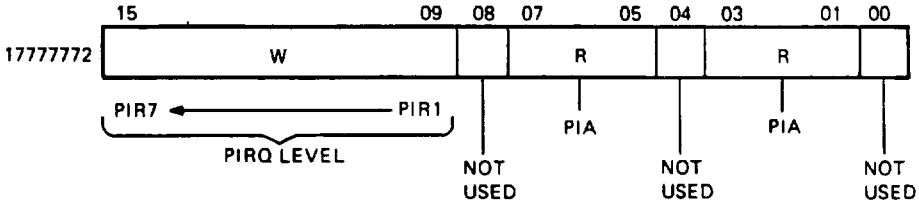
a. Processor Status Word (PSW). The format of the processor status word (PSW) register is shown below.



PSW Register Format

b. Program Interrupt Request (PIRQ) Register. System software may request an interrupt by setting one of bits (PIR) 15:09 for PIR7-PIR1 in the program interrupt request (PIRQ) register. The hardware sets bits 07:05 and 03:01 to the encoded value of the highest PIR bit set. Bits 07:05 allow the program interrupt active (PIA) field to be moved into the processor status word register and set the processor priority to the level of the request honored. This disables all requests on the same level or below. Bits 03:01 can be used as an index constant in branching to an interrupt service routine for the appropriate priority level request.

When a priority interrupt request is granted, the processor traps to location 240. A new PC is taken from location 240 and a new PSW from location 242. The interrupt service routine must queue requests within a priority level and clear the PIR bit before the interrupt is dropped. The figure below shows the bit assignments of the PIRQ.



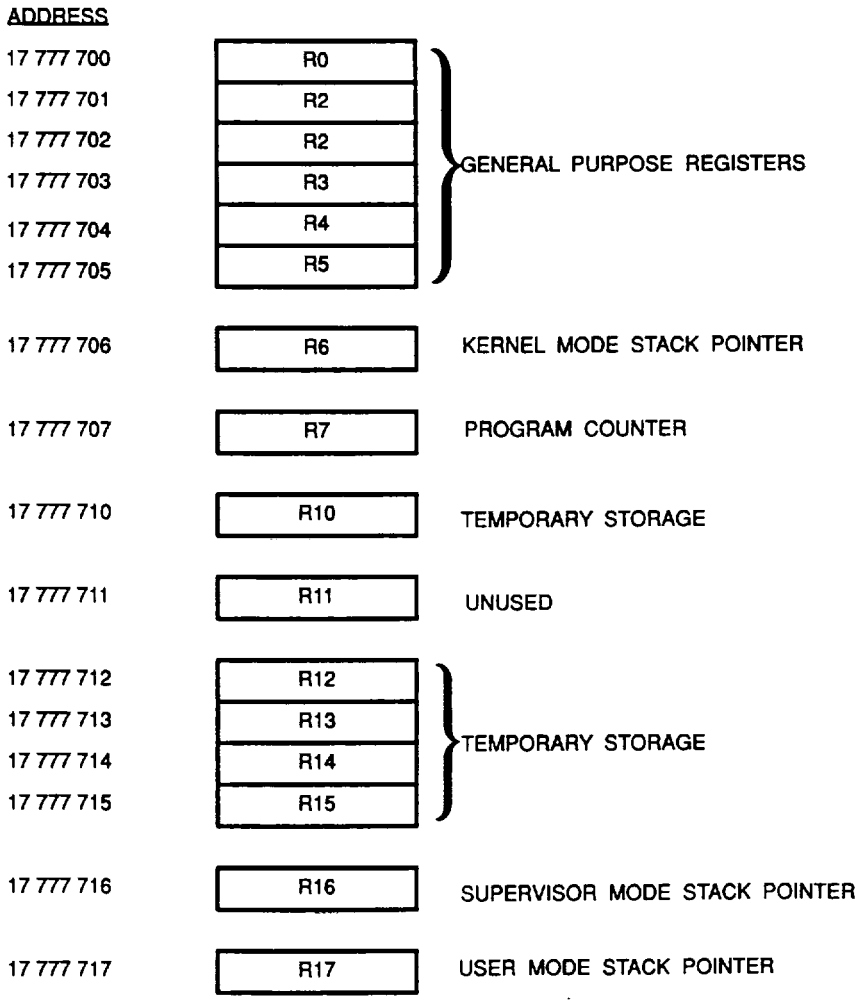
PIRQ Register Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

(1) CPU Registers (Cont.)

c. General Registers. The CPU contains several 16-bit general registers that can be used as accumulators, index registers, auto-increment registers, auto-decrement registers or as stack pointers for temporary storage of data. A few of these registers are used for special purposes. Register 7 (R7) is used as the program counter (PC) and contains the address of the next instruction to be executed. R6 is generally used as the processor stack pointer (SP) if the processor is in kernal mode. If the processor is in supervisor or user mode, R16 or R17 is used as the processor stack pointer, respectively.



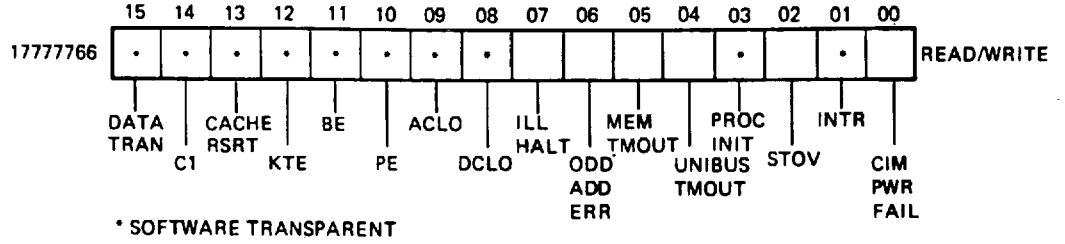
General Register Utilization

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

(1) CPU Registers (Cont.)

d. Error Register. This register identifies the source of the abort or trap that used the vector at location 4. Bits 07:04, bit 02 and bit 00 are cleared when the CPU error register is written; the remaining bits are software transparent and are accessible only when the console has control

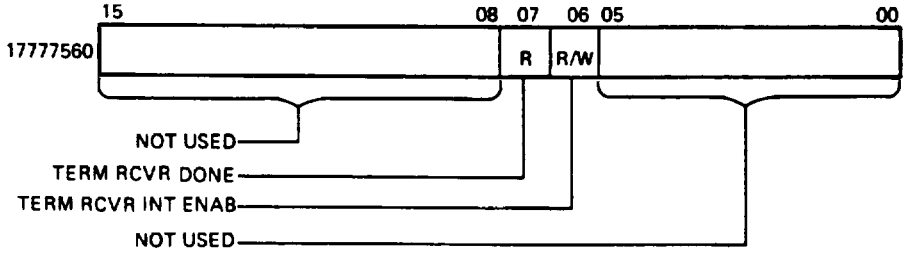


CPU Error Register Format

(2) Multifunction Module Registers

The multifunction module (MFM) contains two serial line units (SLU's) which provide the interface ports between the serial line devices and the AN/UYK-42(V)4 processor. In the AN/UYK-42(V)4, the SMI modules effectively extend the number of serial data ports to 12. The console terminal can operates as a standard I/O device or as a programmer's console to access and load registers within the CPU.

a. Console Terminal Receiver Control/Status Register(RCSR). The figure below shows the format of the console terminal receiver control/status register (RCSR).



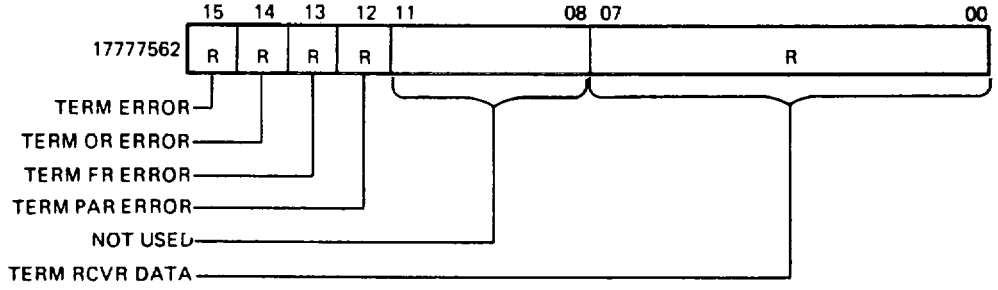
Console Terminal RCSR Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

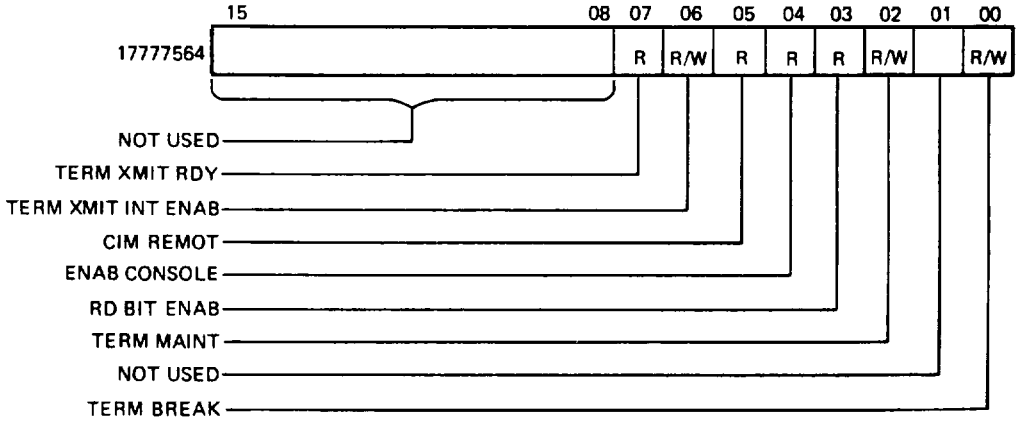
(2) Multifunction Module Registers (Cont.)

b. Console Terminal, Receiver Data Buffer (RBUF). The figure below shows the format of the console terminal receiver data buffer register.



Console Terminal RBUF Format

c. Console Terminal Transmitter Control/Status Register(XCSR). The figure below shows the format of the console terminal transmitter control and status register (XCSR).

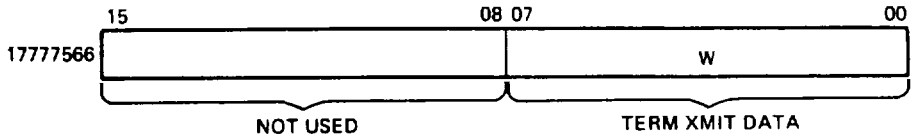


Console Terminal XCSR Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

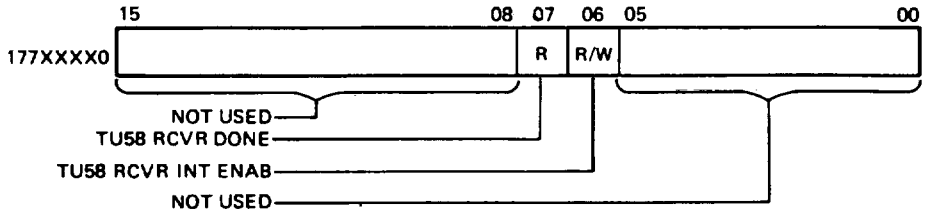
(2) Multifunction Module Registers (Cont.)

d. Console Terminal Transmitter Buffer Register (XBUF). The figure below shows the format of the console terminal transmitter register (XBUF).



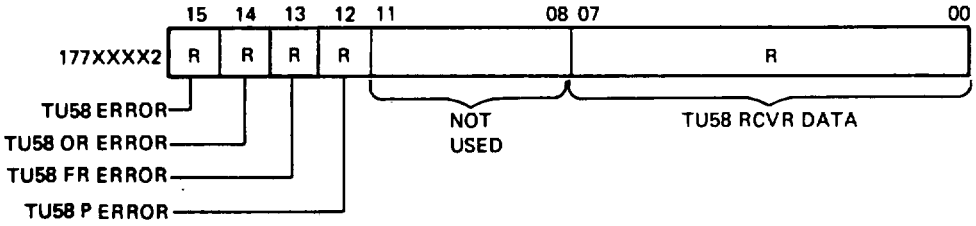
Console Terminal XBUF Format

e. TU58 Receiver Control/Status Register (RCSR). The figure below shows the format of the TU58 receiver control/status register (RCSR). The typical addresses assigned to the TU58 registers are from 17776500 to 17776506.



TU58 RCSR Format

f. TU58 Receiver Buffer Register (RBUF). The figure below shows the format of the TU58 receiver buffer register (RBUF).



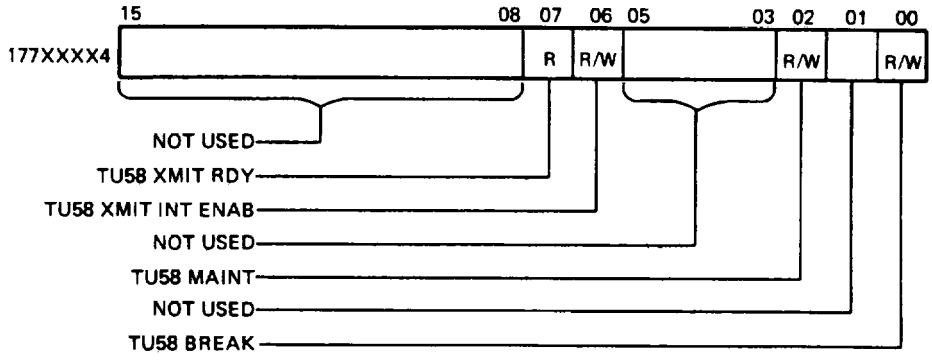
TU58 RBUF Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

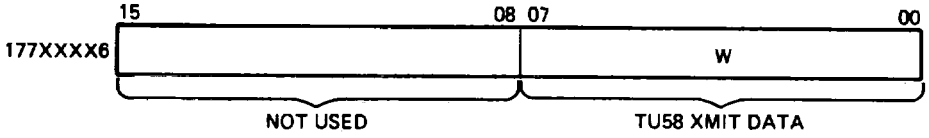
(2) Multifunction Module Registers (Cont.)

g. TU58 Transmitter Control/Status Register (XCSR). The figure below shows the format of the TU58 transmitter control/status register (XCSR).



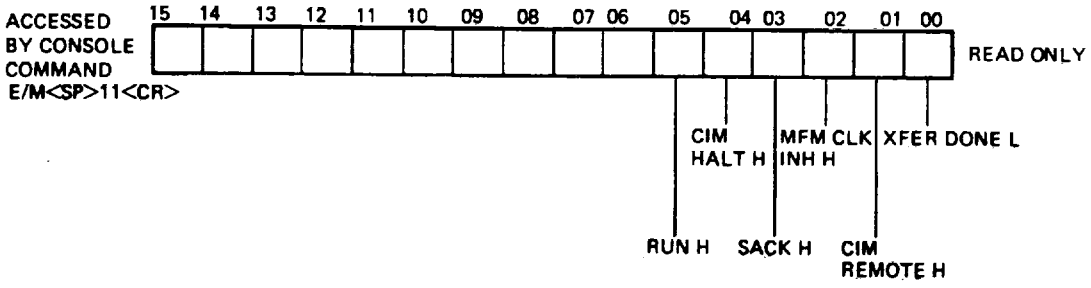
TU58 XCSR Format

h. TU58 Transmitter Data Buffer (XBUF) Register. The figure below shows the format of the TU58 transmitter buffer register (XBUF).



TU58 XBUF Format

i. Signal Register. The signal register provides information about the operational status of the MFM module and CPU. The figure below shows the format of the signal register.



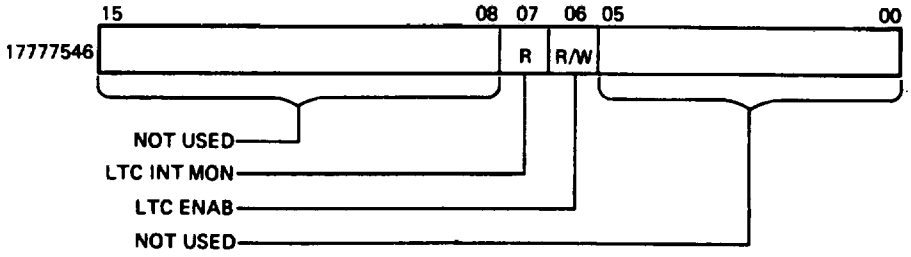
Signal Register Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

(2) Multifunction Module Registers (Cont.)

j. Line Time Clock Control/Status Register (LKS). The figure below shows the format of the Line Time Clock Control Status Register (LKS'



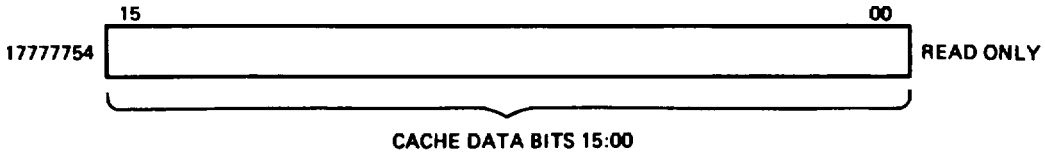
Line Time Clock (TCSR) Format

Line Time Clock (TCSR) Format

(3) Cache Memory I/O, Page Registers.

The cache memory module contains several registers that are used to store data information, error indications, and control and status information.

a. Cache Memory Data Register (CDR). The cache memory data register (CDR) is loaded from the 16-bit data array section of the cache RAM when a read-access occurs to main memory. The figure below shows the CDR format.



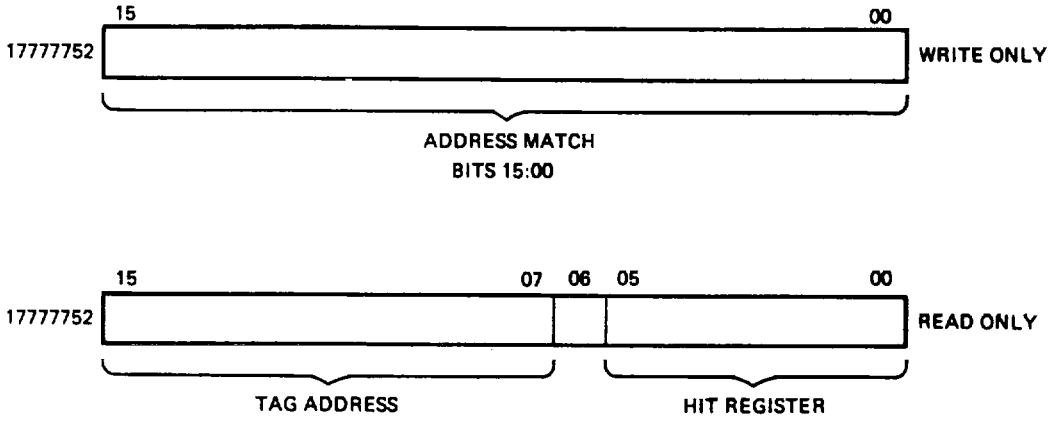
Cache CDR Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

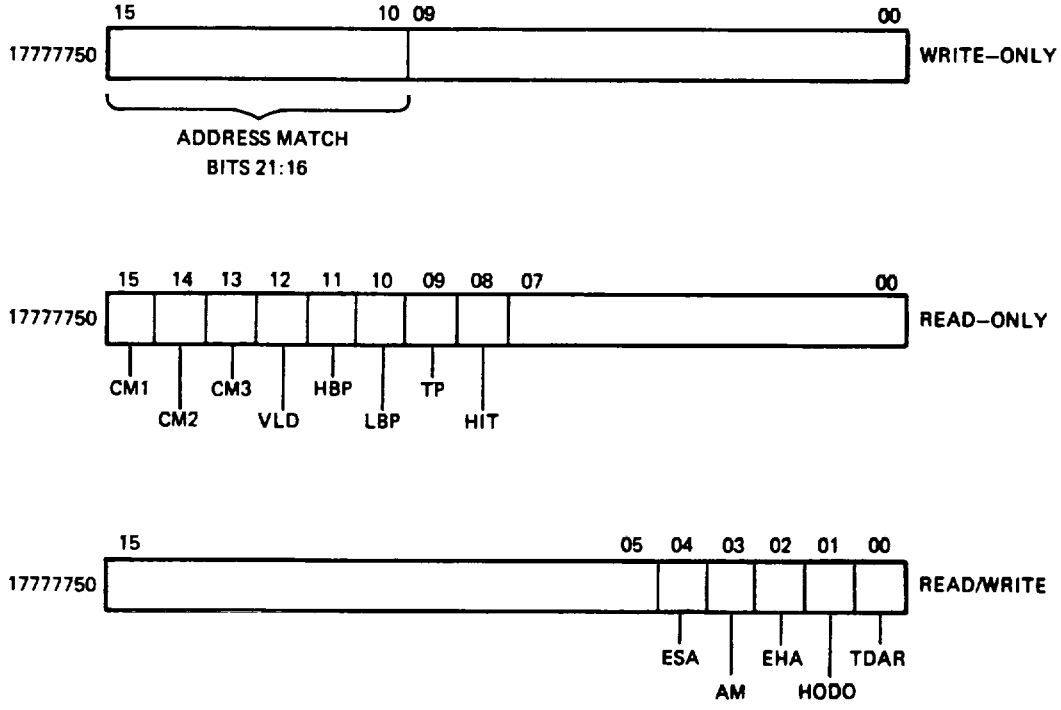
(3) Cache Memory I/O, Page Registers (Cont.)

b. Cache Hit Register (CHR). The cache hit register (CHR) is a dual-purpose register used as an address match register when written and as a tag address/hit register when read.



Cache CHR Format

c. Cache Maintenance Register (CMR). The cache maintenance register (CMR) is a dual-purpose register. The high byte is used as an address match register when written and contains maintenance bit when read. The lower byte contains read/write maintenance bits. The figure below shows the format of the CMR register.



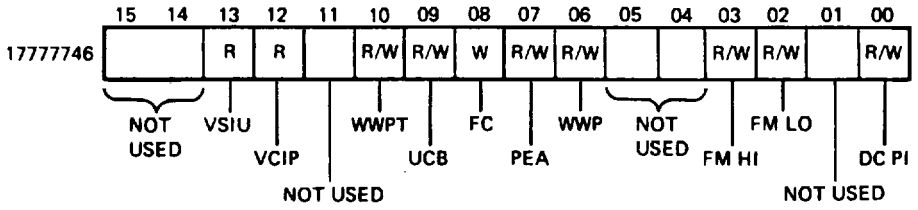
Cache CMR Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

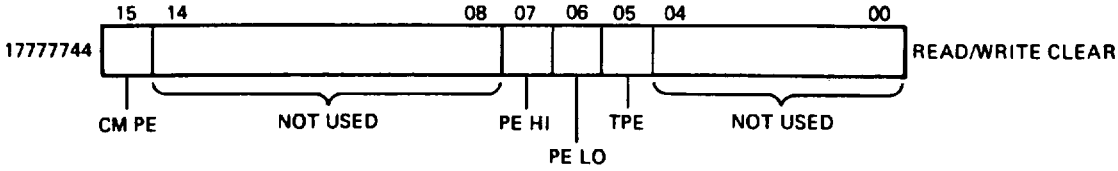
(3) Cache Memory I/O, Page Registers (Cont.)

d. Cache Control/Status Register (CCSR). The figure below shows the format of the cache CCSR.



Cache CCSR Format

e. Cache Error Register (CME). The figure below shows the format of the cache CME register.



Cache CME Format

(4) Memory Management Registers.

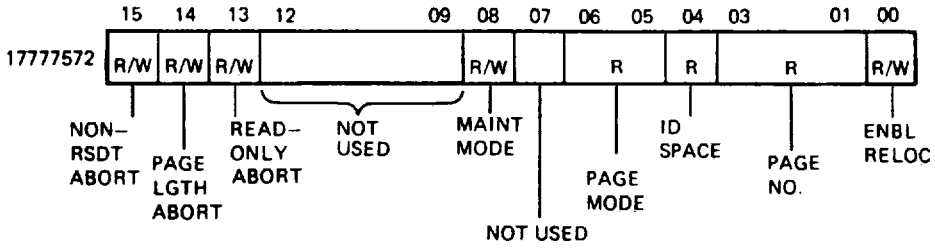
The 16-bit virtual address is translated to a 22-bit physical address by the memory management function. Four status registers, 48-page address registers (PAR), and 48-page descriptor registers (PDR) are associated with the memory management.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

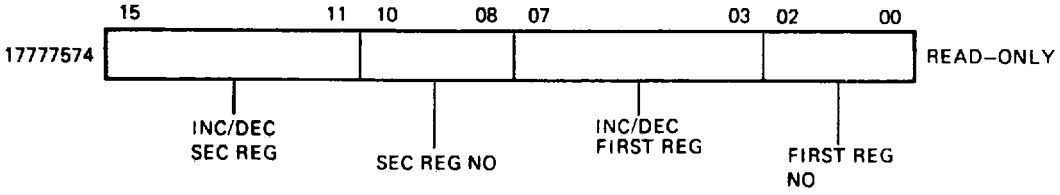
(4) Memory Management Registers (Cont.)

a. Status Register 0 (SRO). Memory management status register 0 (SRO) contains error flags, the page number whose reference caused the abort and various status flags. The format of SRO is shown below.



Memory Management SRO Format

b. Status Register SR1. The format of memory management status register 1 (SR1) is shown below. SR1 records any auto-increment/decrement of the general purpose register, including explicit references through the PC. SR1 is cleared at the beginning of the fetch cycles for each instruction. Whenever a general purpose register is either auto-increment or auto-decrement, the register number and the amount in 2's complement notation by which the register was modified are written into SR1. A single operand instruction will only set the lower byte with the source register change and the upper byte with the destination register change.



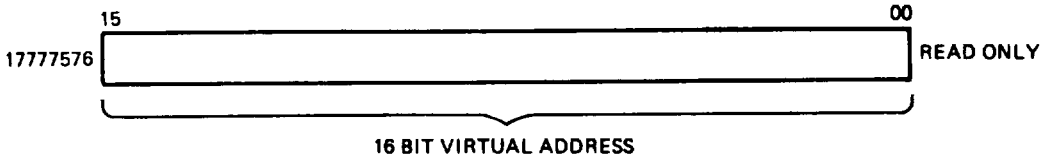
Memory Management SRI Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

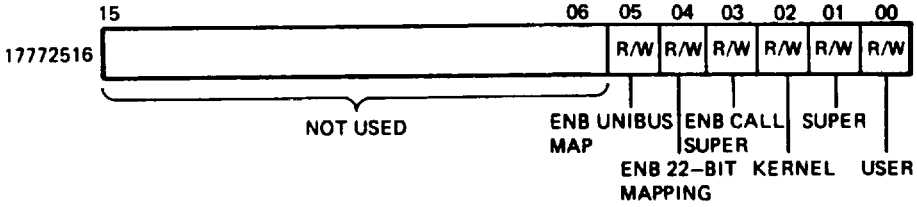
(4) Memory Management Registers (Cont.)

c. Status Register SR2. The status register SR2 is loaded with the value of the program counter at the beginning of the fetch cycle of each instruction. At the beginning of an interrupt, SR2 contains the address trap vector, the T bit, parity traps, odd address, parity and time-out aborts. The figure below shows the format of SR2.



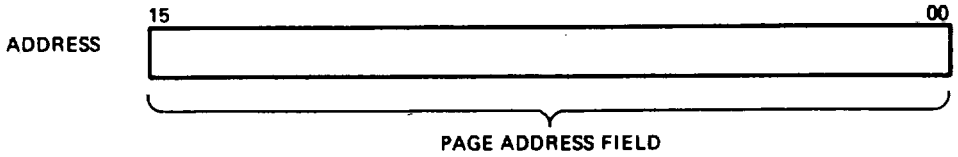
Memory Management SR2 Format

d. Status Register SR3. The following figure shows the format of SR3.



Memory Management SR3 Format

e. Page Address Registers (PAR). The page address registers (PAR) contain the 16-bit page address field that specifies the base address of the page as a block number in physical memory. There are six sets of eight PARs, one set each for kernel data space, kernel instruction space, supervisor data space, supervisor instruction space, user data space and user instruction space.



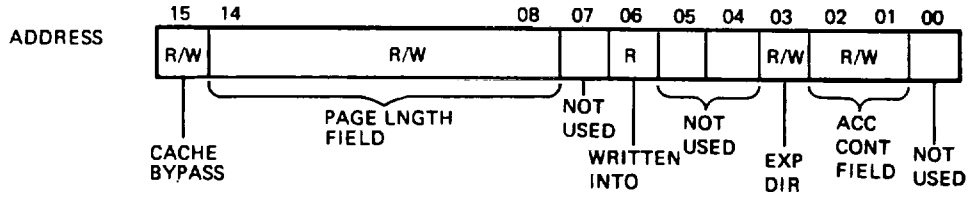
Memory Management PAR Format

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

b. AN/UYK-42(V)4 Registers (Cont.)

(4) Memory Management Registers (Cont.)

f. Page Descriptor Register (PDR). The page descriptor registers (PDRs) contain information relative to page expansion, page length and access control. There are six sets of eight PDRs which are allocated in the same manner as the PARs.



Memory Management PDR Format

c. Memory Management

The memory management system of the AN/UYK-42(V)4 provides the address relocation and memory protection facilities required in a multiprogramming system. This system enables several user programs to be located simultaneously in memory. Memory management includes three mapping schemes: 16-bit, 18-bit, or 22-bit. Mapping converts the 16-bit, processor-generated virtual address to a physical address. A separate mapping scheme, the UNIBUS map, converts 18-bit UNIBUS addresses to 22-bit memory addresses. This allows devices on the UNIBUS to communicate with main memory via nonprocessor requests (NPRs).

The AN/UYK-42(V)4's memory management system supports three processor modes: Kernel, Supervisor, and User. These modes permit a fully protected environment for a multiprogramming system providing the user with three distinct sets of processor stack and memory management registers for memory mapping. In all modes, except Kernel, a program is inhibited from executing a "HALT" instruction. Furthermore, the processor will ignore the "RESET" and "SPL" (set priority level) instructions and will execute No Operation. A program operating in Kernel mode can map users' programs anywhere in the memory and thus explicitly protect key areas from the User operating environment. In Kernel mode, the processor will execute all instructions.

The memory management system permits instructions or pure code to be mapped into physical memory separately from data. When this feature is enabled, instructions, index values and immediate operands are mapped through instruction (I) space. Data, or words that can be modified, are mapped through data (D) space. The I/D space facility

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

is enabled under software control. When it is disabled, all memory references are mapped through instruction space.

Memory management is used to relocate a 16-bit virtual address, if necessary, and transmit the 22-bit physical address to the UNIBUS, cache memory, or main memory. Address modification is the main function of memory management. The modification of addresses is called relocation because it consists of adding a fixed constant to a virtual address to create a physical address.

Memory management also allows the user to protect one section of memory from access by programs located in another section. Memory management divides memory into individual sections called pages. Each page has a protection or access key associated with it that defines the type of access allowed on that particular page. With the memory management unit, a page can be keyed nonresident (memory neither readable nor write-able) or read-only (no write operations to memory). These two types of protection, in association with other features, enable the user to develop a secure operating system.

It is often desirable to load a program into one area of physical memory and execute it as if it were located in another area of memory, for example, when several user programs are simultaneously stored in memory. When any one program is running, it must be accessed by the processor as if it were located in the set of addresses beginning at 0. This process is called relocation. When the processor accesses virtual bus address 0. a base address is added to it and the relocated 0 location of the program is accessed. Typically this base address is added to all references while the program is running. A different base address is used for each of the other programs in memory.

Memory management specifies relocation on a page basis, which allows a large program to be loaded into nonadjacent pages in memory. This capability eliminates the need to shuffle programs to accommodate a new one. It also minimizes unusable memory fragments, thus allowing more users to be loaded into a specific memory size.

A program and its data can occupy as many as 16 pages in the memory. The size of each page may vary and can be any multiple of 32 words up to 4096 words in length. This feature allows small areas of memory to be protected (stacks, buffers, etc.), and also allows the last page of program, exceeding 4K words, to be of adequate length to protect and relocate the remainder of the program. As a result, the memory fragmentation problem inherent with fixed-length pages is eliminated. The base address of each page can be any multiple of 32 words in the physical address space, thus ensuring efficient use of main memory. The variable page length also allows the pages to be dynamically changed at run time.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

Memory management provides three separate sets of pages for use in the processor's kernel, supervisor, and user modes. These sets of pages increase system protection by physically isolating user programs from service supervisor programs and the kernel program. The service programs are also separated from the kernel program. Separate relocation register sets greatly reduce the time necessary to switch context between mapping. The three sets of registers also aid in designing an operating system that has clearly defined communications, is modular, and is more easily debugged and maintained.

The virtual bus address space is further divided, within each of the kernel, supervisor, and user pages, into instruction space and data space (I and D space). I space contains code, that is, any word that is part of the program such as instructions, index words and immediate operands. D space contains information that can be modified, such as data buffers.

By using this feature, memory management can relocate data and instruction references with separate base address values. Therefore, it is possible to have a user program of 64K words consisting of 32K of instructions and 32K of data.

(1) Relocation

When memory management is enabled, the normal 16-bit direct-byte address is no longer interpreted as a direct physical address (PA) but as a virtual bus address (VBA) containing information to be used in constructing a new 22-bit PA. The information contained in the VBA is combined with relocation information contained in the page address register (PAR) to make a 22-bit PA. Using memory management, memory can be dynamically allocated in pages composed of from 1 to 128 blocks of 32 words each.

The starting PA for each page is a multiple of 32 words, and each page has a maximum size of 4096 words. Pages may be located anywhere within the PA space. The set of 16 PARs to be used to create the PA is determined by the current mode of operation of the CPU (kernel, supervisor, or user).

a. Address Mapping. All addresses with memory relocation enabled reference information in either instruction (I) space or data (D) space. I space and D space each have eight PARs in each mode of CPU operation. Using register SR3, the operating system may select to disable D space and map all references through I space, or to use both I and D space.

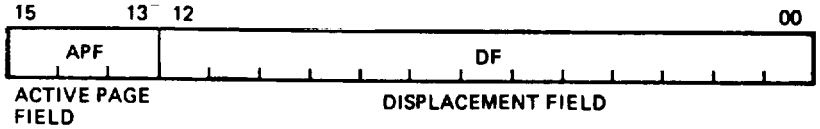
1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(1) Relocation (Cont.)

a. Address Mapping (Cont.)

The basic information needed for the construction of a PA comes from the VBA, which is illustrated below, and the appropriate PAR set.



Interpretation of VBA

The VBA consists of:

1. The Active Page Field (APF) - This 3-bit field determines which of the eight PARs will form the PA.

2. The Displacement Field (DF) - This 13-bit field contains an address relative to the beginning of a page. This permits page lengths of up to 4K words. The DF is further subdivided into two fields as shown below.

Displacement Field

The displacement field consists of:

1. The Block Number (BN) - This 7-bit field is interpreted as the block number within the current page.

2. The Displacement in Block (DIB) - This 6-bit field contains the displacement within the block referred to by the block number (BN).

The remainder of the information needed to construct the PA comes from the 16-bit page address field (PAF) which is contained in

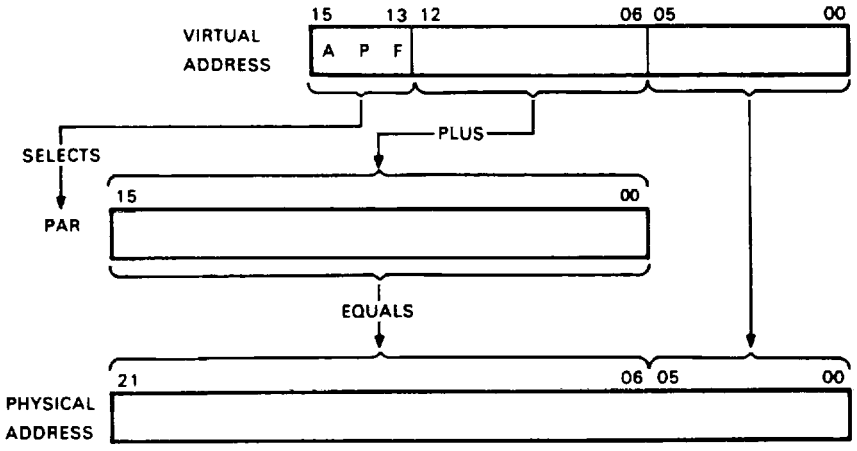
1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(1) Relocation (Cont.)

a. Address Mapping (Cont.)

the PAR and specifies the starting address of the memory page. The PAF is actually a block number in the physical memory, for example, PAF=3 indicates a starting address of 96 (3x32) words in physical memory. The formation of the PA is illustrated below.



Construction of PA

The logical sequence involved in constructing a PA is as follows:

1. Select a set of PARs, depending on the space being referenced (I or D).

2. The APF of the VBA is used to select a PAR(PARO-PAR7).

3. The PAF of the selected PAR contains the starting address of the currently active page as a block number in physical memory.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(1) Relocation (Cont.)

a. Address Mapping (Cont.)

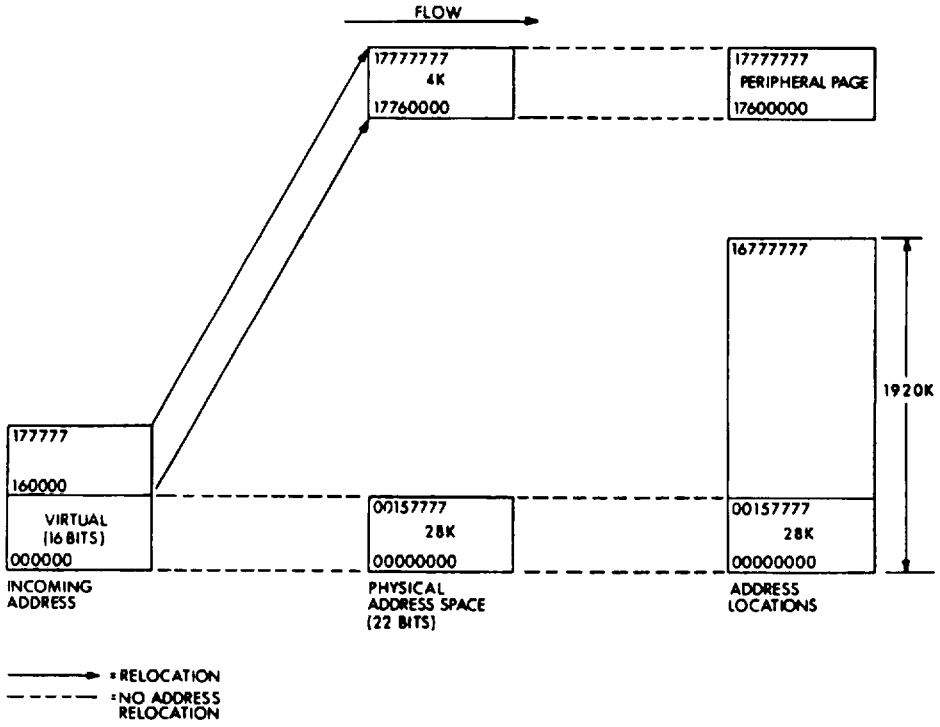
4. The block number (BN) from the VBA is added to the PAF to yield the number of the physical block in memory which will contain the PA being constructed.

5. The displacement in block (DIB) from the displacement field (DF) of the VBA is joined to the physical block number to yield

a 22-bit PA.

b. Address Translation

1. 16-Bit Mapping. In 16-bit mapping, the PA space consists of 28K memory locations (PA= 00000 000 --00 157 777) and the 4K peripheral page (PA=17 760 000-17 777 777). Physical addresses 00 160 000 - 17 577 777 cannot be generated when using 16-bit mapping.



16-Bit Mapping

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

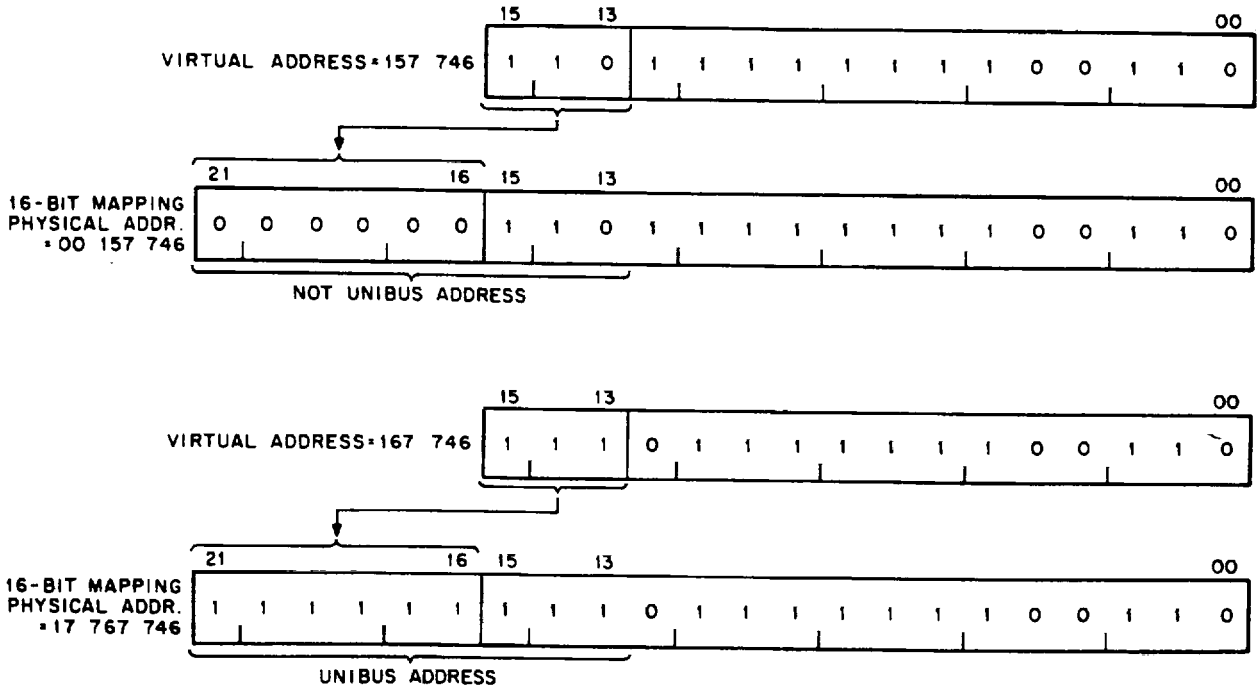
c. Memory Management (Cont.)

(1) Relocation (Cont.

b. Address Translation (Cont.)

1. 16-Bit Mapping (Cont.)

A 16-bit VBA is the PA if bits 15:13 are not equal to 111. In this case bits 21:16 of the PA are made zeros and bits 15:00 of the PA are the same as bits 15:00 of the VBA. If bits 15:13 of the VBA are equal to 111, then a reference to the peripheral page is intended by the program and bits 21:16 of the PA are set to 1 and bits 15:00 are the same as the VBA.



16-Bit Mapping: Generation of PA

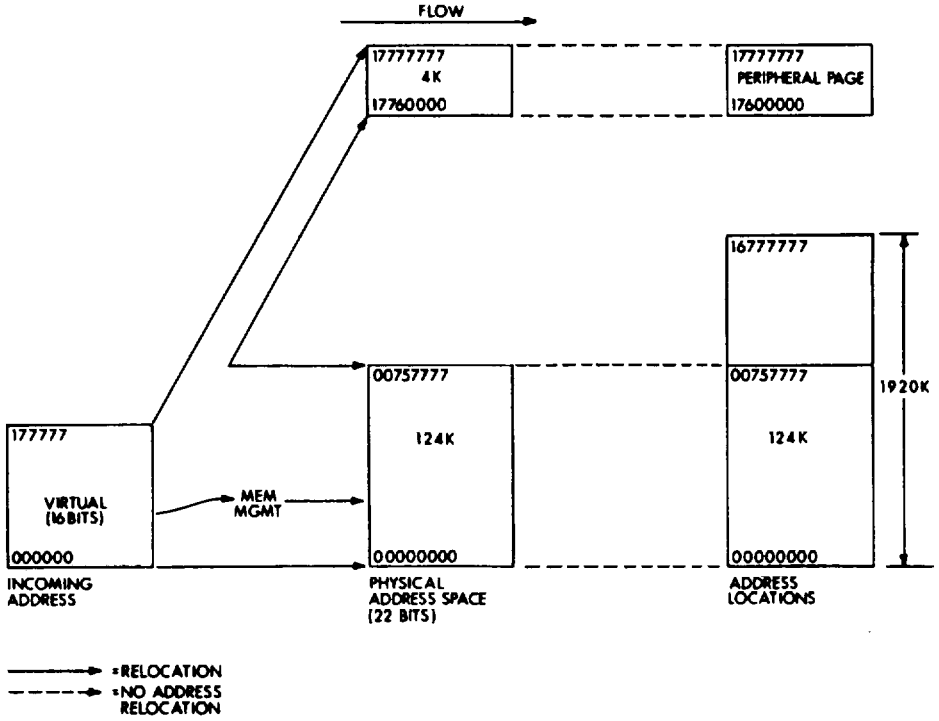
1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(1) Relocation (Cont.)

b. Address Translation (Cont.)

2. 18-Bit Mapping. In 18-bit mapping the VBA is added to the selected PAF to generate the PA. This address mode has a range of 128K. The PA space consists of 124K (00 000 000-00 757 777) and the 4K peripheral page (17760000 - 17777777).



18-Bit Mapping

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

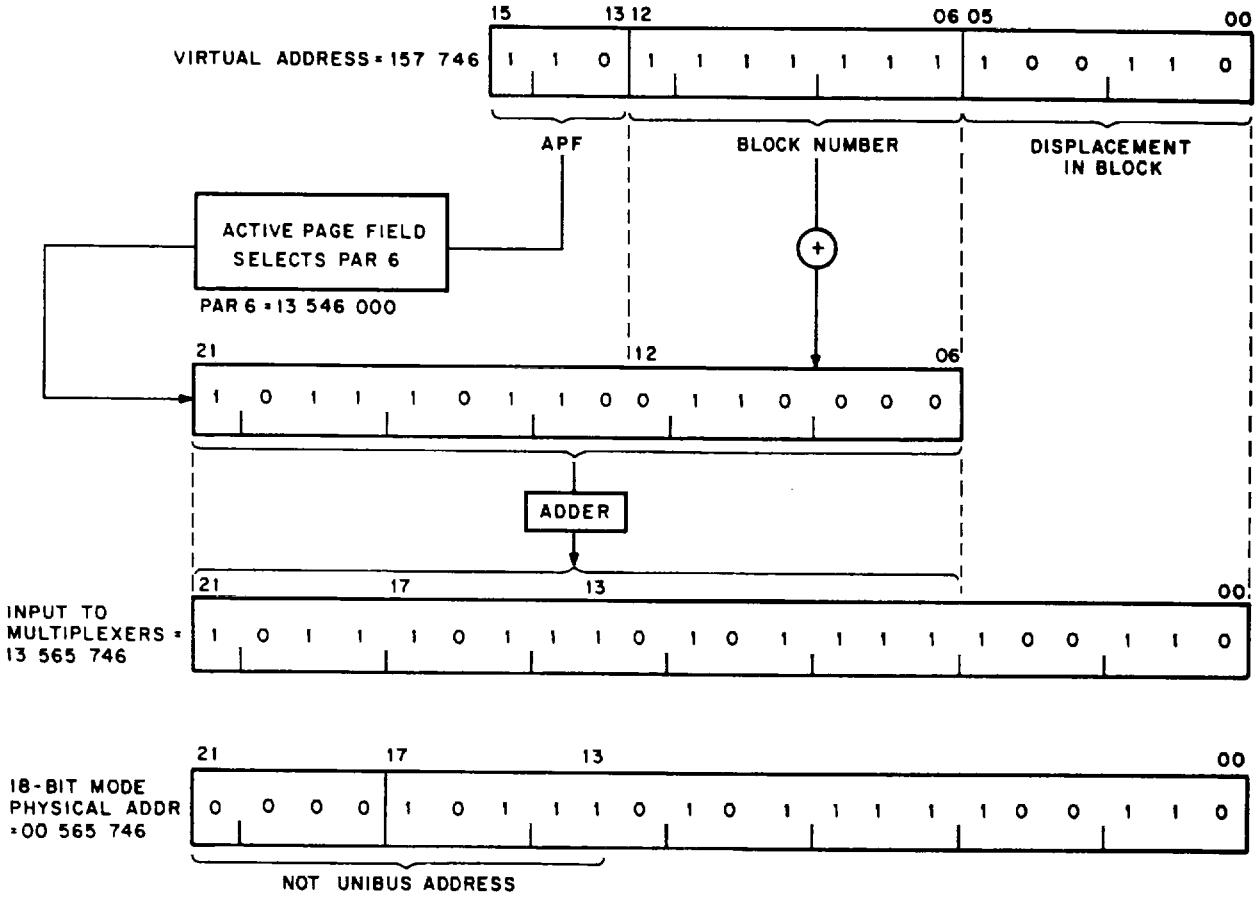
c, Memory Management (Cont.

(1) Relocation (Cont.)

b. Address Translation (Cont.)

2. 18-Bit Mapping (Cont.)

The figure below illustrates an 18-bit PA that is not a UNIBUS reference, that is, bits 17:13 are not all ones. In this case, bits 21:18 of the PA are set to zeros, which causes a memory reference.



18-Bit Mapping: Memory Address

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

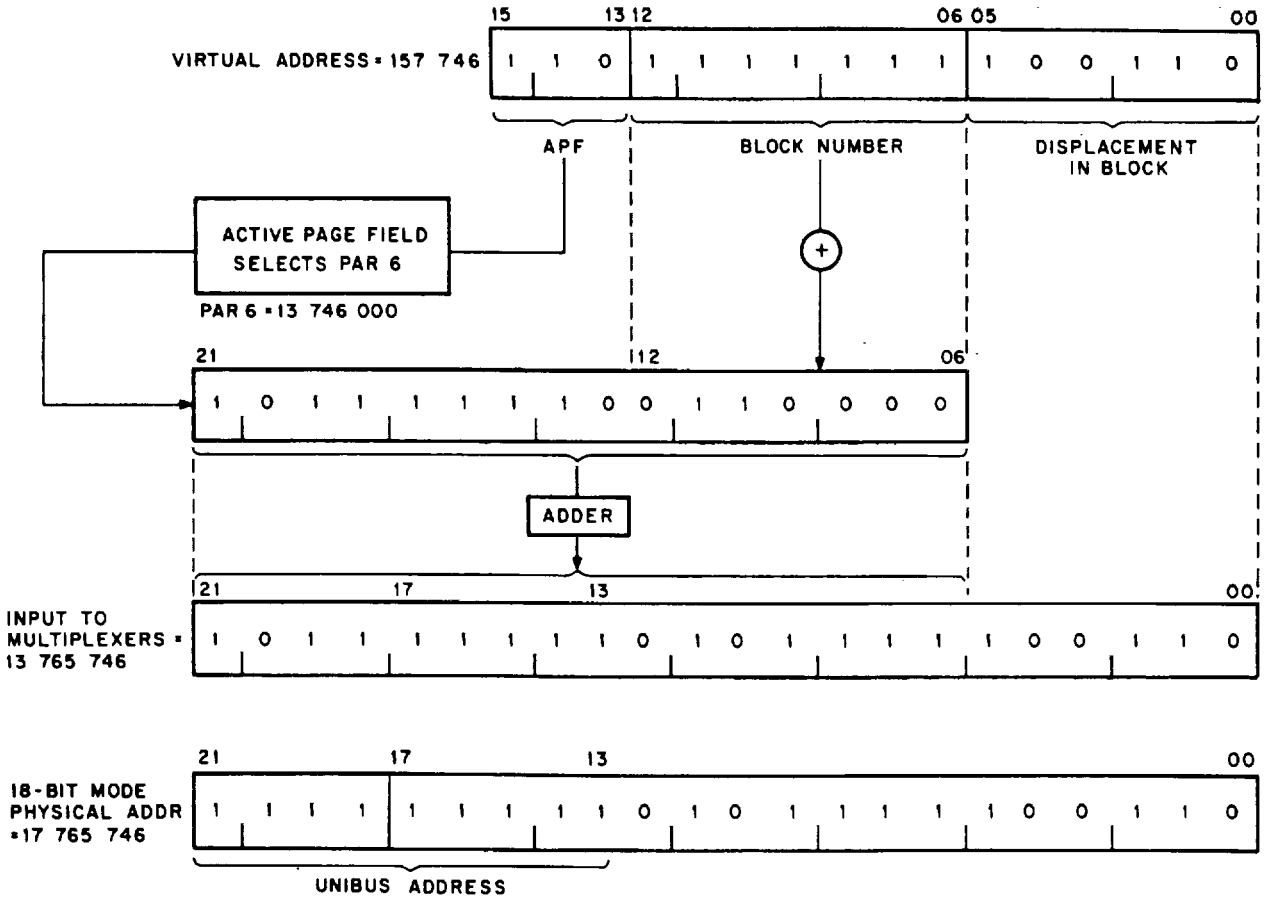
c. Memory Management (Cont.)

(1) Relocation (Cont.)

b. Address Translation (Cont.)

2. 18-Bit Mapping (Cont.)

The figure below illustrates an 18-bit relocated address that is UNIBUS reference, that is, bits 17:13 are all ones. In this case, its 21:18 of the PA are changed to ones, which causes a UNIBUS reference.



18-Bit Mapping: UNIBUS Address

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

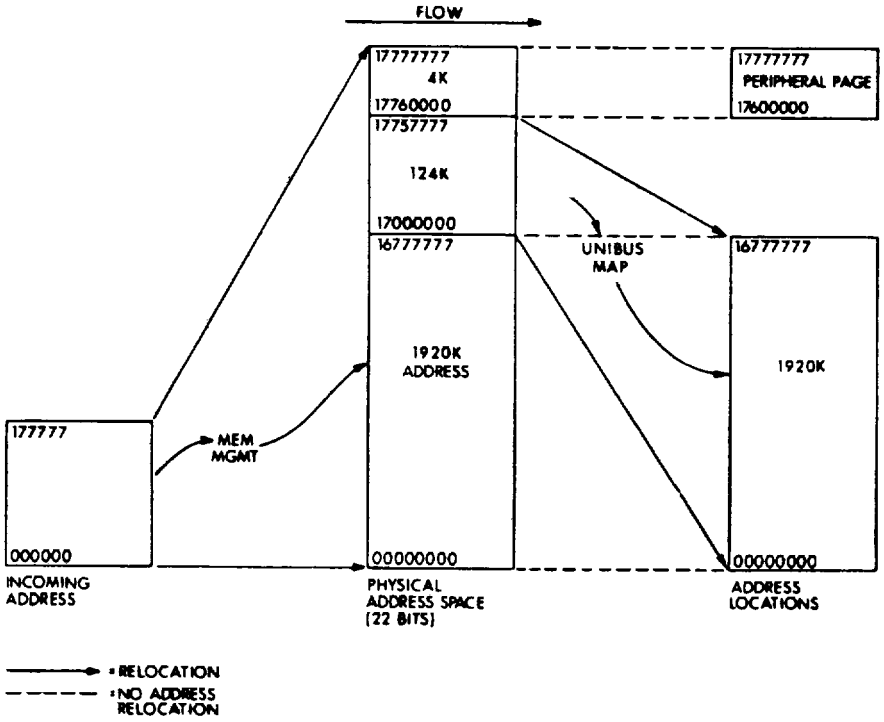
c. Memory Management (Cont.)

(1) Relocation (Cont.)

b. Address Translation (Cont.)

2. 22-Bit Mapping

In 22-bit mapping the VBA is relocated in the same manner as 18-bit mapping, but the relocated address becomes the PA without modification. Thus, all PAs from 00 000 000 - 17 777 777 can be generated. Addresses 17 760 000 - 17 777 777 are UNIBUS I/O page references. Addresses 00 000 000 - 16 777 777 are memory addresses. The top 124K of addresses 17 000 000 - 17 757 777 may be used to access memory via the UNIBUS map.



22-Bit Mapping

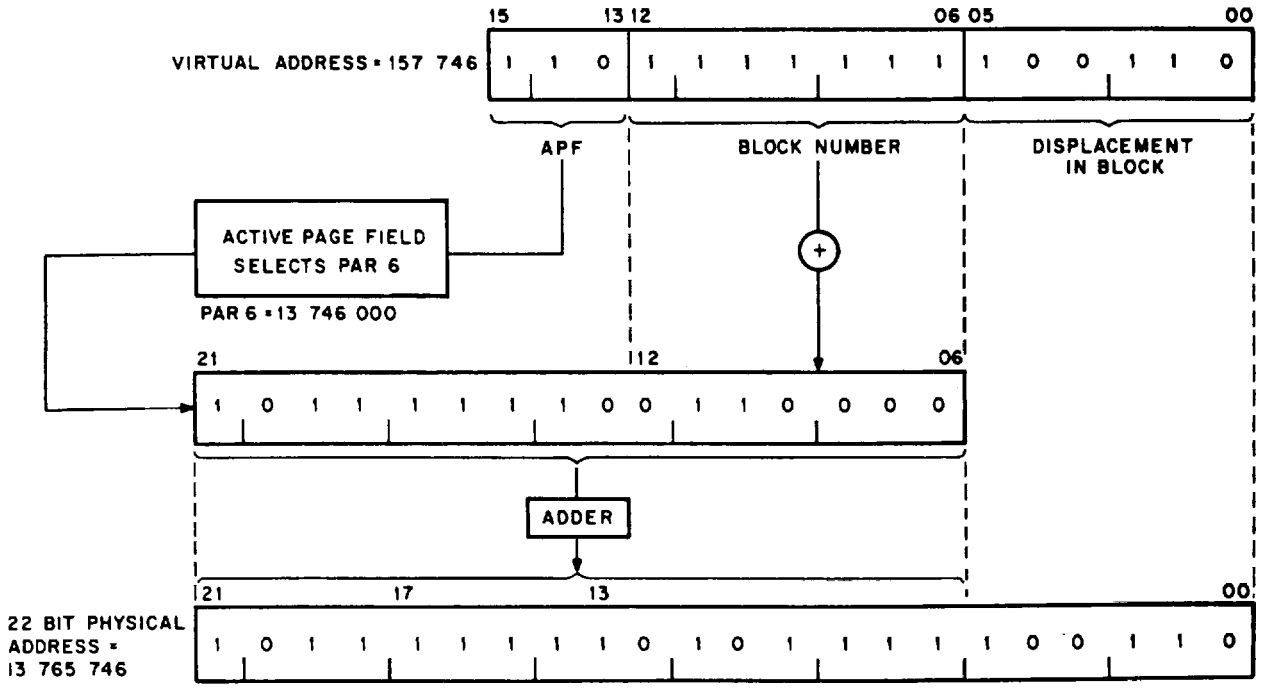
1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(1) Relocation (Cont.)

b. Address Translation (Cont.)

2. 22-Bit Mapping (Cont.)



22-Bit Address Mapping

(2) Protection

A timesharing system performs multiprogramming; it allows several programs to reside in memory simultaneously, and to operate sequentially. Access to these programs and the memory space they occupy must be strictly defined and controlled. Several types of protection must be afforded a timesharing system.

a. User programs must not be allowed to expand beyond allocated space, unless authorized by the system.

b. Users must be prevented from modifying common subroutines and algorithms that are resident for all users.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(2) Protection (Cont.)

c. Users must be prevented from gaining control of or modifying the operating system software.

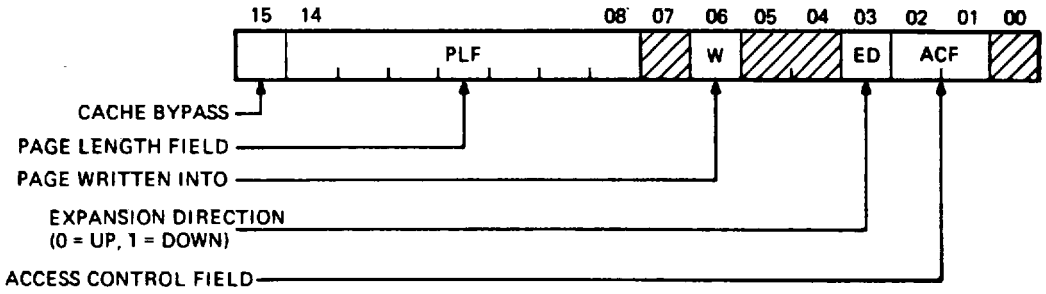
The memory management logic provides the hardware facilities to implement all of the above types of memory protection.

(3) Page Address Registers (PAR)

The page address registers contain the constant or base address which memory management adds to the VBA to create a 22-bit physical address. The forty-eight 16-bit PARs are made up of four 256x4 random-access memories. These registers can either read or written.

(4) Page Descriptor Registers (PDR)

In addition to its relocation function, memory management has supervisory or memory protection functions which are determined by the contents of the PDR. The PDR is read at the same time as its corresponding PAR during relocation and contains all the information required for the supervisory or memory protection functions. The figure below shows the PDR.



Page Descriptor Register

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(4) Page Descriptor Registers (PDR) (Cont.

a. Access Control Field (ACF)

This 2-bit field, occupying bits 2:1 of the PDR, contains the access rights to a particular page. The keys specify the manner in which a page may be accessed and whether or not a particular access should result in an abort of the current operation. In the context of access control, the term 'write' is used to indicate the action of any instruction which modifies the contents of any addressable word.

The access control keys are the following.

ACF	DESCRIPTION	FUNCTION
00	nonresident	abort all accesses
01	read only	abort all write attempts
10	illegal mode	abort all accesses
11	'read/write	read or write allowed

It should be noted that the use of I space in conjunction with read only access provides the user with another form of protection Execute Only.

b. Expansion Direction (ED)

Bit 3 of the PDR specifies the direction the page is to expand. If ED=0, the page expands upward from block number 0 to include blocks with higher addresses (next figure). If ED=1 the page expands downward from block number 1778 to include blocks with lower addresses (subsequent figure). Upward expansion is typically used for program space, and downward expansion for stack space.

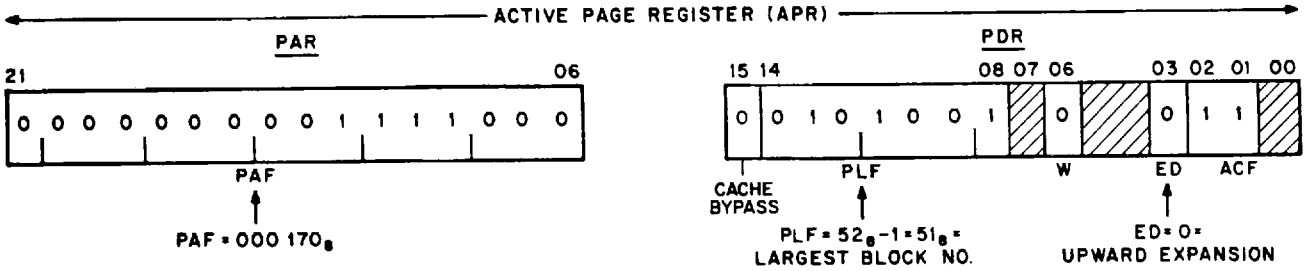
c. Written Into (W)

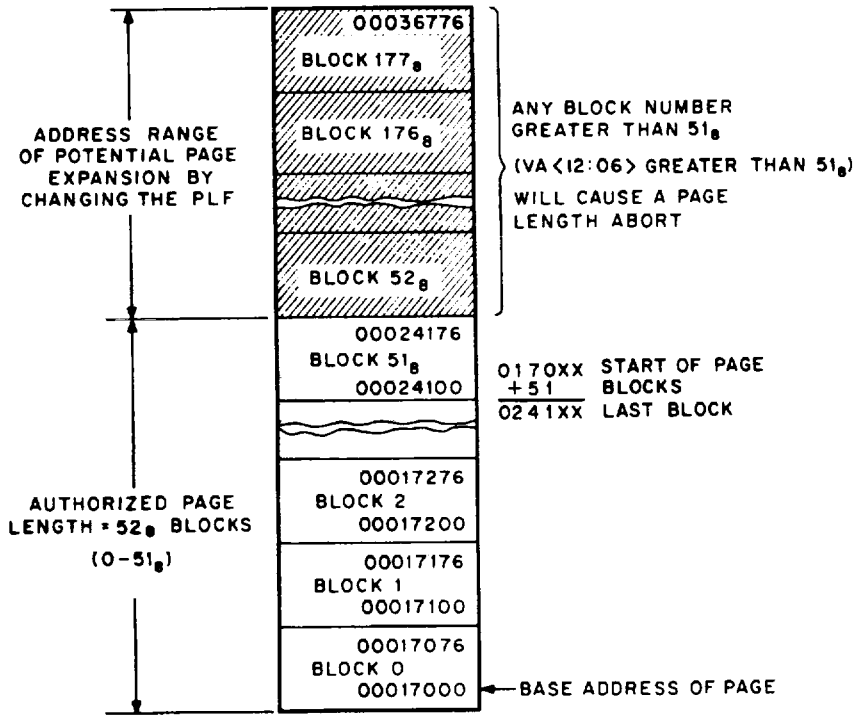
The W bit, bit 6, indicates whether or not the specified page has been modified (written into) since either the PAR or PDR was loaded (W=1 is affirmative). The W bit is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and must be saved in their new form, and which pages have not been modified and can be simply overlayed. The W bit is reset to 0 whenever the PAR or PDR associated with it is written into.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(4) Page Descriptor Registers (PDR) (Cont.)



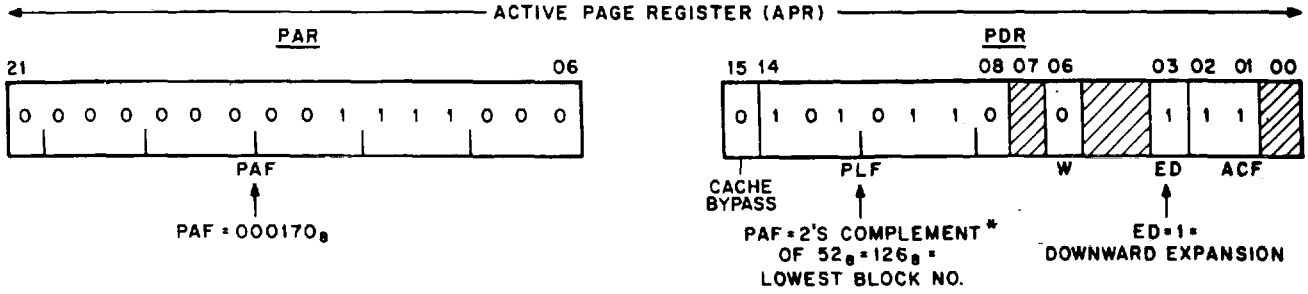


Upward Expansion

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

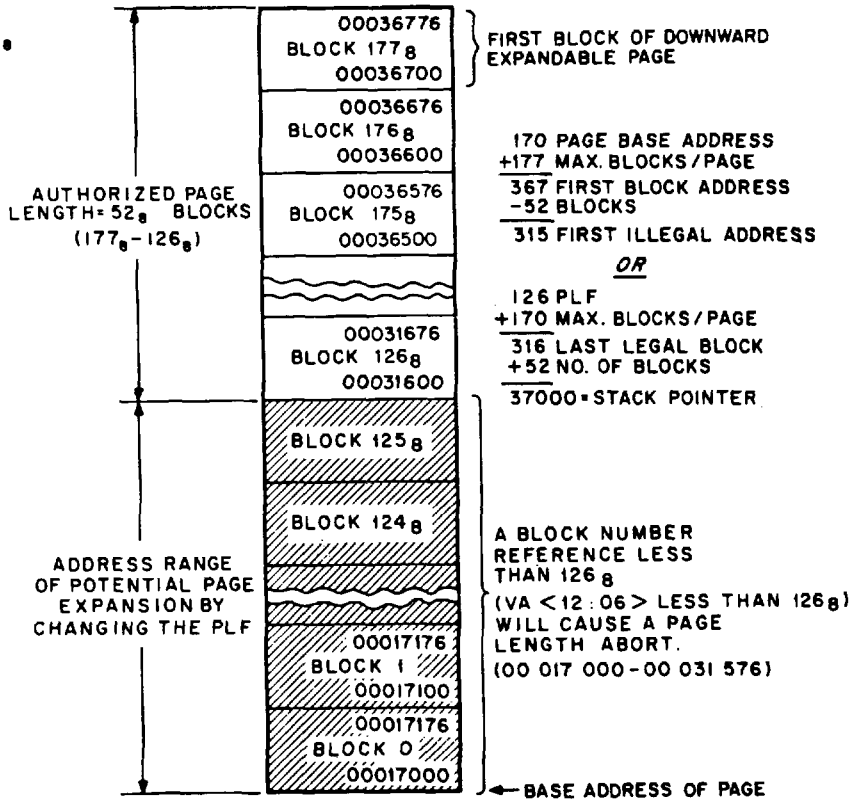
c. Memory Management (Cont.)

(4) Page Descriptor Registers (PDR) (Cont.)



* 2'S COMPLEMENT = 1'S COMPLEMENT + 1:

$52_8 = 0101010$
1'S COMP = 1010101
+ 1
$1010110 = 126_8$



Downward Expansion

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

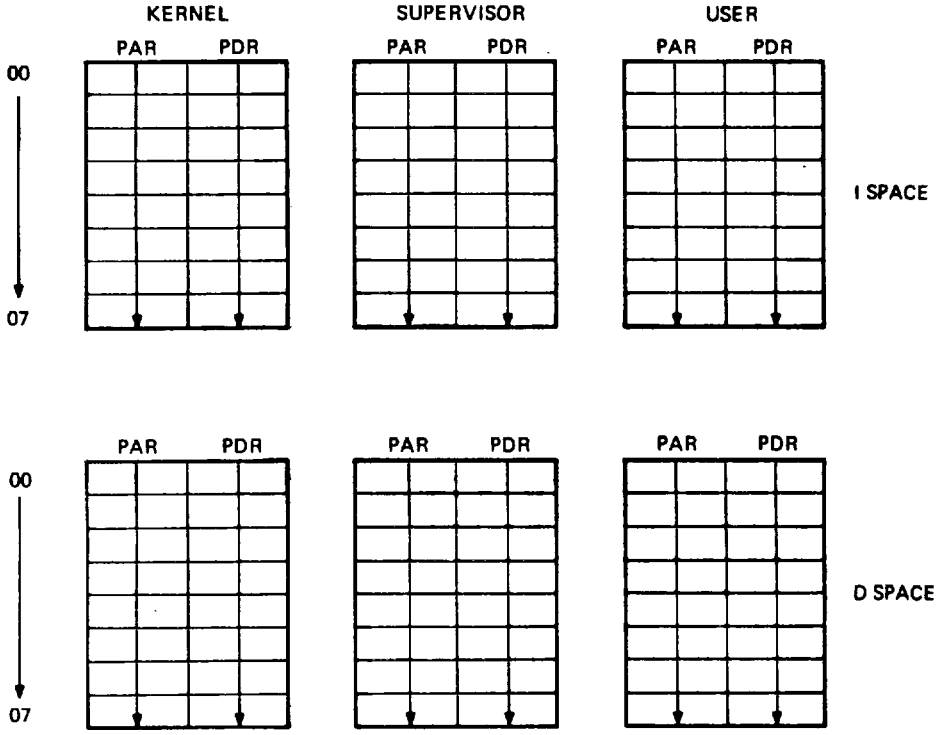
(4) Page Descriptor Registers (PDR) (Cont.)

d. Page Length Field (PLF)

The 7-bit field occupying bits 14:08 of the PDR specifies the block number (BN) which makes up the boundary of that page. The BN of the VBA is compared against the PLF to detect page length errors. An error occurs when expanding upward if the BN is greater than the PLF, and when expanding downward if the BN is less than the PLF..

(5) I and D Space

The concept of I and D space is used in mapping information into separate physical memory segments depending on whether the information is considered instructions (I) or data (D). In PDP-11 architecture all instruction fetches, immediate mode operands, absolute addressees, and index words are located in I space; any other memory reference that does not fit into these catagories is located in D space. In the PDP-11/44 separate PARs and PDRs are used for I and D space relocations.



Memory Management Relocation Registers

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

c. Memory Management (Cont.)

(4) I and D Space (Cont.)

Bits 02:00 of SR3 enable D space for each of the three processor operating modes: bit 00 user, bit 01 supervisor, bit 02 kernel. The hardware then selects the correct register set. If D space is not enabled for a particular operating mode, all references are then relocated through I space.

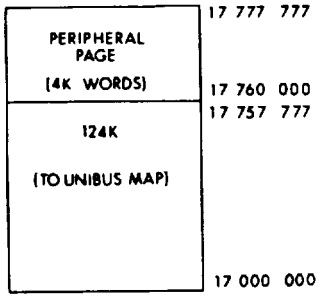
The use of I and D space allows programs to exist in two virtual segments and effectively doubles the addresses available to the user from 32K words to 64K words.

d. UNIBUS Map

The UNIBUS map is the interface between the UNIBUS and main memory. It responds as a slave device to UNIBUS signals and converts 18-bit UNIBUS addresses to 22-bit memory addresses.

The top 4K word addresses of the 128K UNIBUS addresses are reserved for the CPU and I/O registers and are called the peripherals page. The lower 124K addresses are used by the UNIBUS map to reference physical memory.

UNIBUS Address Space



The UNIBUS map is made up of a 21-bit adder and 32 mapping registers which may be written or read. These registers are 21 bits wide and require two UNIBUS transactions for each read or write. Therefore, 64 addresses are allotted to them on the I/O page (Table next page). It should be noted that the last mapping register (addresses 17 770 374 and 17 770 376) can be read and written, but cannot be used to map UNIBUS addresses because it would be used by addresses in the range of the peripherals page (17 760 000 - 17 777 777).

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

d. UNIBUS Map (Cont.)

Table: Access to Unibus Map Registers

Register No.	UNI BUS Address	Read or Write	UNIBUS Address for Memory Reference
	HI	LO	
0	17 770 200,	02	17 000 000 - 17 017 777
I	17 770 204,	06	17 020 000 - 17 037 777
2	17 770 210,	12	17 040 000 - 17 057 777
3	17 770 214,	16	17 060 000 - 17 077 777
4	17 770 220,	22	17 100 000 - 17 117 777
5	17 770 224,	26	17 120 000 - 17 137 777
6	17 770 230,	32	17 140 000- 17 157 777
7	17 770 234,	36	17 160 000 - 17 177 777
10	17 770 240,	42	17 200 000 - 17 217 777
11	17 770 244,	46	17 220 000 - 17 237 777
12	17 770 250,	52	17 240 000 - 17 257 777
13	17 770 254,	56	17 260 000 - 17 277 777
14	17 770 260,	62	17 300 000 - 17 317 777
15	17 770 264,	66	17 320 000 - 17 337 777
16	17 770 270,	72	17 340 000 - 17 357 777
17	17 770 274,	76	17 360 000 - 17 377 777
20	17 770 300,	02	17 400 000 - 17 417 777
21	17 770 304,	06	17 420 000 - 17 437 777
22	17 770 310,	12	17 440 000 - 17 457 777
23	17 770 314,	16	17 460 000 - 17 477 777
24	17 770 320,	22	17 500 000 - 17 517 777
25	17 770 324,	26	17 520 000 - 17 537 777
26	17 770 330,	32	17 540 000 - 17 557 777
27	17 770 334,	36	17 560 000 - 17 577 777
30	17 770 340,	42	17 600 000 - 17 617 777
31	17 770 344,	46	17 620 000 - 17 637 777
32	17 770 350,	52	17 640 000 - 17 657 777
33	17 770 354,	56	17 660 000 - 17 677 777
34	17 770 360,	62	17 700 000 - 17 717 777
35	17 770 364,	66	17 720 000 - 17 737 777
36	17 770 370,	72	17 740 000 - 17 757 777
*37	17 770 374,	76	17 760 000 - 17 777 777

*Can be read or written into, but not used for mapping.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

d. UNIBUS Map (Cont.)

The UNIBUS map does relocation by adding one of 31 UNIBUS map registers , which contain a relocation constant, to the 18-bit UNIBUS address to create a 22-bit physical address (PA) which is used to reference physical memory. When the UNIBUS map is disabled its operation is transparent to the user and the incoming UNIBUS address is used to reference the first 124K of physical memory.

The figure on the next page shows a block diagram of the UNIBUS map and its associated control logic.

(1) Map Control

The map control logic is used to control the reading and the writing of the 32 map registers and consists of UNIBUS map and boot address decode PLA, a delay line, and associated read/write and buffer control logic. The PLA decodes the UNIBUS address to determine if a read or write of the map registers is intended and asserts the-appropriate signal, MAP WRITE L or MAP READ L. MAP WRITE L and MAP READ L are used to generate MAP R/W L. MAP R/W L is used to accomplish the following during a read or write of the map registers.

a. Assert DISALLOW MEM MSYN. This keeps MSYN, intended for the map registers, from being sent to main memory.
b. Asserts the input of the delay line which is used to generate UBI SSYN L (approximately 120 ns after MAP R/W L is asserted), and MAP SSYN H which is used to negate WRITE MAP L.
c. Assert MAP CE L which is the chip-enabling signal for the map registers.

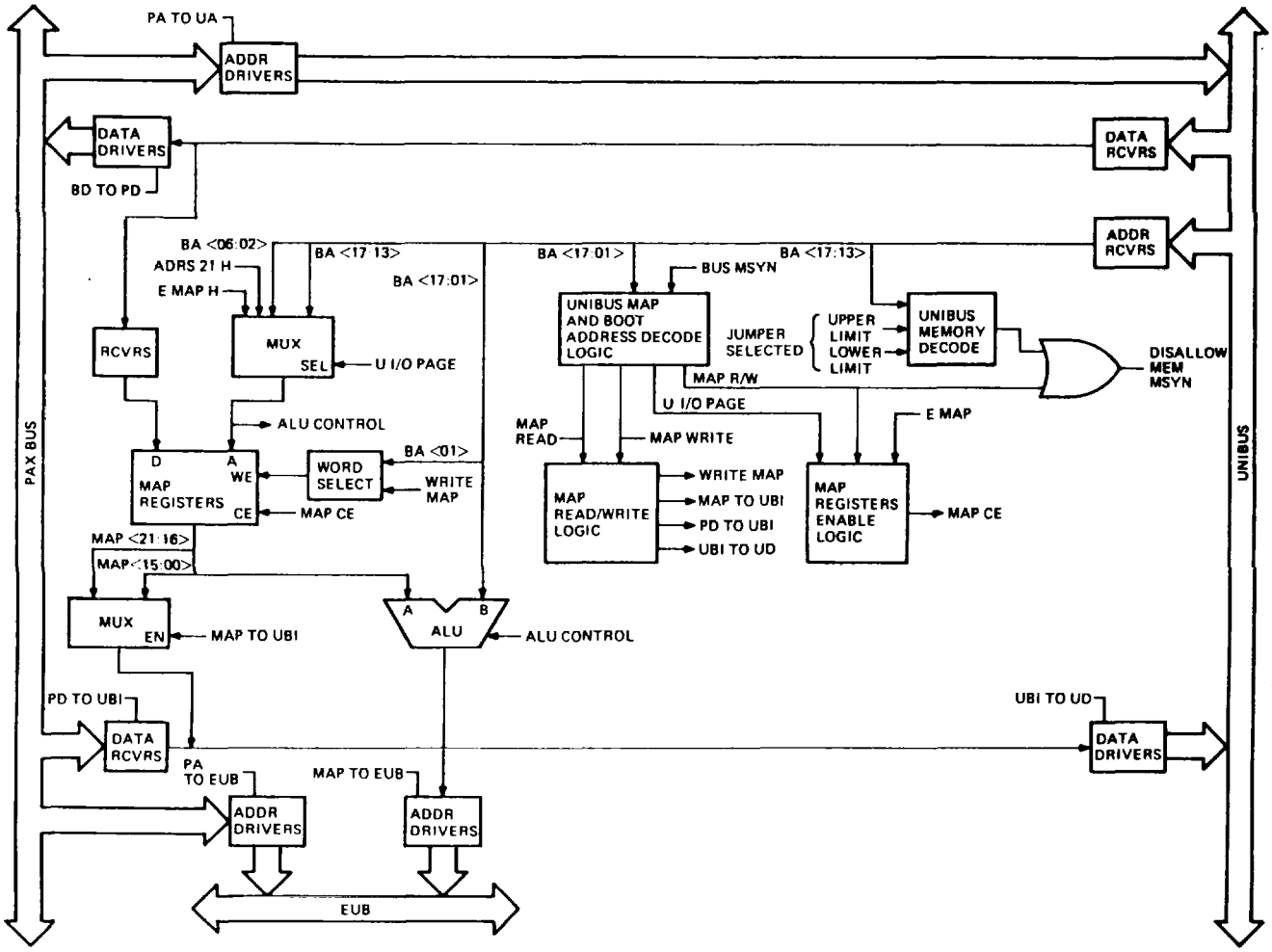
The remainder of the map control logic is used to steer the map output to the proper bus during a read operation. Normally PD TO UBI H and PD TO UBI L are asserted and PAX data is passed directly to the UNIBUS drivers. For a map read operation, these signals are negated and MAP TO UBI L is asserted and causes the output of the map registers to be passed to the UNIBUS drivers. (2) Map Addressing and Relocation Relocation expands the 18-bit UNIBUS address to the 22-bit main memory address. This allows the UNIBUS to access any location in main memory. This relocation or mapping of addresses is done by adding the contents of one of the mapping registers to bits (12:01) of the incoming UNIBUS address.

All mapping registers in the UNIBUS map are 21 bits wide. A 22-bit, which is not writeable and is always read as zero, acts as

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

d. UNIBUS Map (Cont.)

(2) Map Addressing and Relocation (Cont.)



UNIBUS Map Block Diagram

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

d. UNIBUS Map (Cont.)

(2) Map Addressing and Relocation (Cont.)

the lowest-order bit for each register. Each register specifies the 21-bit PA of a 4K page residing on any word boundary in memory. The reason for using word boundaries is that the mapping logic does not know if a byte operation is being executed, and if so, what byte is required.

The figure on the following page illustrates the contruction of a PA by the UNIBUS map. Bits (17:13) of the 18-bit UNIBUS address select a map register. The remaining bits (12:00) of the UNIBUS address are used as an offset into the page to which the mapping register is pointing.

When an address is taken off the UNIBUS, the mapping register is automatically selected and the contents read out. That 21-bit address is added to the 12-bit offset in the UNIBUS address to form the PA. This mapping function is very similar to that performed by memory management.

The program controls this process both by selecting the contents of the mapping registers and by its ability to enable and disable the UNIBUS map relocation function.

The UNIBUS map is enabled by the assertion of E MAP H (bit 5 of SR3). The UNIBUS addresses lines BA (17:00) are received by the map logic. BA 17:13 are selected by the map address multiplexer to generate the address, RAM A 4:0, to the map registers. The output of the selected register, MAP 21:01 H, is sent to the adder, which is made up of ALUs and carry generators, where it is added to BA 12:01 to create MA 21:01. The output of the ALUs, MA 21:01, along with BA 00 and ADRS OUT 21 H, are used to create the PA. These signals are then passed to the memory bus (EUB) via buffers.

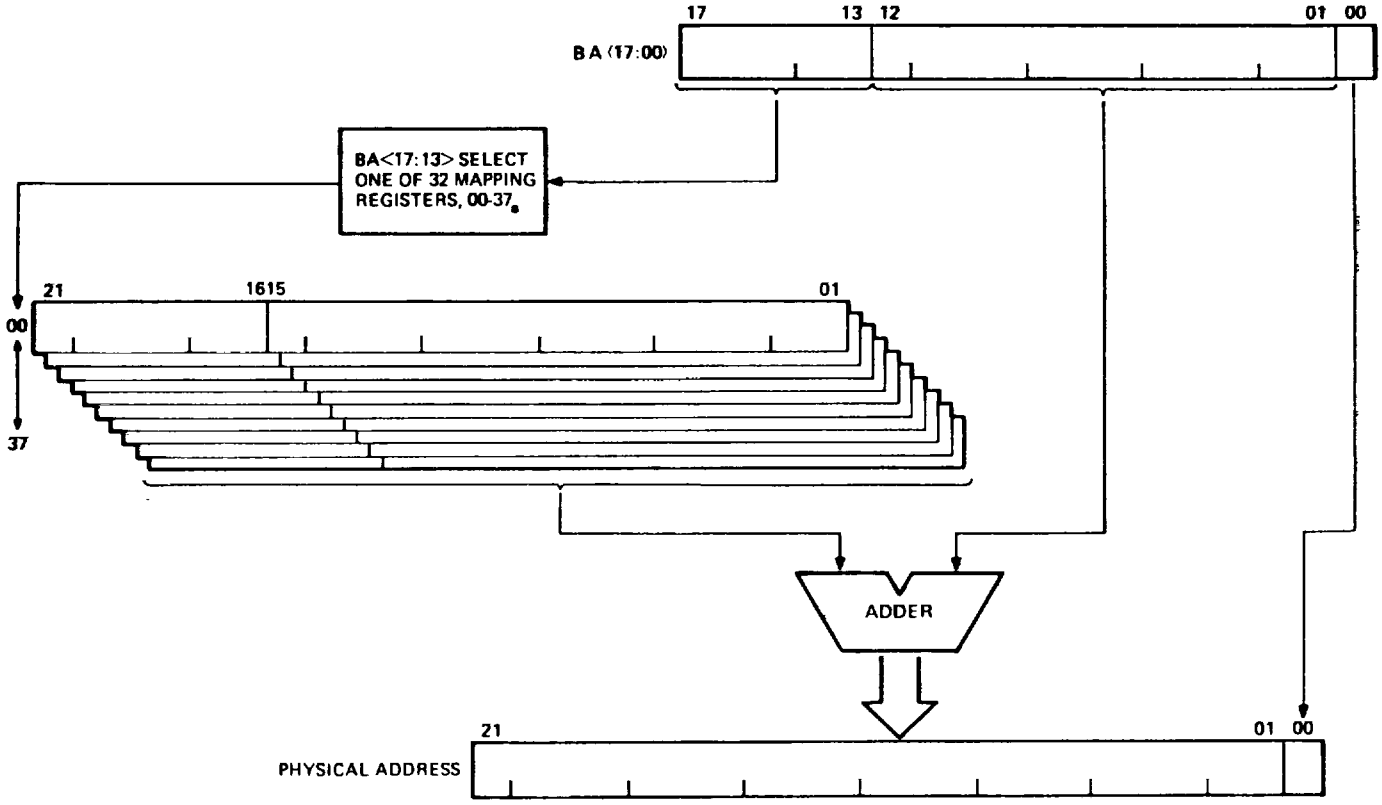
When the UNIBUS map is disabled, bits 21:18 of the PA are set to 0 and BA 17:00 are used for bits 17:00 of the PA. This allows the UNIBUS to access the first 24K of main memory.

When a peripherals page address (17 760 000 - 17 777 777) is decoded by the map, U I/O PAGE L is asserted. U I/O PAGE L being asserted forces bits 21:13 of the PA to be set to ones and BA 12:00 are used for bits 12:00 of the PA. This action forces a reference to the upper 4K of physical memory.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

d. UNIBUS Map (Cont.)

(2) Map Addressing and Relocation (Cont.)



Construction of the PA

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

d. UNIBUS Map (Cont.)

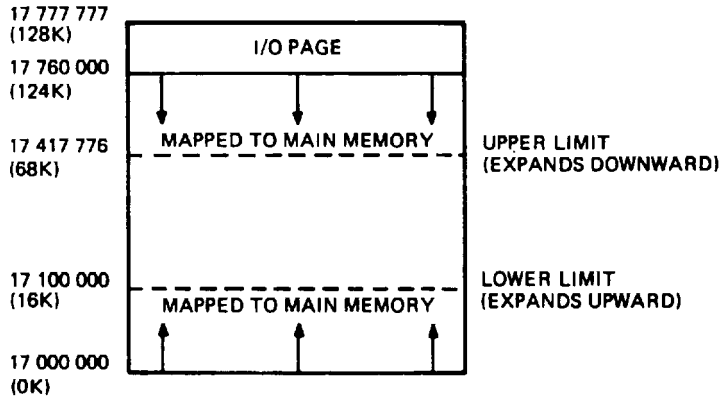
(3) Addressing Limits

There are 31 mapping registers which can be accessed by the UNIBUS for relocation. The actual number is determined by two sets of five jumpers which are used to set the upper limit and the lower limit.

The lower limit jumpers are used to select the first address that will not be mapped to main memory starting at UNIBUS address 0 up to the lower limit. The lower limit allows the UNIBUS space that will be mapped to main memory to be expanded upward from UNIBUS address 0 up to 760 000 in 4K word segments.

The upper limit jumpers are used to select the first address that will not be mapped to main memory starting at UNIBUS address 757 776 down to the upper limit. The upper limit allows the UNIBUS space that will be mapped to main memory to be expanded downward from UNIBUS address 760 000 in 4K word segments.

The figure below shows how the addressing limits affect UNIBUS space. When the upper and lower limits are set to address 0 (OK) or 760 000 (124K) or if the limits overlap (that is, lower limit =400 000 (64K), upper limit = 417 776 (68K)) all of the UNIBUS space, with the exception of the I/O page, will be passed to main memory. UNIBUS Map Addressing Limits



1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

e. Console Processor

The console processor consists of an 8085 microprocessor and associated logic. The console processor, in conjunction with a con- sole terminal, is used to interpret ASCII characters so they can perform the equivalent functions of the " lights and switches" console of earlier processors.

The console terminal (the LA120 or equivalent used for the system console/programmer console) can be operated in one of two modes.

1. Console Mode - the console is used to perform such functions as: start, halt, deposit, examine, continue, etc.The operation of the console is controlled by the 8085 microprocessor.
2. Program I/O Mode - the console functions as the system console and is controlled by the operating system of the CPU.

For an explanation of the console commands refer to TM11-6625-3268-14&P, Appendix H.

The next two pages contain the block diagram of the console processor showing the addressing and data flow.

(1) 8085 Addressing

The 8085 microprocessor, as it is used in this application, when addressing a location will do one of two cycles, a read or a write. The 8085 uses a 16-bit address when referencing its program store, random access memory, or I/O locations. The upper eight bits of the address are direct buffered onto the console-address bus. The lower eight bits, because they are multiplexed with data going to or from the 8085, are latched by E123 (K3-2) and then buffered onto the console address bus. The 8085 controls E123 with the address latch enable (ALE) signal.

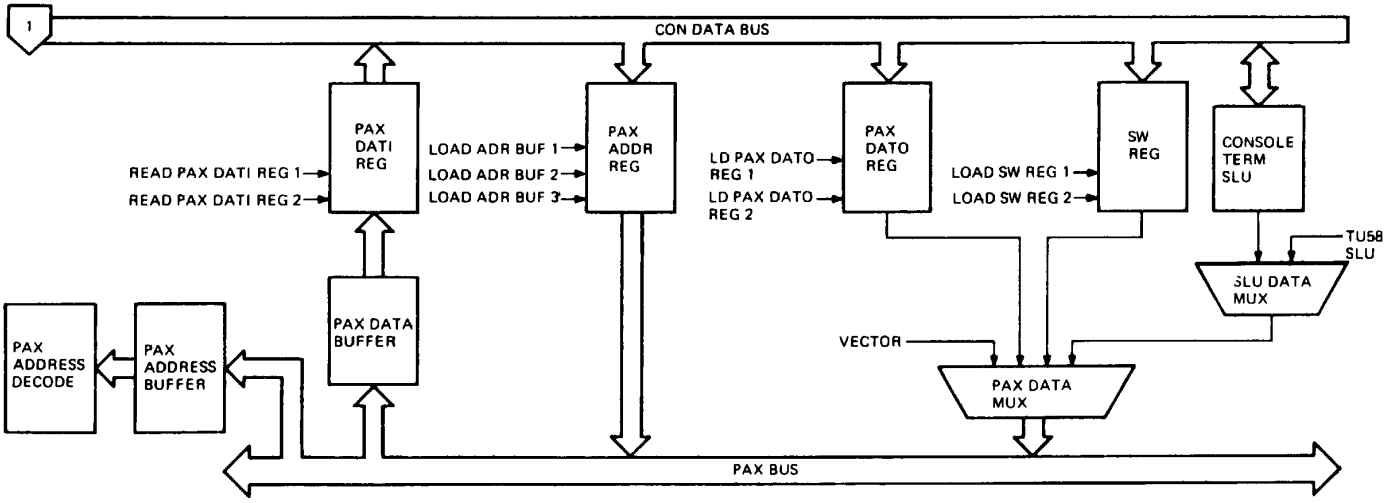
When the 8085 asserts an address, the upper eight address bits and the I/O signal from the 8085 are decoded by the address decode select ROM. The address decode select ROM determines whether a program store, RAM, or I/O address has been asserted. The I/O addresses are further decoded by the I/O address decode logic. The outputs of the I/O address decode logic are used for two different functions: (1) Register load and unload, and (2) Control functions. The control functions are implemented by writing to the I/O address that corresponds to the particular function. There is no transfer of data to or from the 8085. Thus, by the 8085 writing to the correct I/O address, the selected control function is implemented. There are 5 control signals selected by the I/O addresses. All other I/O locations addressed by the 8085 involve either the writing or reading of data to or from the console data bus by the 8085.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

e. Console Processor (Cont.)

Console Processor Block Diagram (Sheet 1 of 2)

e. Console Processor (Cont.)



Console Processor Block Diagram (Sheet 2 of 2)

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

e. Console Processor (Cont.)

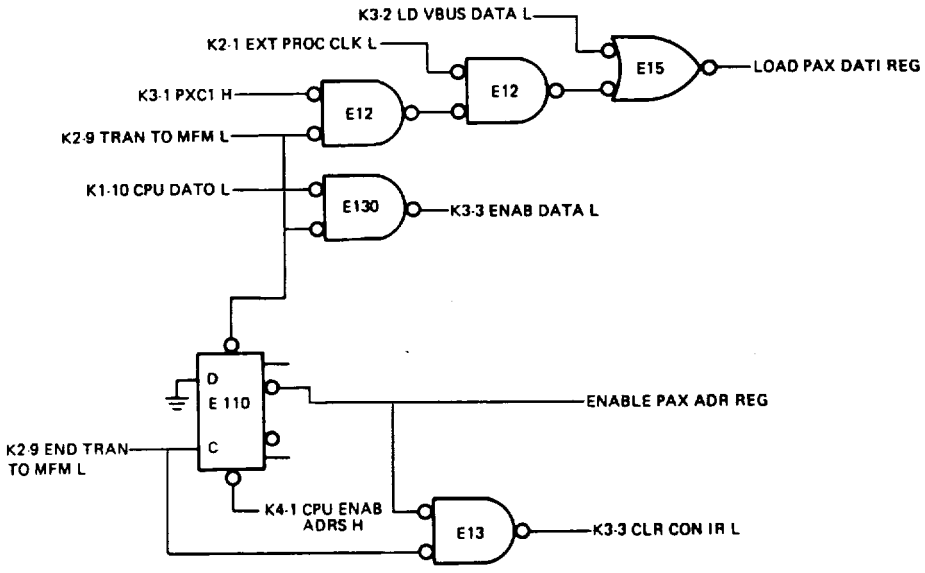
(2) Console Data Flow

The 8085 microprocessor, as it is used in this application, has only two types of I/O cycles: a read for incoming data and a write for outgoing data. The data going to and coming from the 8085 microprocessor is transferred on the console data bus. Because the number of loads on the console data bus are more than the 8085 can drive, it is necessary to buffer the data entering and-leaving the microprocessor via its address/data lines (AD 07:00). The console block diagram shows the buffers and the different loads on the console data bus.

(3) Console-to-PAX Interface

The console-to-PAX interface is the path by which the console processor communicates with the AN/UYK-42(V)4 processor. The PAX bus is the internal data and address bus of the CPU and is the route by which all information going to or from the AN/UYK-42(V)4 CPU must pass. The console-to-PAX interface is made up of buffers, registers, and control logic necessary for the console processor to interface with the PAX bus.

The logic for the console-to-PAX interface is located on K3-3 and K3-4 of the print set. The interface consists of an outgoing 24-bit (22-bit address and 2 control bits) PAX address register, an outgoing 16-bit PAX data register, and an incoming 16-bit PAX data register. The control logic consists of flip-flop Ell0 and gates E12, E13,E15,E130 on K3-3 along with the VBUS and CPU system clock control logic on K3-4.The AN/UYK-42(V)4 data transfer logic is used to handle bus arbitration, timing, and detection of data transfer errors. This eliminates the need to duplicate this logic in the console processor. Console Processor to PAX, Interface Control Logic



1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

e. Console Processor (Cont.)

(3) Console-to-PAX Interface (Cont.)

To understand how the console-to-PAX interface works, an understanding of the various types of deposits and examines, used by the console processor, is needed. (For an explanation of the console commands, refer to TMll1-6625-3268-14&P, Appendix H.) An examine (E) command from the console is executed as follows.

1. Load data out registers with next MPC for MFM data in.
2. Load next MPC register in CPU.
3. Load the outgoing PAX address registers with the address to be examined.
4. Start the CPU clock to do the data transfer.
5. Read PAX DATI register.
6. Check for a transfer error by checking the CPU error register
7. Convert binary data to ASCII and send to console terminal.

A deposit (D) command is similar to an examine command except that a different MPC is loaded into the CPU and the data to be deposited is loaded into the data out registers. A deposit(D) command from the console is executed as follows.

1. Load data out registers with next MPC for MFM data out.
2. Load next MPC register in CPU.
3. Load outgoing PAX address registers with location of where data is to be deposited.
4. Load data out registers with data.
5. Start CPU clock to do data transfer.
6. Check CPU error register for data transfer error.

A more detailed explanation of how an examine and deposit command functions is contained in the following paragraph.

(4) Operation During Command Execution

The operation of the console processor during command execution is a function of the software contained in the console processor's program store. When doing any type of function that requires the transfer of data to or from the console, some of the control for the data transfer is handled by the CPU data transfer logic. During command execution, the console processor controls the manipulation of data within itself, direct communication with the console terminal, control of the CPU clock and the loading of the next MPC, if required.

A detailed explanation of a deposit command (D) best explains how the console processor functions during command execution.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

e. Console Processor (Cont.)

(4) Operation During Command Execution (Cont.)

Deposit 5 into location 1000. This is entered at the console terminal as follows:

D<SP> 1000<SP> 5 <CR>

The carriage return <CR> at the end of the command tells the console processor that the command is complete and execution can start. The console processor first determines that a deposit is to be done and then converts the address and data from ASCII to binary format and stores this information in RAM. After this conversion is done, the command execution begins. First the console processor selects an internal constant which will be used as the next MPC value in the CPU. When doing a deposit this constant designates that an MFM data out is going to be done by the CPU. The console processor then loads this constant into the PAX DATO registers in two write cycles by the 8085 microprocessor. MFM LOAD MPC L(K3-2) is then asserted by the 8085 to put the MPC value on the PAX bus and clock it into the next MPC registers in the CPU. After the MPC is loaded into the CPU, the console processor sets up for the deposit by loading the PAX ADR registers (three write cycles by 8085) with the address where the data is to be deposited and the PAX DATO registers (two write cycles by 8085) with the data. The console processor also asserts FREE BUS H. This signal puts the PAX bus into a high impedance state and prevents any conflicting data from being on the bus when the transfer begins.

When the setup is complete the console processor is ready to let the CPU take control of the data transfer. This is accomplished by the console processor setting the XFER DONE bit and the WAIT bit in the CON IR (K3-4 E90). By setting the WAIT bit, one-shot E35 is triggered and asserts K3-4 WAIT H which triggers one-shot E37 (K3-2) to start the CPU clock by asserting K3-2 CONTINUE L. The CPU now takes control of the transfer; this is done by the control logic on K3-3 (illustration on page 1-63). When the CPU clock starts running, TRAN TO MFM L is asserted and direct sets flip-flop Ell0 as soon as CPU ENAB ADRS H is asserted by the data transfer Logic(K4-1), approximately 60 ns after the clock starts. The PAX address buffers are enabled by Ell0, when it is set, and puts the address on the PAX bus. A short time after CPU ENAB ADRS H is asserted, CPU DATO L is asserted, CPU DATO L is ANDed with TRAN TO MFM L to assert ENAB DATA L. When ENAB DATA L is asserted, the contents of the PAX DATO registers are put on the PAX bus and deposited in the addressed location. When the transfer is complete, TRAN TO MFM L is negated and END TRAN L is asserted. END TRAN L is ANDed with the output of Ell0 to clear the CON IR and then clocks Ell0 to clear the flip-flop. Clearing the CON IR clears the wait one-shot and restarts the 8085. Also, at the end of the transfer, the CPU halts and returns control of the CPU clock to the console processor.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

e. Console Processor (Cont.)

(4) Operation During Command Execution (Cont.)

When the transfer is completed the console processor checks the CPU error register to see if there was a transfer error. If a transfer error has occurred and the transfer is not completed, the console processor does not know until it checks the CPU error register. This is because the WAIT one-shot will timeout and restart the 8085 in 220 ms if the CPU has not asserted END TRAN L before the one-shot times out.

An examine command is similar to a deposit except that there is no data that needs to be loaded into the PAX DATO registers after the MPC constant for an examine has been loaded. Gates E12, E15, and EXT PROC CLK L (illustration on page 1-63) are used to clock the incoming data into the PAX DATI registers. The console processor, after checking for a transfer error, converts the data and address from binary to ASCII and puts the information out on the console terminal. Note that when examining one of the machine registers it is not necessary to load the PAX address registers because the VBUS register (K3-4,E122,E121) is used to select the source registers in the CPU.

For a complete listing of the console commands and their functions refer to TM11-6625-3268-14&P, appendix H.

f. Serial Line Units

The multifunction module (MFM) contains two serial line units (SLUs): a console terminal SLU and a DEC TU58 SLU.

(1) Console Terminal SLU

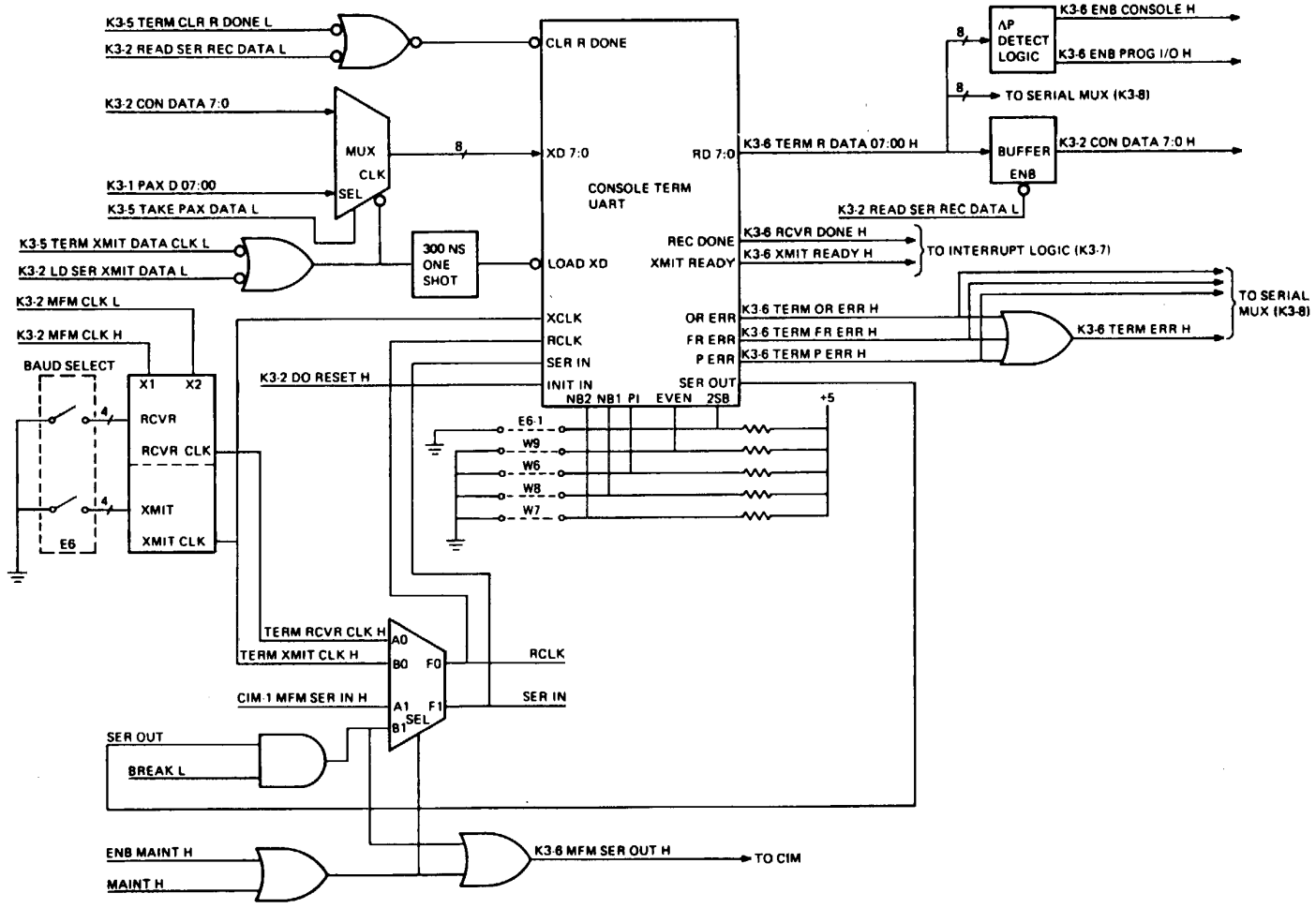
The console terminal SLU (shown on next page) provides the I/O port for an LA36 or LA120 serial terminal or equivalent. The console terminal operates in two modes: as the standard system terminal(program I/O mode) or as a programer's console (console mode).In console mode, the terminal is used in conjunction with the 8085 microprocessor to functionally replace the switch register and light display of earlier traditional control panel. In this mode, all characters input on the terminal are interpreted as commands to the processor control section or as commands to verify and control the console logic.

In either console or program mode, the console terminal SLU enables the transfer of data between the console processor or CPU (parallel data) and the external terminal (serial data). The major functional area of this unit is a universal asynchronous receiver/ transmitter (UART).

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

f. Serial Line Units (Cont.)

(1) Console Terminal SLU (Cont.)



Console Terminal SLU

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

f. Serial Line Units (Cont.)

(1) Console Terminal SLU (Cont.)

a. Transmitter Operation (Terminal UART)

Parallel data to be transmitted from the processor to the terminal is input to the UART transmit data lines (XD 7:0). The source for the transmit data is a multiplexer which selects either the console data bus (K3-2 CON DATA 7:0) or the PAX data bus (K3-1 PX D 07:00). This multiplexer is clocked under two circumstances:

1. when the central processor performs a DATO operation to the terminal transmitter buffer via the PAX data bus (K3-5 TERM XMIT DATA CLK L is generated), or

2. when the console processor writes data to the terminal via the console data bus (K3-2 LD SER XMIT DATA L is-generated).

In both circumstances, the signal that clocks the multiplexer also triggers a 300-ns one-shot which generates the data strobe (K3-6 LD XD L) signal on the UART. The 300-ns one-shot keeps the load signal low for the time period required by the UART transmitter. The parallel-loaded character is converted by the UART to serial data and is output through the SER OUT line of the UART. When the transmitter buffer is emptied, the UART generates the transmit ready line (K3-6 XMIT READY H) indicating a new character can be loaded. The format of the serial character is determined by control inputs to the UART.

The serial character (K3-6 MFM SER OUT H) is transferred from the MFM to the console interface module (CIM) where it can be output to the terminal. The rate at which the character bits are transmitted (baud rate) is switch selectable.

b. Receiver Operation (Terminal UART)

The receiver section of the UART accepts a serial character from the terminal for conversion to parallel data. The receiver samples the serial input line (SER IN) at selected edges of the receiver clock (RCLK).The source of data for the serial input line is a multiplexer. During normal operation, the multiplexer selects serial data from the console interface module (CIM-1 MFM SER IN H). In maintenance mode, the multiplexer selects the SER OUT line of the UART. This enables the closed-loop test of the receiver and transmitter.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

f. Serial Line Units (Cont.)

(1) Console Terminal SLU (Cont.)

b. Receiver Operation (Terminal UART) (Cont.)

The receiver enters the data entry state when it detects a mark-to-space (high to low) transition of the serial input line. If the receiver control logic has been set up to detect parity (jumper W6 IN), the receiver checks the parity of the data bits plus the parity bit following the data bits. The receiver compares the parity of these lines with the parity select line (pin 39 of the UART). If the parity of the received character differs from the parity of the UART control logic, the parity error line (K3-6 TERM P ERR H) is asserted and bit 12 of the terminal receiver buffer register is set.

The receiver samples the first stop bit which occurs after the parity bit or after the data bits if no parity is selected. If the stop-bit or bits are valid, it indicates that the entire character has been received and shifted into the receiver shift register. The receiver then parallel transfers the contents of the shift register into the receiver data holding register, and sets the data available line(K3-6 RCVR DONE H).

If the receiver samples the first stop bit and it is low, this indicates an invalid stop code. The UART will then generate a framing error signal (K3-6 TERM FR ERR H) which sets bit 13 of the terminal receiver buffer register.

In addition to the parity error and framing error conditions, a third error condition (overrun) is associated with receiver operation. The overrun condition indicates that a new character is being loaded into the UART before the previous character has been read. Under these circumstances, the UART generates K3-6 TERM OR ERR H which sets bit 14 of the terminal receiver buffer register.

The serial character received is converted by the UART to parallel data (K3-6 TERM R DATA 07:00). The central processor can read this data by reading the terminal receiver buffer register. The console processor can read the parallel data via the console data bus (K3-2 CON DATA 07:00 H). Also, the character is decoded to determine if it is the console break character (ASCII ^P). If the character is decoded as ^P(0208or 2208), the console terminal enters console mode.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

f. Serial Line Units (Cont.)

(1) Console Terminal SLU (Cont.)

c. Console Terminal Baud Rate Logic

The baud rates for the console terminal receiver and transmitter are derived from a 5.52960 MHz master oscillator and frequency divider circuits. The oscillator drives the internal clock generator of the 8085 microprocessor (K3-2). The clock output of the 8085 is used to generate two timing signals (K3-2 MFM CLK H and K3-2 MFM CLK L) which are used as the clock inputs of the frequency dividers.

The frequency divide circuits have switch-selectable inputs which determine the receiver and terminal clock frequencies and the corresponding baud rate of each. The baud rate ranges from 50 to 19, 200 baud. The frequencies required by the UART are 16 times the desired baud rate.

The clock outputs of the two frequency dividers (K3-6 TERM RCLK H and K3-6 TERM XCLK H) are input to a multiplexer. In the normal mode of operation, K3-6 TERM RCLK H is fed into the receiver clock input of the UART and K3-6 TERM XCLK H is fed into the transmitter clock input. In maintenance mode, the multiplexer is selected so that K3-6 TERM XCLK H is fed into both the receiver and transmitter inputs of the UART, thereby ensuring the same baud rate for both.

(2) DEC TU58 SLU

The TU58 SLU provides the I/O port for the DEC TU58 tape unit. Operation of this serial line unit is very similar to that of the console terminal SLU. Serial data transferred to and from the TU58 is converted to parallel data for the central processor. As in the console terminal SLU, the major functional unit is the UART.

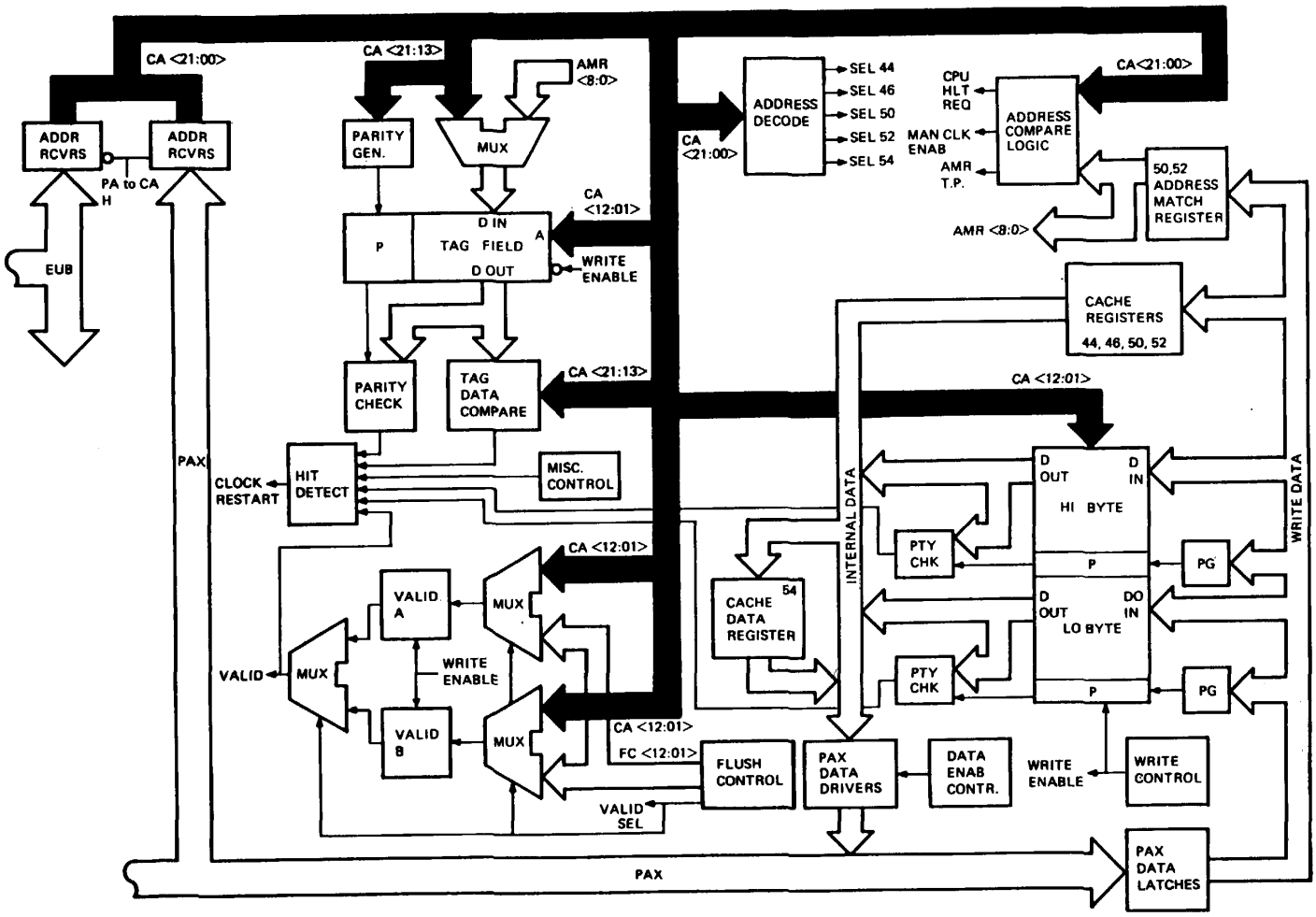
g. CACHE MEMORY

Cache Memory is an integral part of the AN/UYK-42(V)4 processor and is designed to increase the CPU performance by decreasing the CPU-to-memory read access time. It is an 8K-byte high-speed RAM memory organized as a direct-mapped cache with write-through. The figure on the next page shows a block diagram of the AN/UYK-42(V)4 cache.

The AN/UYK-42(V)4 cache operates as an associative memory in parallel with main memory and is connected to the CPU via the PAX

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

g. CACHE MEMORY (Cont.)



Cache Memory Block Diagram

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

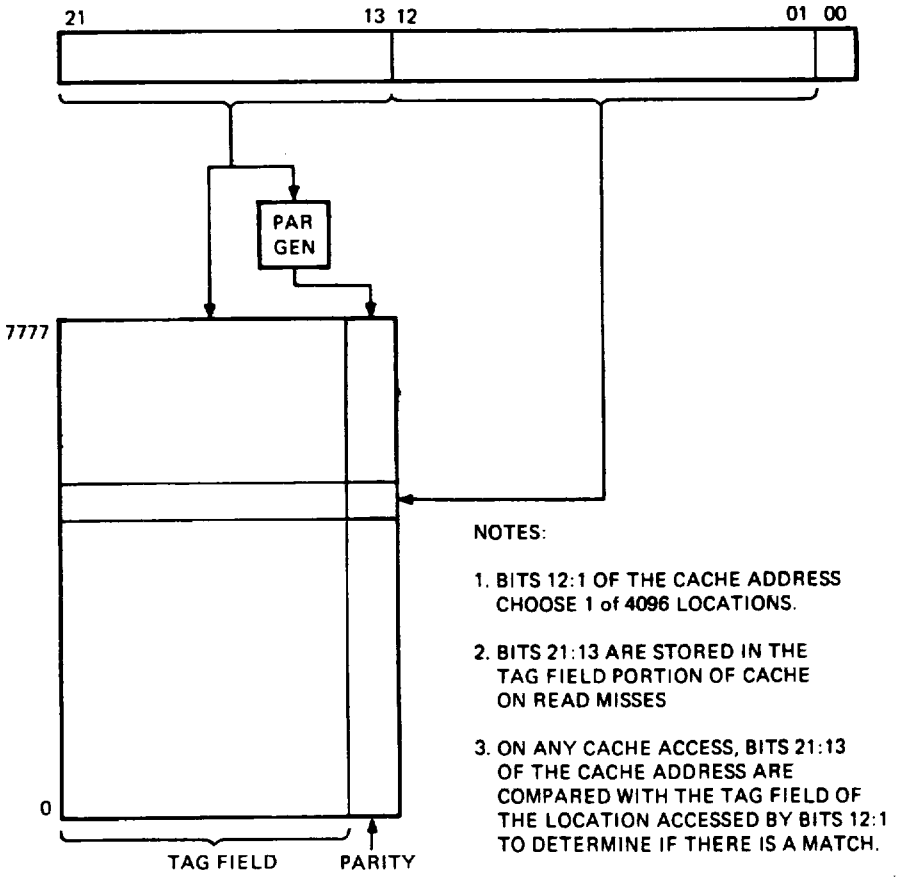
g. CACHE MEMORY (Cont.)

lines. When the CPU is performing a DATI from main memory, the cache memory is first checked to see if it contains the requested data. If the data is in cache memory (a read hit), the data transfer from main memory is discontinued and the data in cache is sent to the CPU via the PAX data lines. If the data is not in cache memory (a read miss), the data transfer is completed, with cache memory performing a write-through to update itself. When the CPU performs a DATO to main memory, the cache updates itself if the addressed location is presently in cache. DMA (direct memory access) and data transfers from the UNIBUS are monitored by the cache and result in the invalidation of cached locations. Only CPU transfers to main memory are cached. Memory located on the UNIBUS will not be cached.

The AN/UYK-42(V)4 cache is an 8K-byte direct-mapping cache with write-through. A direct-mapping cache allows each main memory address only one possible location in cache.

Each address is divided into two fields: the index field and tag field. The index field specifies the cache locations in which the tag and data are stored. The stored tag field is then compared to the tag of the requested word to determine if there is a cache hit.

PAX ADDRESS



Cache Memory Addressing

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

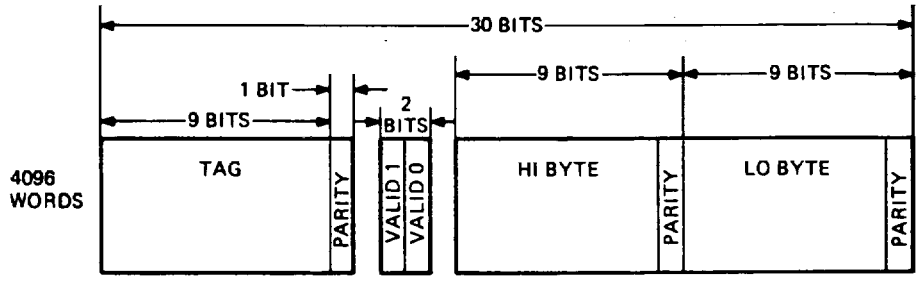
g. CACHE MEMORY (Cont.)

The cache memory consists of 30 4096xl static MOS RAM chips. The organization of these chips is shown below. The cache memory is divided into three basic segments.

TAG Consists of nine tag field bits plus one parity bit.

VALID Consists of two bits; one bit is active while the other bit is cleared. The two bits allow a fast flush of cache by switching to the set of valid bits previously cleared.

DATA Consists of two 8-bit bytes plus a parity bit for each byte.



Cache Memory Organization

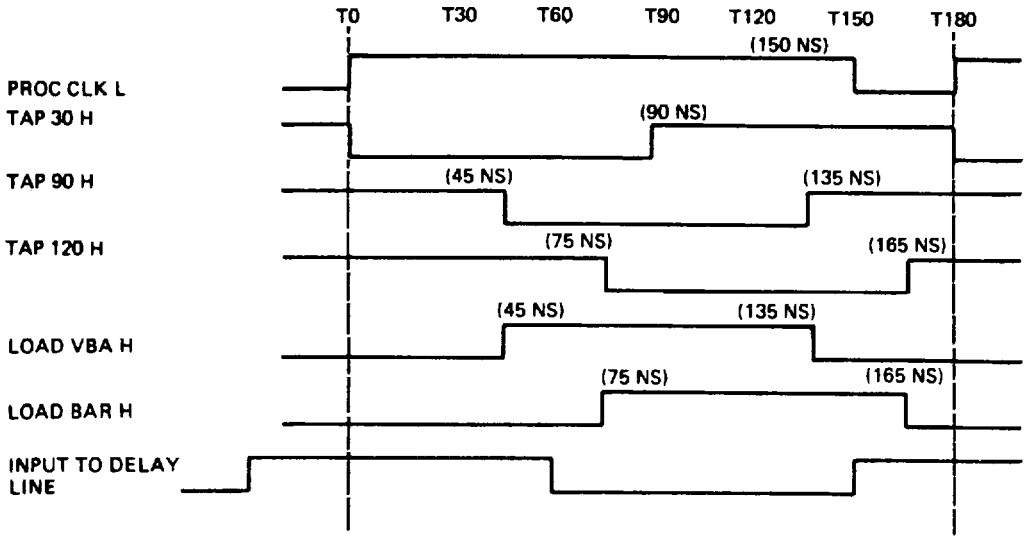
h. SYSTEM CLOCK

The system clock on the AN/UYK-42(V)4 generates all the timing signals to which the processor is synchronized. This allows an orderly execution of the various functions performed by the processor. The clock consists of a delay line and associated logic that is used to create the positive feedback necessary for the clock to sustain oscillation. The various timing signals are taken from the different taps on the delay line.

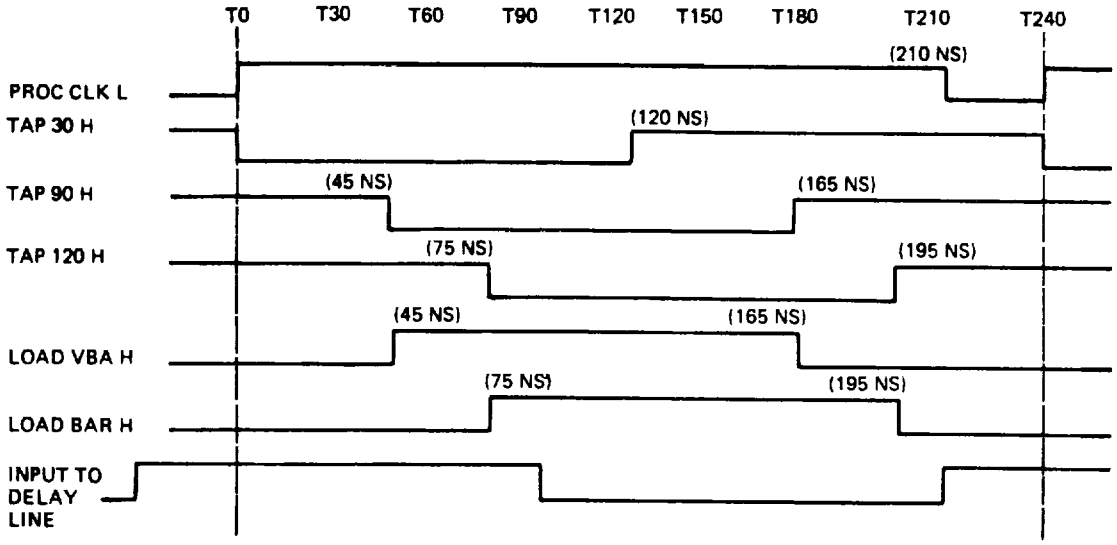
When power is applied to the clock, and if none of the clock disable signals are asserted (K42 INH L, K2-11 INT PROC INIT L, MAN CLK ENAB L), the clock will start running. The length of the operating cycle will be either 180 ns or 240 ns. The normal cycle, or short cycle, for the processor is 180 ns. The 240 ns cycle, or the long cycle, is used when a DATO or DATOB is being performed, or in situations where the condition code must be determined before an operation can be performed. The long cycle is selected by K2-6 LONG CYCLE L being asserted.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

h. SYSTEM CLOCK (Cont.)



System Clock Short Cycle Timing Diagram



System Clock Long Cycle Timing Diagram

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

h. SYSTEM CLOCK (Cont.)

The basic timing signals generated by the clock are shown on the proceeding page in relationship to the delay line input (E3). The rising edge of PROC CLK L is designated as TO because it is at this time that the execution of the next microinstruction begins. The other signals created from these basic signals are the following:

1. EXT CLK A L, EXT CLK B L, EXT CLK CL - These timing signals are logically identical to PROC CLK CL.. These separate signals are sent to the various modules. These signals are used so that loading will be equalized and edge skews minimized.

2. PROC CLK H - is the inverse of PROC CLK'L.

3. EXT TAP 30 H - is identical to TAP 30 H.

4. EXT TAP 90 L - is the inverse of TAP 90 H.

5. ALLOW MSYN H - is generated by the ANDing of TAP 30 H, TAP 90 H, TAP 120 H or by RELOCATE H not being asserted. This signal delays the memory cycle until the PAX ADRS is loaded during a DATI or DATIP operation.

The clock may be stopped by asserting one of three signals:

1. MAN CLK ENABL - This signal disables the clock and allows it to be manually stepped by the assertion of MAN CLK L. Any TTL-compatible waveform may be used to single-step the clock.

2. INT PROC INIT L - This signal will stop the clock when asserted.

3. INH L - This signal stops the clock when asserted. This signal indicates a bus cycle is in progress and can be overridden by CACHE RESTART L which restarts the clock.

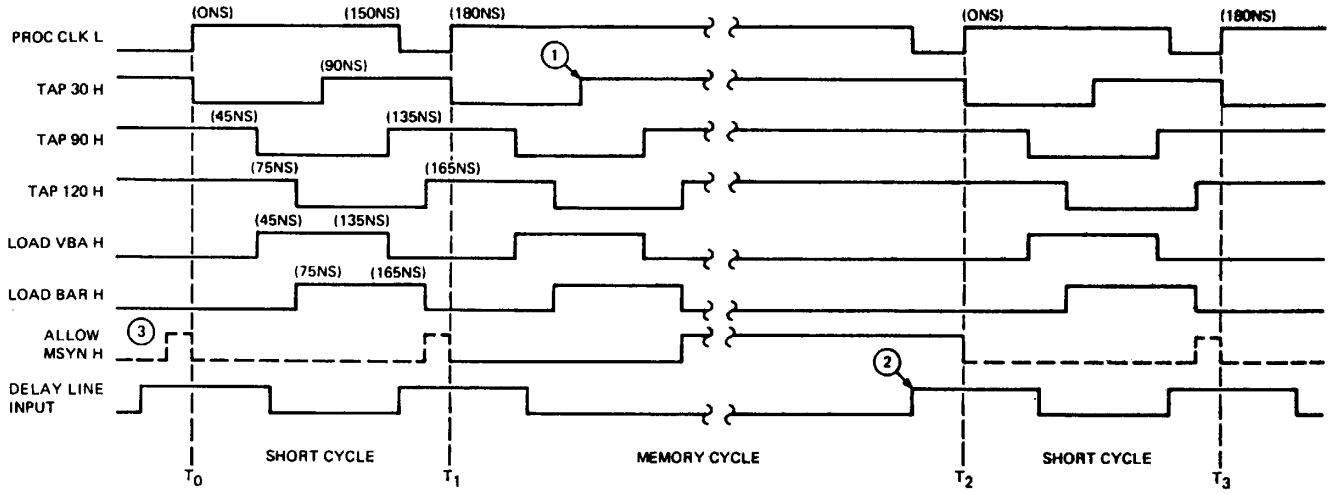
The figure on the next page shows a memory cycle in which the system clock is stopped.

The system clock is turned off by the appropriate signal under the following conditions:

1. During a BUS INIT that is not caused by a RESET.
2. During the INIT portion of the power-up routine.
3. During the INIT portion of the power-down routine.
4. During a RESET.
5. During a BUT service arbitration delay.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

h. SYSTEM CLOCK (Cont.)



NOTES:
1. CLOCK INHIBITED
2. CLOCK RESTARTED
3. IF THE MEMORY CYCLE IS A NON-RELOCATED CYCLE ALLOW MSYN H IS ALWAYS ASSERTED.

System Clock Timing Diagram 'with Memory Cycle

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

h. SYSTEM CLOCK (Cont.)

6. During a priority interrupt.
7. While BUS SACK is asserted by an interrupting device(not for NPRs)
8. During bus data transfers.
9. After a HALT instruction is executed.
10. When the console processor generates a clock inhibit signal.
11. When the manual clock is enabled.

i. POWER FAIL/AUTO RESTART

The AN/UYK-42(V)4 power fail/auto restart circuitry (K2-2) serves the following purposes.

1. Initializes the microprogram, the UNIBUS control, and the UNIBUS to a known state immediately after power is applied to the computer.

2. Notifies the microprogram of an impending power failure.

3. Prevents the processor from responding to an impending power failure for 2 ms after initial startup.

The actual power fail/auto restart sequences are microprogram routines. The operation of the power fail/auto restart circuitry depends on the proper sequencing of two bus signals: AC LO and DC LO. Because of the electrical properties of the UNIBUS drivers and receivers, the entire computer system must be powered up for the machine to operate. Therefore, the processor is notified of a power failure in peripherals, as well as in its own ac source.

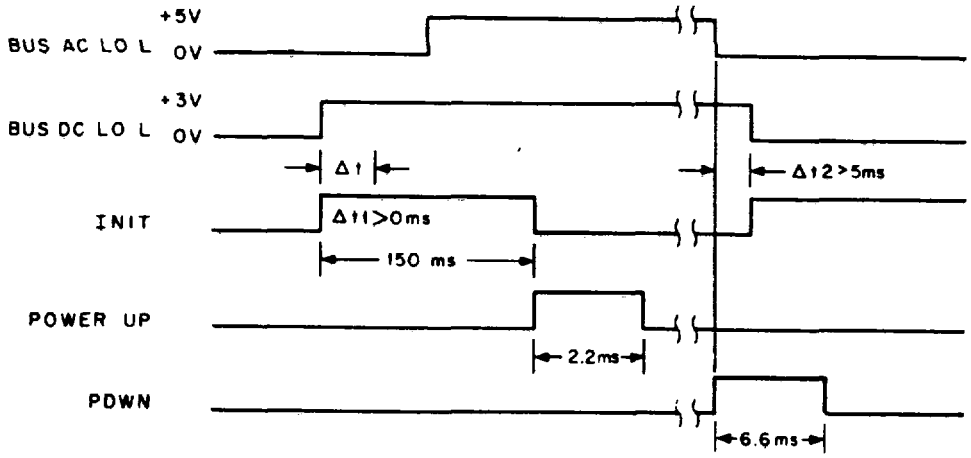
The notification of power status of any AN/UYK-42(V)4 system component is transmitted from each device by the signals BUS AC LO L and BUS DC LO L(K2-2). The power-up sequence (shown on the next page) shows that BUS DC LO L is unasserted before BUS AC LO L is unasserted. When BUS DC LO L is not asserted, it is assumed that the power in every component of the system is sufficient to operate. When BUS AC LO L is not asserted, there is sufficient stored energy in the regulator capacitors of the power supply to operate the computer for 5 ms, should power be shut down immediately.

As ac power is removed, BUS AC LO L is asserted by the power supply, warning the processor of an impending power failure. When BUS DC is asserted, it must be assumed that the computer system can no longer operate predictably. Memories manufactured by DEC use BUS DC LO L as a switched signal, turning them off even if power is still

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

i. POWER FAIL/AUTO RESTART (Cont.)

available. Time at2 (shown below) is the time delay between the assertion of BUS AC LO L and the assertion of BUS DC LO L; this time delay must be greater than 5 ms. This allows for power to be rapidly cycled on and off. According to PDP-11 specifications, on system start up, a minimum of 2 ms run time is guaranteed before a power fail trap occurs, even if the line power is removed simultaneous with the beginning of the power-up sequence. After the power fail trap occurs, a minimum of 2 ms run time is guaranteed before the system shuts down. Given the tolerance permitted in the timing circuitry used in most equipment, At2 must be greater than 5 ms.



BUS AC LO and BUS DC LO Timing Diagram

When a pending power fail is sensed, a program trap occurs, causing the present contents of the PC(R7) and the PSW to be pushed onto the memory stack, as determined by the contents of R6(stack pointer register). The PSW is then loaded with the contents of location 268and R7 with the contents of 248. Processing is continued with the new R7 and PSW. The user's program must prepare for the impending power failure by storing away volatile registers and reloading location 248and 268with a power-up vector. This vector points to the beginning of a restart routine.

When power is restored, the processor loads the PC(R7) with the contents of location 248and the PSW with the contents of location 268. After loading these registers, the user's program presumably will prepare locations 248and 268for another power failure. If HLT 1-78 RQST L input is asserted by an external switch closure, the processor powers up through locations 248and 268and halts.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE

Execution of each AN/UYK-42(V)4 instruction requires the performance of a sequence of operations. The sequence is controlled by the microprogram contained in the PROM control store. The central processor control store provides storage for 1K of 56-bit microinstructions. Every microinstruction comprises 23 fields which control particular functions in the processor. The chart on the next two pages illustrates the format of the central processor microinstruction and the significance of each field value.

(1) MicroPC Generation

The address of the current microinstruction(microPC) can be generated from a number of sources. Refer to the illustration on page 1-83. The two major sources of the microPC lines (K2-6 MPC 10:00 H) are the central processor and the console processor. The signals from the central processor and console processor are wire ORed but only one group of signals is enabled at any particular time.

The console processor can generate a particular microPC by writing the address onto the PAX data bus and generating K3-2 MFM LOAD MPC L. This signal clocks the PAX data bits into a flip-flop and enables that data onto the MPC lines (K2-6 MPC 10:OOH). In addition, the console processor can read the current microPC via the PAX data bus by generating K3-4 FORCE CPU MPC L.

Under normal conditions, the central processor generates the address of the microinstruction. The signal K3-2 MFM LOAD MPC L is false and the CPU MPC line drivers are enabled by the signal K2-9 ENAB CPU MPC L. The next address field (CS 00:10) of the current. microinstruction will specify the microPC. Control store bits 00:10 generate MPC bits 10:00, respectively. However, several signals are wire ORed with the MPC lines to enable branching at specific points within the microprogram. Branches are enabled in the following situations:

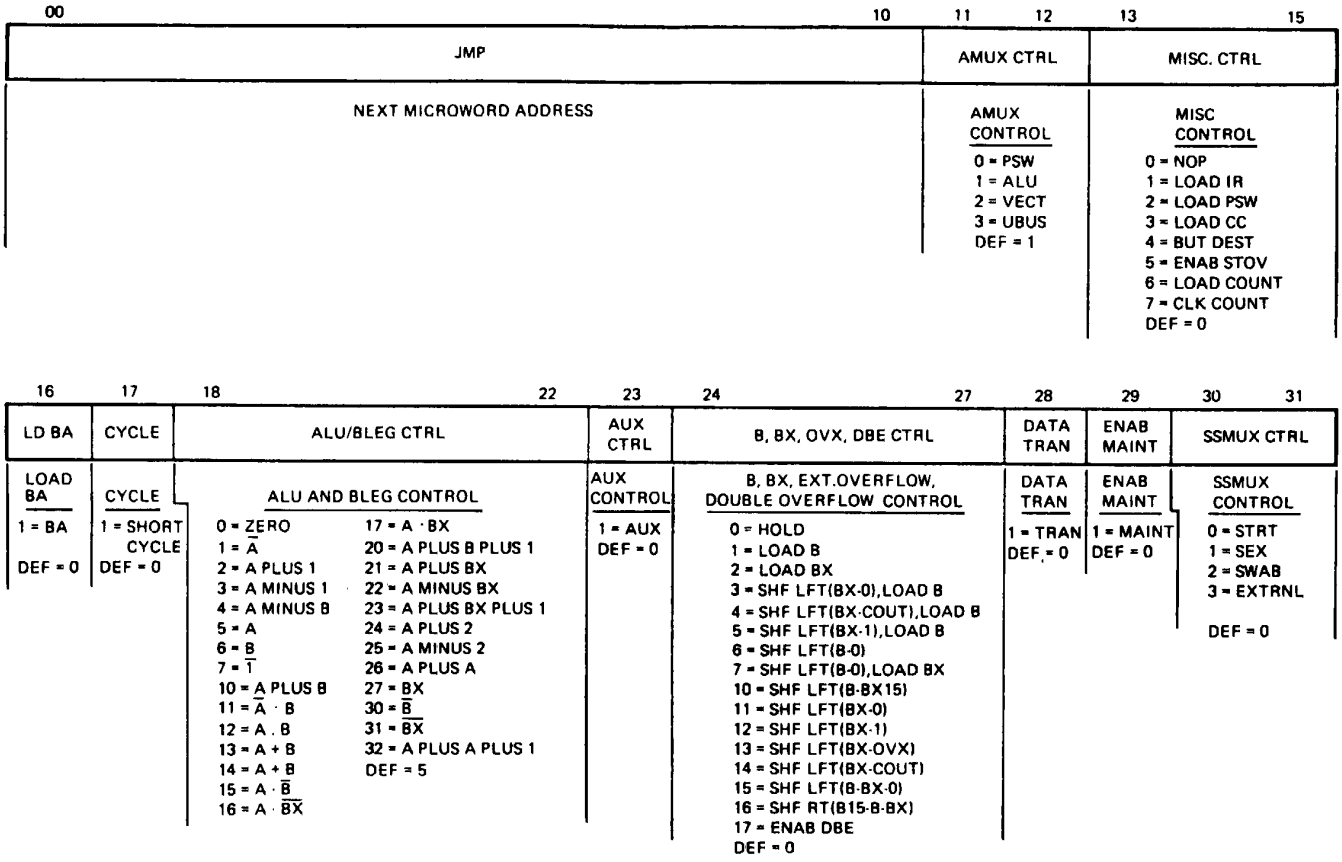
Branch on Micro Test The BUT ENABLE field of the microinstruction (CS 36: 39) selects certain signals or groups of signals to be ORed with MPC bits 07: 00. The microPC will be altered to reflect the status of those signal lines being tested.

Instruction Decode The instruction decode logic generates signals which are wire ORed with MPC bits 07: 00. When enabled, the instruction decode logic can cause branching within the microprogram. The microbranch address will depend on the instruction, mode, and operands specified.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE (Cont.)

(1) MicroPC Generation (Cont.)



Microinstruction Format (Sheet 1of 2)

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE (Cont.)

(1) MicroPC Generation (Cont.)

32 33	34 35	36 39	40	41	42	43	44 45	46	47
BUS CTRL	SPA DST SEL	BUT ENAB	RS + 1	PREV MODE	BUT SERV	FORCE KER	SRI CTRL	ID	NOT USED
UNIBUS CONTROL 0 = DATI 1 = DATIP 2 = DATO 3 = DATOB DEF = 0	SPA DST SELECT 0 = RBA 1 = RS 2 = RD 3 = ROM	BUT ENABLE 0 = NOP 1 = NBIT 2 = ZBIT 3 = C05 4 = BOOT 5 = BX00 6 = BX01 7 = COUT 10 = NOSERV 11 = NBIT, ZBIT 12 = BX00, NBIT 14 = C05, BX01, BX00 15 = ALL 16 = BX00, C05	SRC REG OR 1 0 = RS + 1 DEF = 1	PREV MODE 0 = PREV MODE DEF = 1	BUT SERV 1 = SERV	FORCE KER 1 = FORCE KERNEL DEF = 0	SRI CONTROL 0 = NOP 1 = SRI LOW 2 = SRI HI 3 = ZERO SRI	ID SPACE 0 = I 1 = D	NOT USED

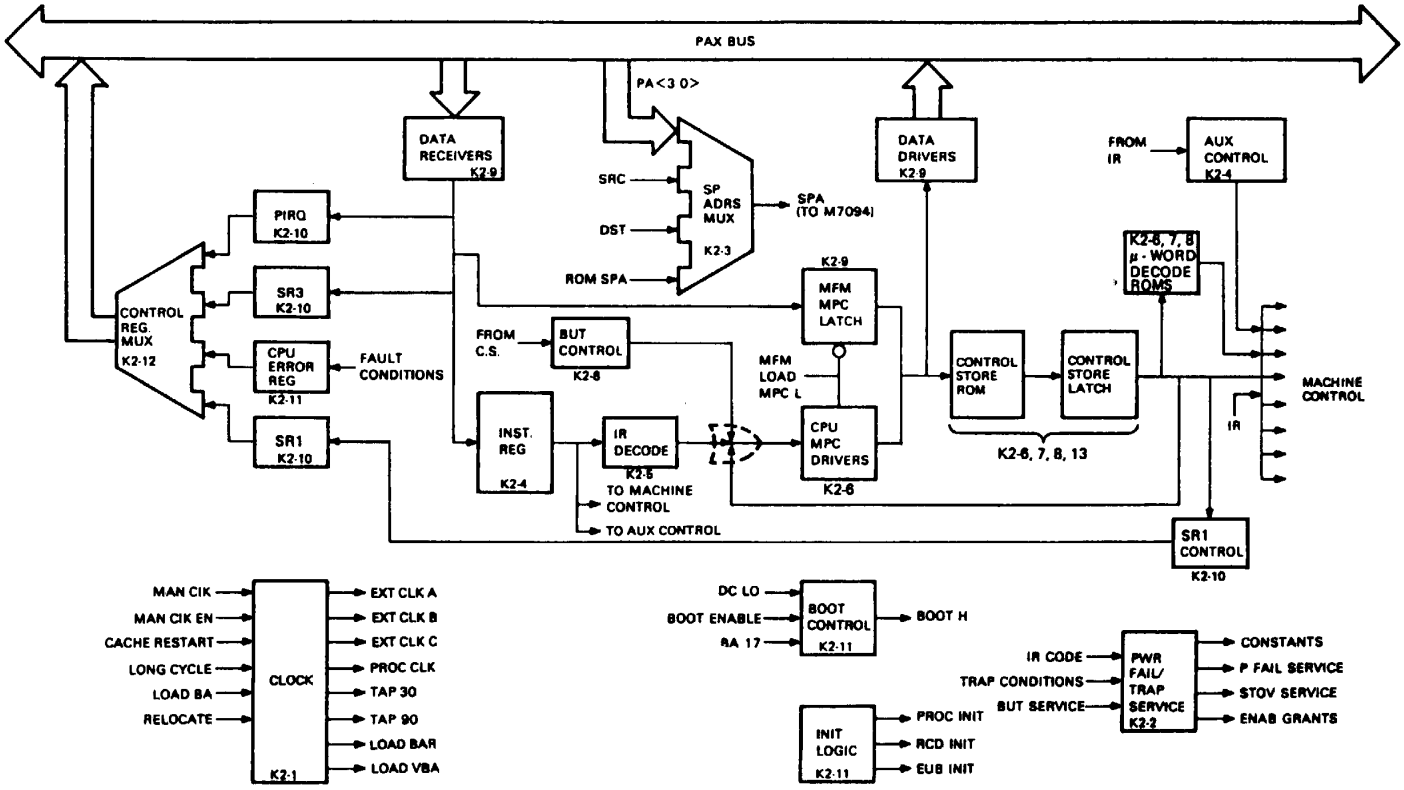
48 51	52 53	54 55
ROM SPA	SPA SRC SEL	SO SI CTRL
ROM SCRATCH PAD ADDRESS 0 = R0 1 = R1 2 = R2 3 = R3 4 = R4 5 = R5 6 = R6 (SP) 7 = R7 (PC) 10 = R10 11 = R11 12 = R12 13 = R13 14 = R14 15 = R15 16 = R16 17 = R17	SPA SRC SELECT 0 = RBA 1 = RD 2 = RS 3 = ROM	CONSTANT CONTROL 0 = K0 1 = K16 2 = K26 3 = K366

Microinstruction Format (Sheet 2 of 2)

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE (Cont.)

- (1) MicroPC Generation (Cont.)

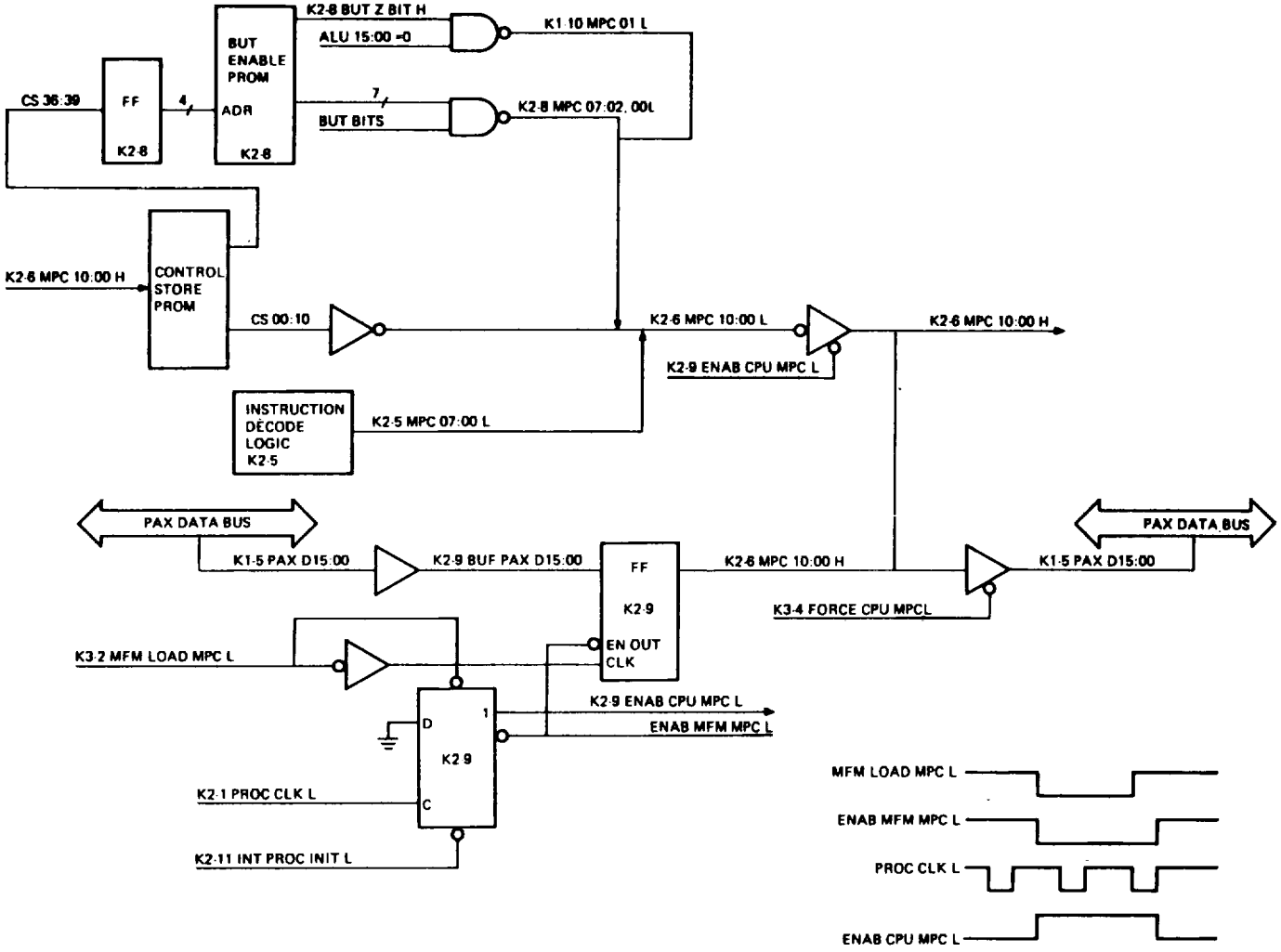


Control Block Diagram

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE (Cont.)

(1) MicroPC Generation (Cont.)

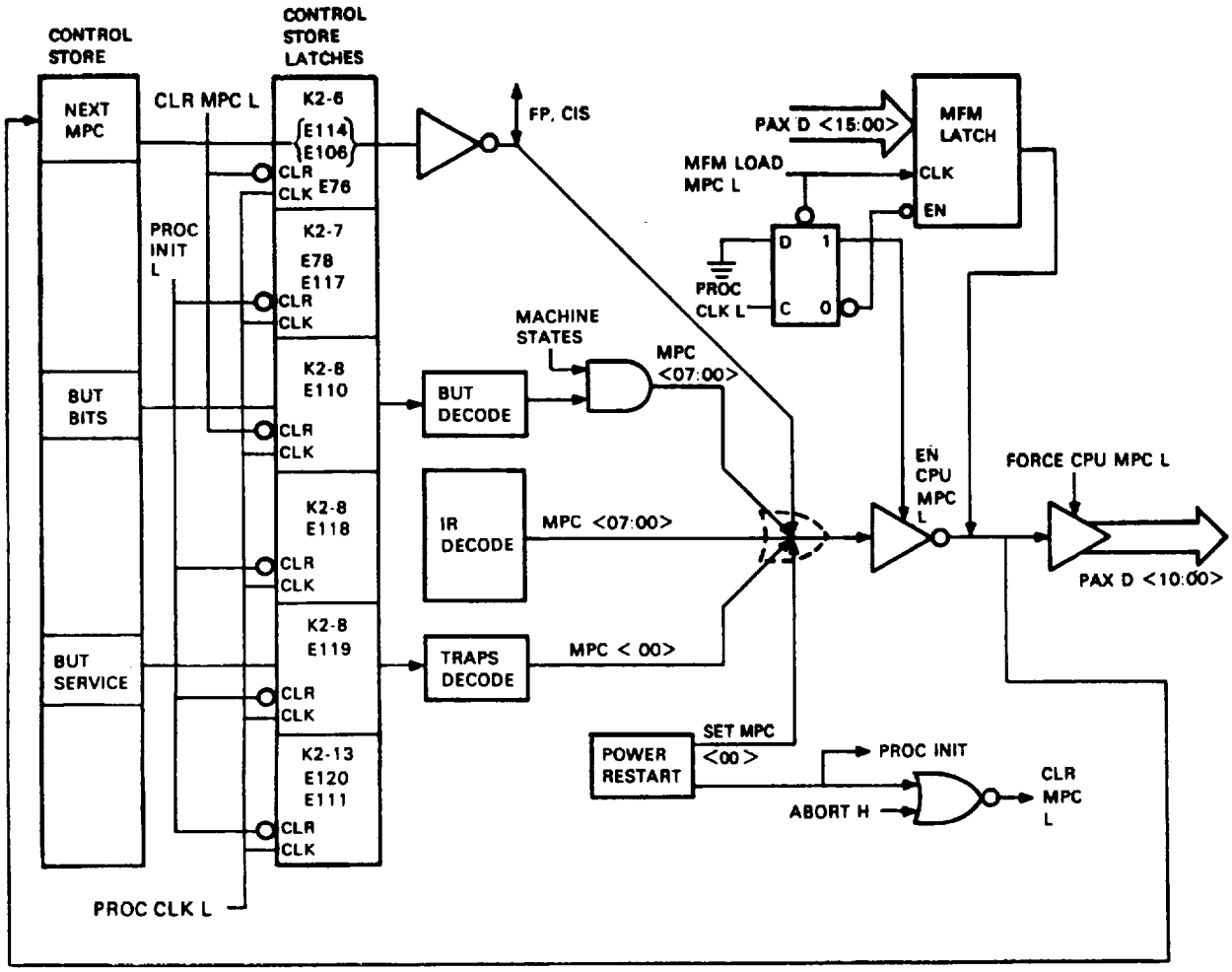


MicroPC Generation

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE (Cont.)

(1) MicroPC Generation (Cont.)



Next MPC Generation

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

j. CONTROL STORE (Cont.)

(1) MicroPC Generation (Cont.)

Power Restart Power restart will force the MPC lines to be cleared by an initialize signal (K2-11 PROC INIT H). The power up circuit (K2-2) will then enable MPC bit 00, forcing the processor to perform the power up routine beginning at microprogram address 001.

Trap Decode The processor enters the service microstate when CS bit 42 is enabled (K2-8 BUT SERVICE 1 (H) is generated).The service logic (K2-2)can then monitor various trap conditions and enable MPC bit 00. This causes a branch to a microroutine which initiates an error macroroutine. The error routine pushes and pops the PC and PSW on or off the processor stack.

k. DATA PATH

The data path (illustration next page) provides the logic required for arithmetic and logic processing (AIU), shifting of 8, 16, and 32-bit data formats (ALU B-leg logic), byte swapping and sign extension of data (SSMUX), storage of general register data (scratch pad memory), and storage of status information (processor status word). The following paragraphs describe each major element of the data path.

(1) Arithmetic Logic Unit (ALU)

The ALU (figure page 1-87) is the main processing element of the data path. It performs arithmetic (with full carry look-ahead) or logic operations on 16-bit operands. The ALU is physically divided into four 4-bit slices (Kl-l through KR1-4). Operations performed by the ALU are specified by the ALU/BLEG CTRL field (CS 18:22) of the current microinstruction or by the auxiliary control logic.

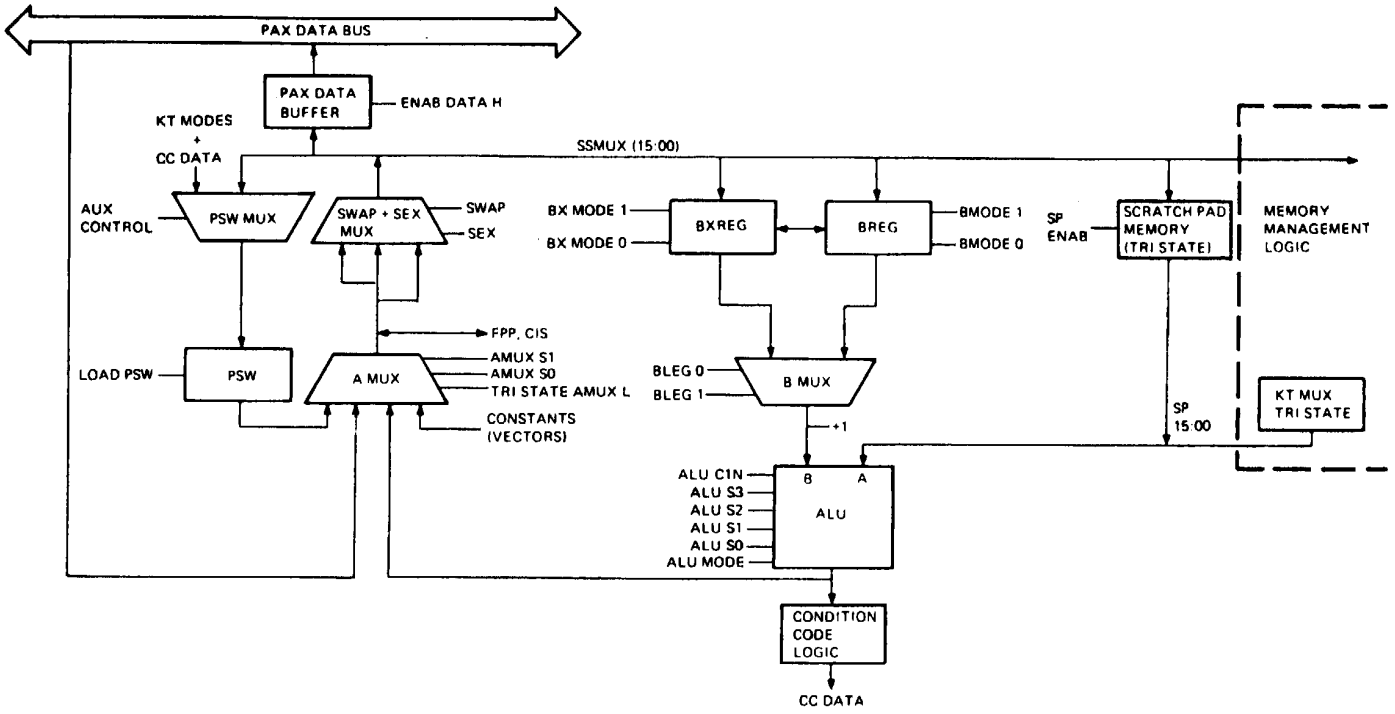
When bit 23 of the microinstruction equals 1, the signal K2-7 AUX CONTROL(1) H is generated and the auxiliary ALU control PROMs(K2-4) are enabled. The ALU operation will then be a direct function of the current AN/UYK-42(V)4 instruction being executed. If the auxiliary control bit (CS 23) is not set, the ALU function is defined explicitly by CS 18:22, as shown on page 1-80.

The data sources for the A input of the ALU are the scratch pad memory and KT multiplexer(KT MUX). These sources are wire ORed to generate the signals SP 15:00(1)H. The internal address decode logic (Kl-10) generates Kl-10 ENAB KT MUX L which enables the KT MUX and disables the scratch pad memory. The KT MUX and scratch pad are thereby prevented from driving the SP lines at the same time. The data source for the B input of the ALU is the B-leg multiplexer (BMUX). The BMUX can select the BX register, B register, +1, or zero.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(1) Arithmetic Logic Unit (ALU) (Cont.)

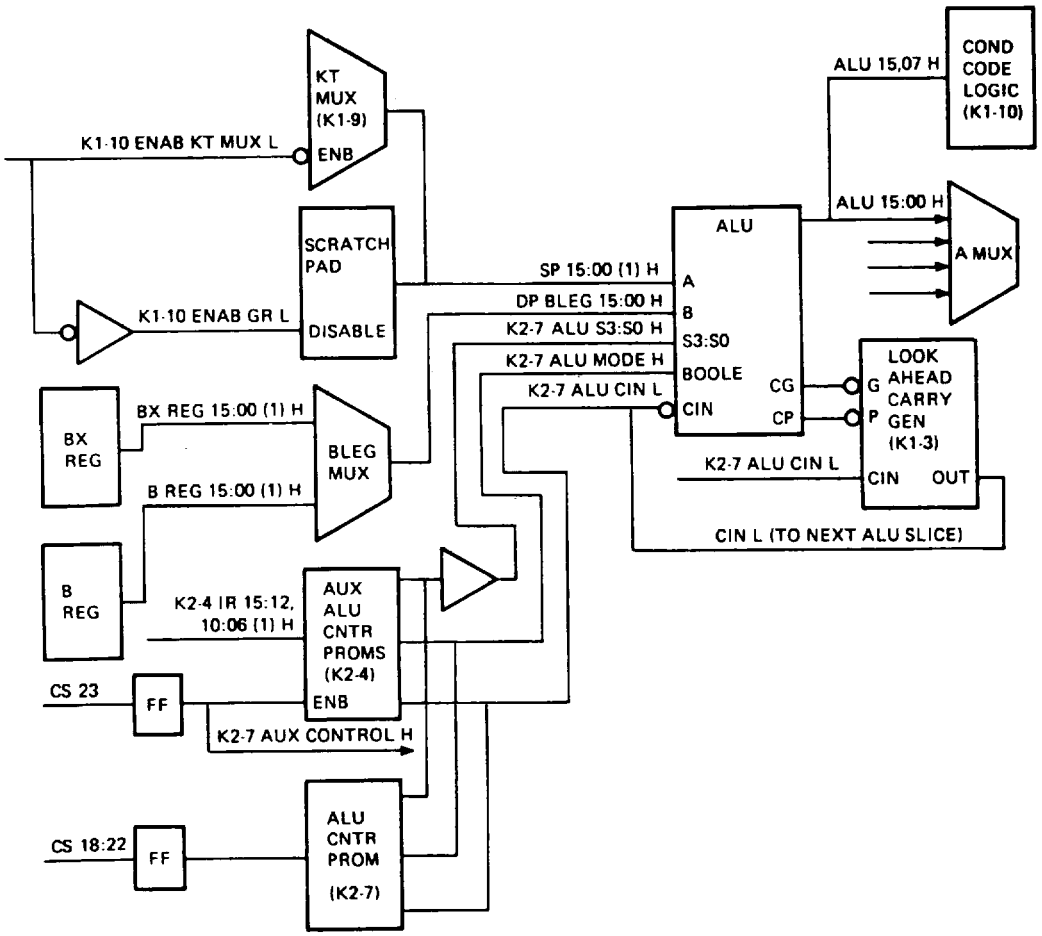


Data Path Block Diagram

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(1) Arithmetic Logic Unit (ALU) (Cont.)



Arithmetic Logic Unit

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.) W

(1) Arithmetic Logic Unit (ALU) (Cont.)

The data outputs of the ALU (ALU 15:00 H) are input to one leg of the ALU multiplexer (AMUX) and the condition code logic (KI-10). The generate and propagate outputs of each ALU slice are input to the look ahead carry generator. This circuit enables the carry to be anticipated across the four ALU slices.

(2) ALU B-Leg Logic

The B leg of the ALU shown on the next page consists of three components: the B-leg multiplexer(BMUX), the B register(B REG) and the BX register(BX REG). Each of these components is divided into four 4-bit slices(Kl-l through K1-4).

The BMUX selects the data source for the B input of the ALU. The BMUX can select the B REG, BX REG, or the constants 1 and 0, depending on the value of the BMUX control lines, as follows:

K2-7 BLEG 01 H	**K2-7 BLEG 00 H**	**BMUX OUTPUT (DP BLEG 15:00 H)**
0	0	BREG 15:00(1)H
0	1	BXREG 15:00(1)H
1	0	0
1	1	DP BLEG 15:01 = 0, DP BLEG 00 - K2-3 PLUS ONE H

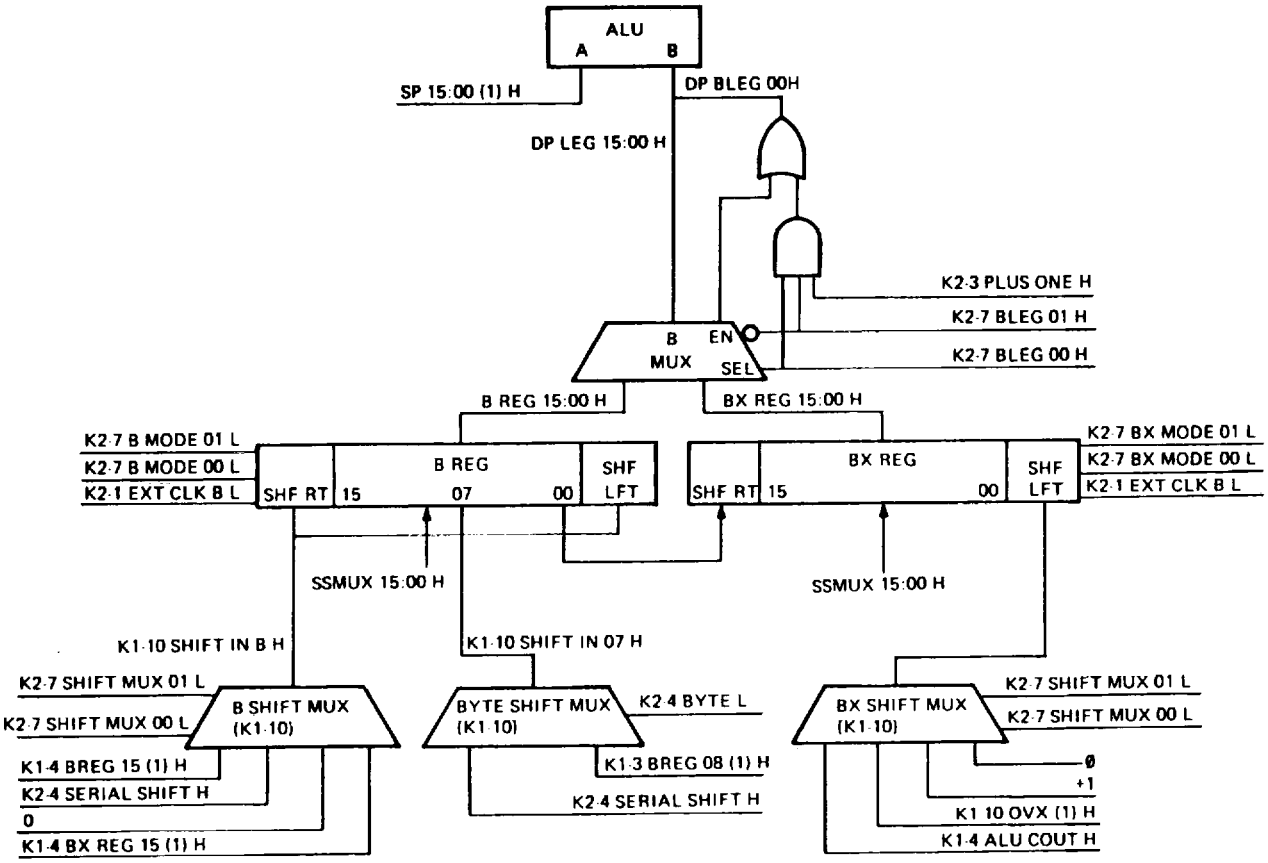
The constants 1 and 0 are generated during autodecrement and autodecrement operations. During either operation, if a word instruction is being performed, the specified register is incremented or decremented by two; if a byte operation is being performed, the register is incremented or decremented by one.

The ALU uses the signal K2-8 ALU CIN L to increment or decrement the A-leg input by one. The B-leg input must provide the constant 1 or 0 to obtain the correct autoincrement or autodecrement result. The constant 0 is generated by disabling the BMUX output. The constant 1 is generated by disabling the BMX output and O Ring BMUX bit 0 with the signal K2-3 PLUS ONE H. This signal is true when the specified register are to be incremented or decremented by two.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(2) ALU B-Leg Logic (Cont.)



ALU B-Leg Logic

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(2) ALU B-Leg Logic (Cont.)

The B REG and BX REG are 16-bit general purpose registers that can be shifted right or left by a single bit. Both registers can ' also be parallel loaded with data from the swap sign extend multiplexer(SSMUX). The BREG and BXREG have separate pairs of mode control lines (Figure previous page), but they perform the same functions, as follows:

Mode 01	Mode 00		Function
L	L	Hold	Contents of register do not change.
L	H	Shift Right	Contents are shifted right one bit.
H	L	Shift Left	Contents are shifted left one bit.
H	H	Parallel Load	Data from SSMUX is loaded into the register and appears at its output.

Each register can be shifted as a 16-bit word or the registers can be combined and shifted as a 32-bit word. When the B REG and BX REG are used in conjunction, the B REG represents the upper 16 bits. The B REG can also be shifted as an 8-bit byte. The signal Kl-10 SHIFT IN B H is fed into both serial shift inputs (SHF RT and SHF LFT) of the B REG. This signal is generated by the B SHIFT multiplexer. The B SHIFT MUX can select B REG bit 15, BX REG bit 15, 0, or K2-4 SERIAL SHIFT H as the serial input for either a right or left shift, To allow the byte shift function of the B REG, bit 07 of the B REG is loaded with the signal Kl-10 SHIFT IN 07 H (generated by the BYTE SHIFT multiplexer. During a byte operation, the BYTE SHIFT MUX selects K2-4 SERIAL SHIFT H to be directly input into bit 07 of the B REG. During a word instruction, the signal K1-3 B REG 08 (1) H is input to bit 07.

As previously mentioned, the BX register can also be shifted to the right or left. During a shift right, the BX register contents are moved one place toward the least significant position and BX REG bit 15 is loaded with B REG bit 00. Thus, for all right shifts, the BX REG represents the low-order 16 bits of a 32-bit word. During a shift left, the register contents are shifted toward the most significant bit position and BX REG bit 00 is loaded with the signal Kl-10 SHIFT IN BX H, generated by the BX SHIFT MUX. The BX SHIFT MUX can select K1-4 ALU COUT H, the output of the EIS overflow detection logic (Kl-10 OUX (1) H), 1 or 0 as the serial input for a left shift.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(3) ALU Multiplexer (AMUX)

The AMUX enables the selection of one of four sources as the input data for the SSMUX. The AMUX can select data which is external to the processor (K1-5 PAX D 15:00 H) or internal data from the ALU, PSW, or constants. The AMUX output can also be placed in a high impedance state. This allows data from the floating point processor or commercial instruction set(CIS) processor to be input to the data path via the AMUX lines. The output enable lines of the AMUX are controlled by the console processor on the multifunction module. When the console processor generates K3-4 FORCE CPU DATA L, the AMUX output is enabled and one of the four AMUX sources can be input to the SSMUX. When the console processor generates K3-4 FREE BUS H, the signal TRI STATE AMUX L is asserted low and the AMUX outputs are placed in the high impedance state.

When the AMUX outputs are enabled, one of the following four inputs will be selected:

a. PAX data (K1-5 PAX D15:00)
b. Constant inputs (K2-2 C7:C1 H) used to generate vectors
c. ALU inputs (ALU 15:00 H)
d. Processor status word (PSW) inputs

(4) Swap Sign Extend Multiplexer (SSMUX)

The SSMUX provides the capability of changing the format of the data before it is output from the data path or routed to another portion of the data path. The value of the two multiplexer select lines determine which of the following functions will be performed by the SSMUX.

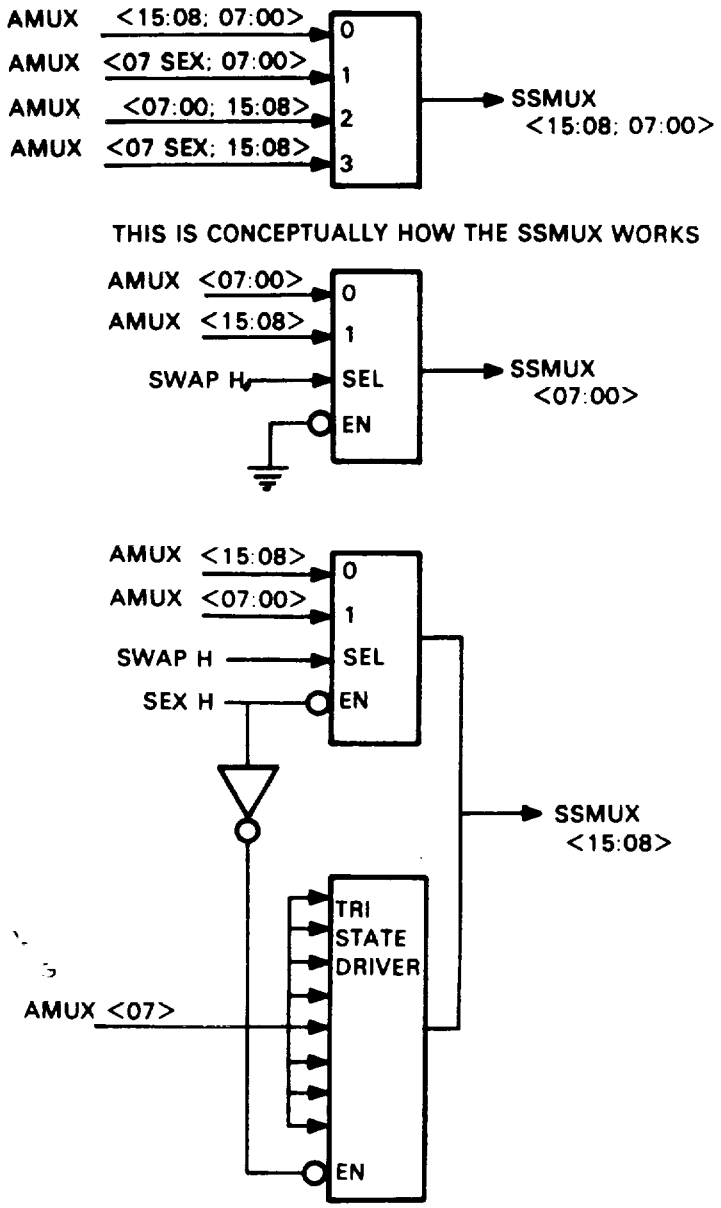
K2-7 SWAP H	K2-7 SEX H	SSMUX Function
0	0	Data is passed through the SSMUX unchanged.
0	1	The sign bit of the low byte (K1-2 AMUX 07 H) is extended into the entire word.
1	0	The low and high bytes of the word are swapped.
1	1	The low and high bytes are swapped and then the sign bit of the new low byte(previously the high byte) is extended into the entire word.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.) _

(4) Swap Sign Extend Multiplexer (SSMUX) (Cont.)

The SSMUX input comes from the AMUX lines (AMUX 15:00). These signal lines can be generated by the AMUX or by the floating point or commercial instruction set (CIS) options. The output of the SSMUX goes to other sections of the data path (PSW, B leg, and scratch pad memory) and to the memory management system. The SSMUX output can also be routed to the rest of the computer system via the PAX data bus.



THIS IS HOW THE SSMUX IS ACTUALLY SET UP.
SSMUX Data Flow

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(5) Scratchpad Memory

The scratchpad (figure next page) consists of a 16-word by 16-bit random access memory. The srcatchpad is divided into four 4-bit slices. The 16 scratchpad registers can be used for temporary storage or as general purpose registers specified during instruction execution. The following lists the scratchpad registers and their normal use.

Register Number	**Description**
R0	
R1	
R2	
R3	General Purpose Registers
R4	
R5	
R6	Kernel Mode Stack Pointer
R7	Program Counter
R8	Temporary Storage
R 11	Unused
R 12	Temporary Storage
R13	Temporary) Storage
R 14	Temporary Storage
R 15	Temporary Storage
R 16	Supervisor Mode Stack Pointer
R17	User Mode Stack Pointer

The scratchpad address (K2-3 SPA 03:00) is generated by the scratchpad address multiplexer (SPAM). The SPAM can select one of the following four address sources on the value of the multiplexer select lines:

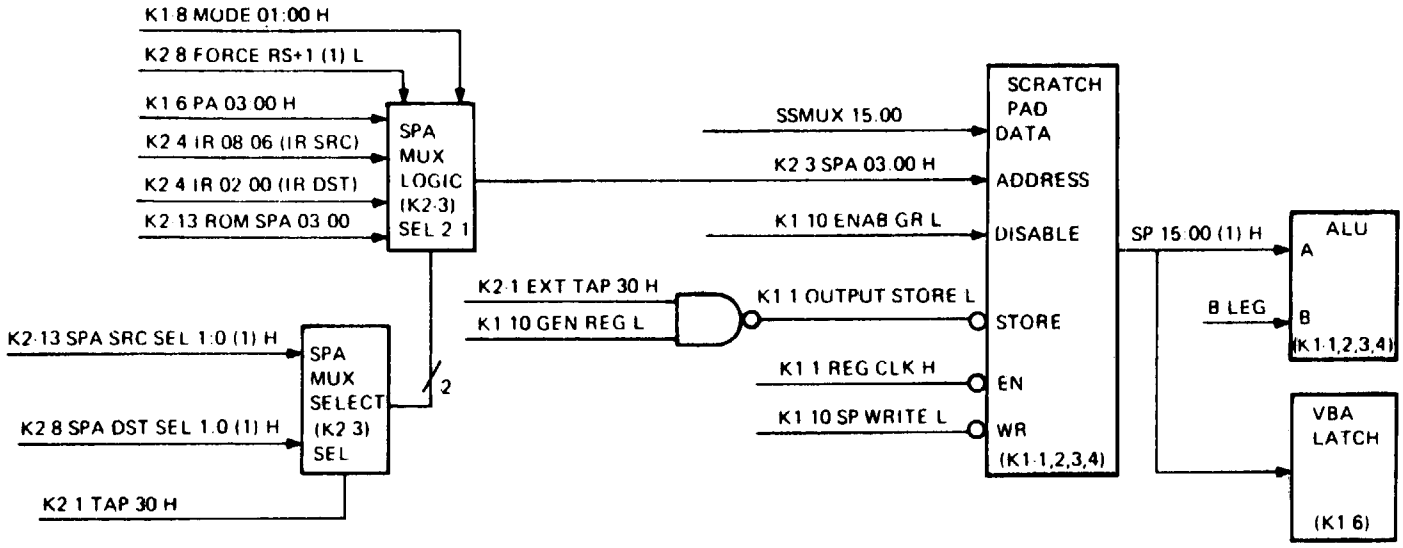
Physical Address Bus (K1-6 PA 03: 00 H) Instruction Register Source Field (K2-4 IR 08: 06) Instruction Register Destination Field (K2-4 IR 02: 00) Control Store ROM SPA Field (K2-13 ROM SPA 03: 00)

Note that scratchpad address R6 is forced to R16 when the memory management system is in user mode and the address is specified by the instruction register or the control store.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(5) Scratchpad Memory (Cont.)



Scratchpad Logic

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(5) Scratchpad Memory (Cont.)

The select lines for the SPAM are also generated by a multiplexer. During the first half of the machine cycle, the signal K2-1 TAP 30 H is not asserted and the multiplexer selects K2-8 SPA SRC SEL 1:0(1) H as the source for the SPAM select lines. During the second half of the machine cycle K2-8 SPA DST SEL 1:0 H is selected as the source. These two sources are generated by two fields of the microinstruction: SPA SRC SEL (CS 52:53) and SPA DST SEL (CS 34:35).

The scratchpad registers can be read or written under program control, or the scratchpad memory can be disabled with its output placed in a high impedance state. Since the scratchpad output is wired ORed with the output of the KT MUX, the scratchpad must be disabled when the KT MUX is enabled. The output of the scratchpad (SP 15:00 (1) H) is fed into the A input of the ALU and the UBA latch.

(6) Processor Status Word (PSW)

The processor status word is a 16-bit register (3 bits are unused) which contains the current and previous memory management modes, an indication of CIS instruction suspension, the current processor priority, a processor trap bit and the condition code results of the previous operation. The following page lists the name and use of each PSW bit.

The PSW is composed of flip-flops (pg. 1-97) which are all clocked by K2-1 EXT CLK B L, provided the proper control signal is enabled. The enabling signals are generated by the control store or the internal address decode PROM. All of the PSW bits can be loaded from the SSMUX. However, the previous memory management mode bits (13:12) and the condition code bits (03:00) can be loaded from alternative sources via the PSW multiplexer.

When the control store generates K2-8 FORCE KERNEL (1) H the PSWMUX selects PSW bits 15:14 as the source of the previous mode bits. When the force kernel line is not enabled, the PSWMUX selects SSMUX bits 13:12.

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(6) Processor Status Word (PSW) (Cont.)

PSW Bit	Name	Use
15:14	Memory Management Current Mode	Contain the current memory management mode.
13:1 2	Memory Management Previous Mode	Contain the previous memory management mode.
11:09	Unused	
08	CIS Instruction Suspension	This bit, when set, indicates that a CIS instruction has been suspended by an interrupt and must be continued upon return from the interrupt. Setting this bit also inhibits a trace trap.
07:05	Priority	Set the processor priority.
0:4	Trace	When this bit is set, the processor traps to the trace vector. Used for program debugging.
03	N	Set when the result of the last data manipulation is negative.
02	Z	Set when the result of the last data manipulation is zero.
01	V	Set when the result of the last data manipulation produces an overflow.
00	C	Set when the result of the last data manipulation produces a carry from the most-significant bit.

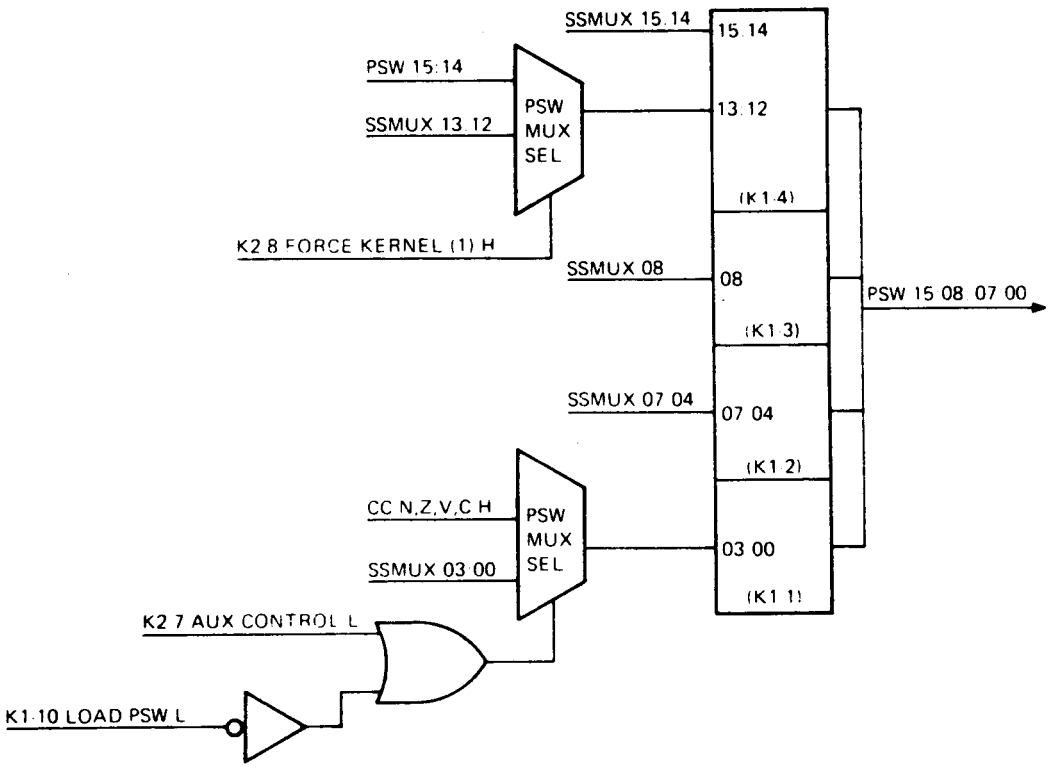
Processor Status Word (PSW) Bits

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

k. DATA PATH (Cont.)

(6) Processor Status Word (PSW) (Cont.)

When the internal address decode logic generates KI-10 LOAD PSWL, the PSWMUX selects the SSMUX as the source for bits 03:00 of the PSW. The condition code bits (KI-10 CC N,Z,V,C) are loaded into the PSW only if the address decode does not generate the LOAD PSW line and the control store generates the auxiliary control signal (K2-7 AUX CONTROL L).



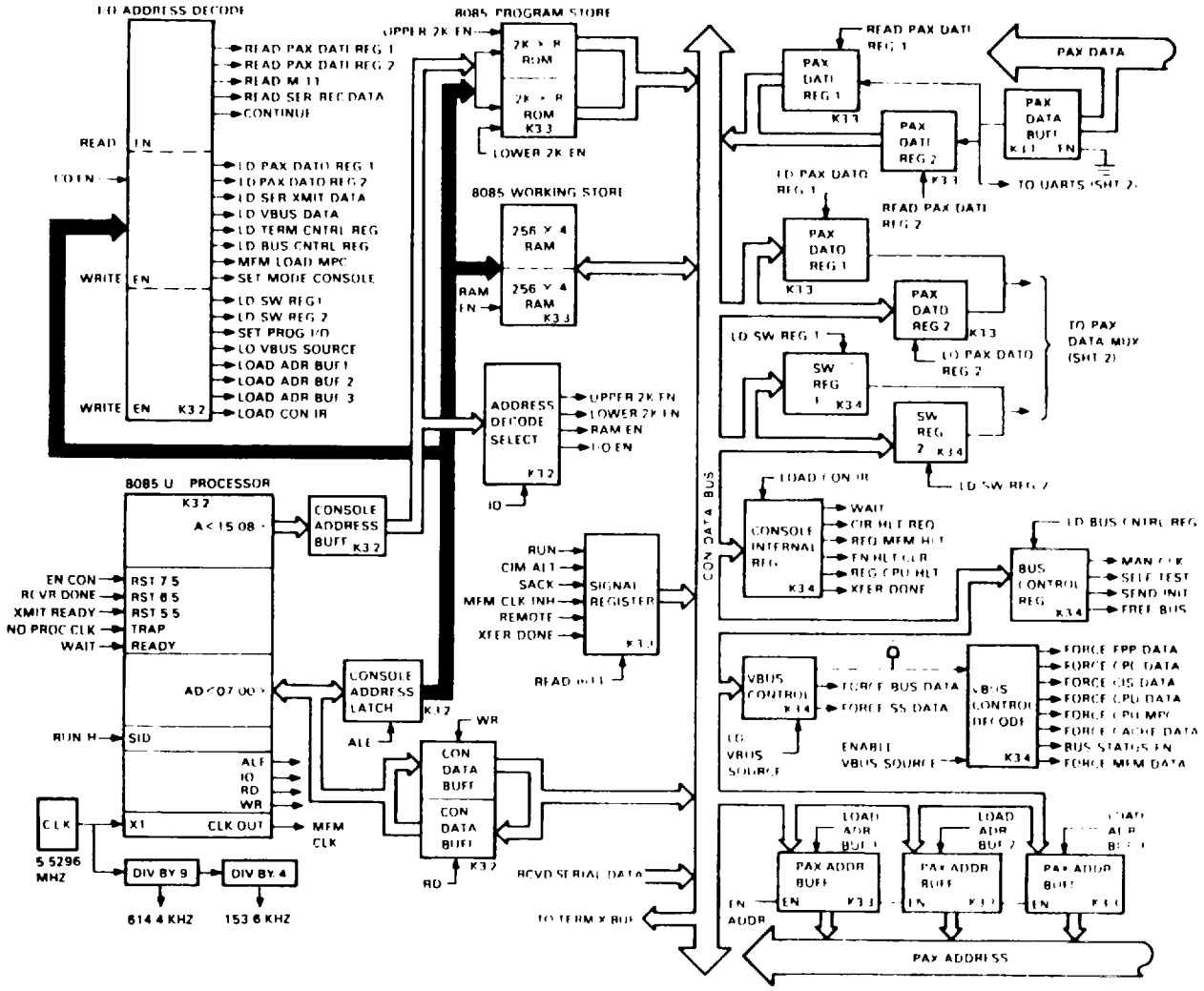
PSW Logic

PSW Logic

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

1. MULTIFUNCTION MODULE (MFM)

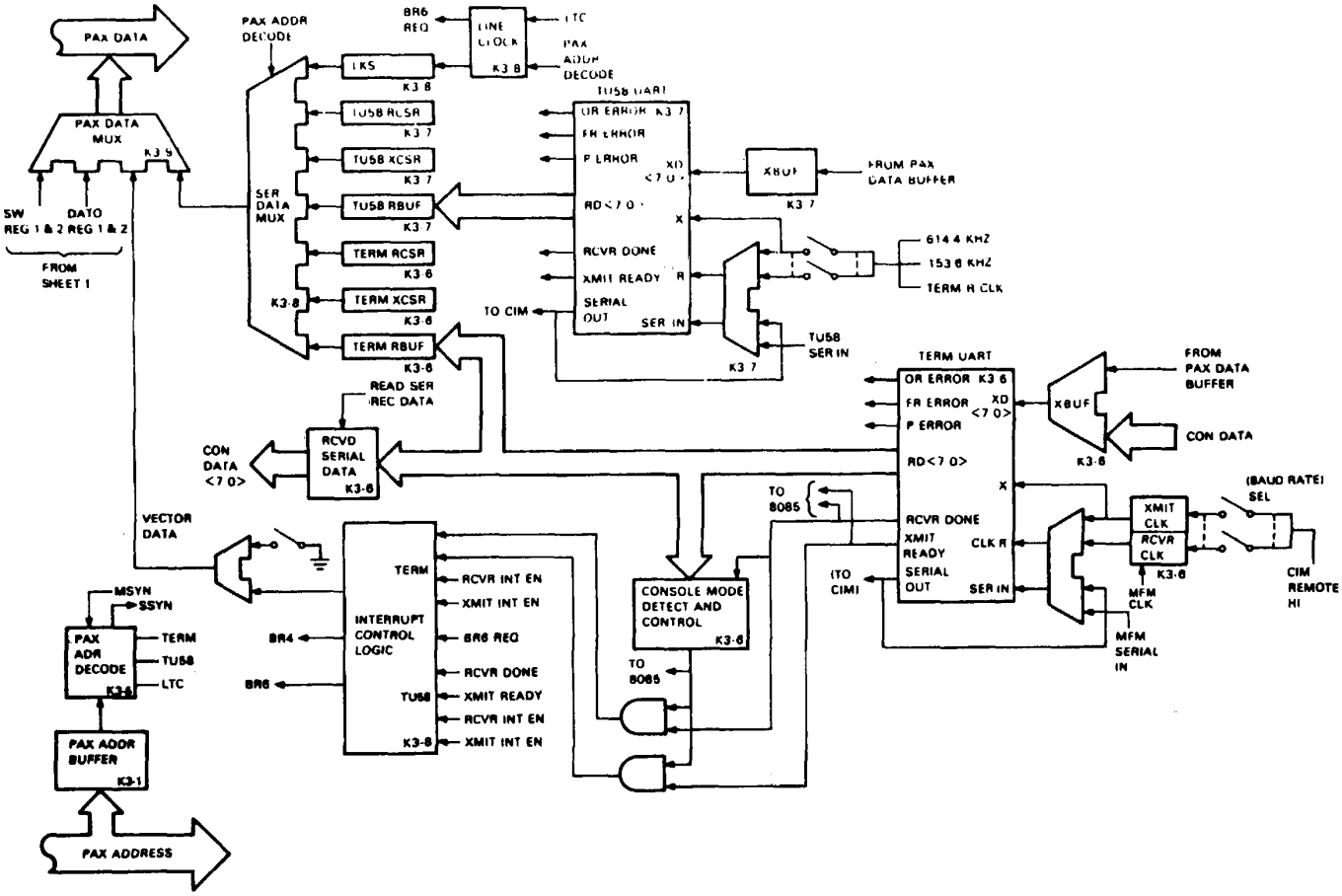
A two-board module containing an 8085 microprocessor, two serial line ports, a line clock, and related logic. The microprocessor allows a system terminal to be used as a programmer's console. The 8085 software routines enable the execution of the console commands discussed in Appendix H of TM11-6625-3268-14&P.The serial line port used for the system terminal also serves as a diagnostic serial port. The second serial line port is available for another serial device such as a tape unit.



MFM Block Diagram (Sheet 1 of 2)

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

1. MULTIFUNCTION MODULE (MFM) (Cont.)

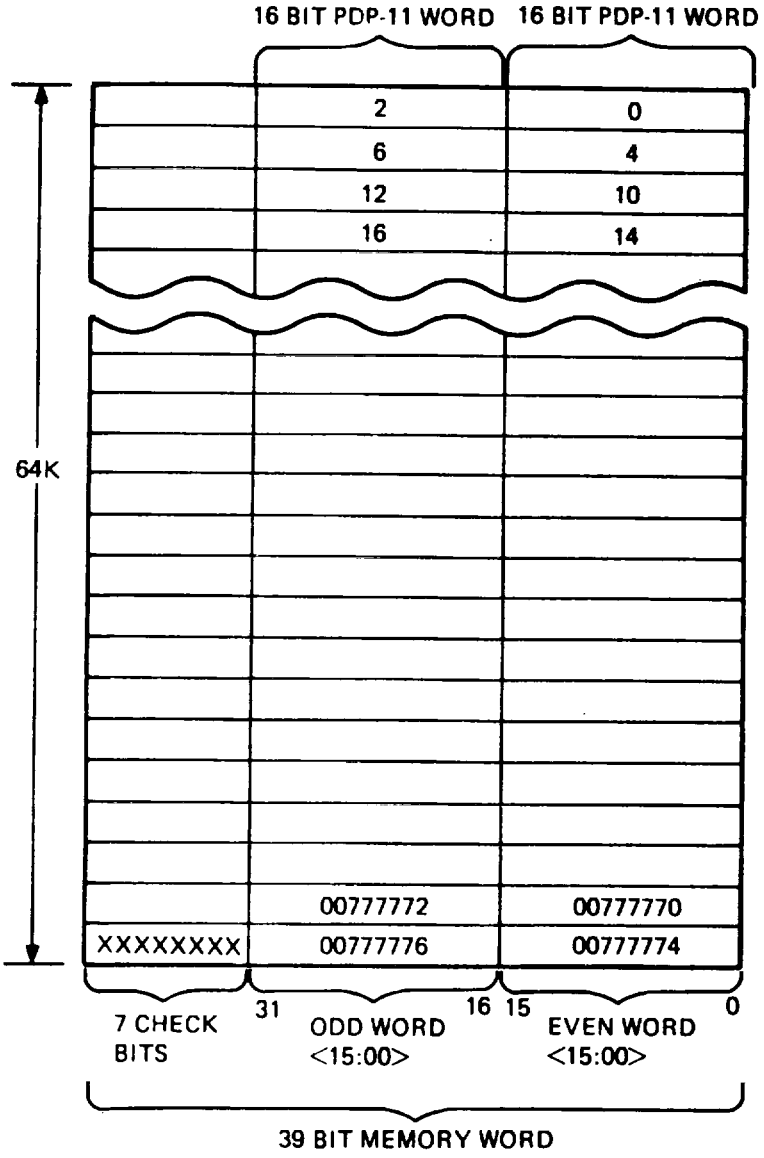


MFM Block Diagram (Sheet 2 of 2)

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

m. MOS. MEMORY

The MOS. memory (MS11-M) provides 256K words on each module. Two are installed in the current configuration. Each memory module contains timing and control logic, error correcting code logic, and a MOS. storage array.

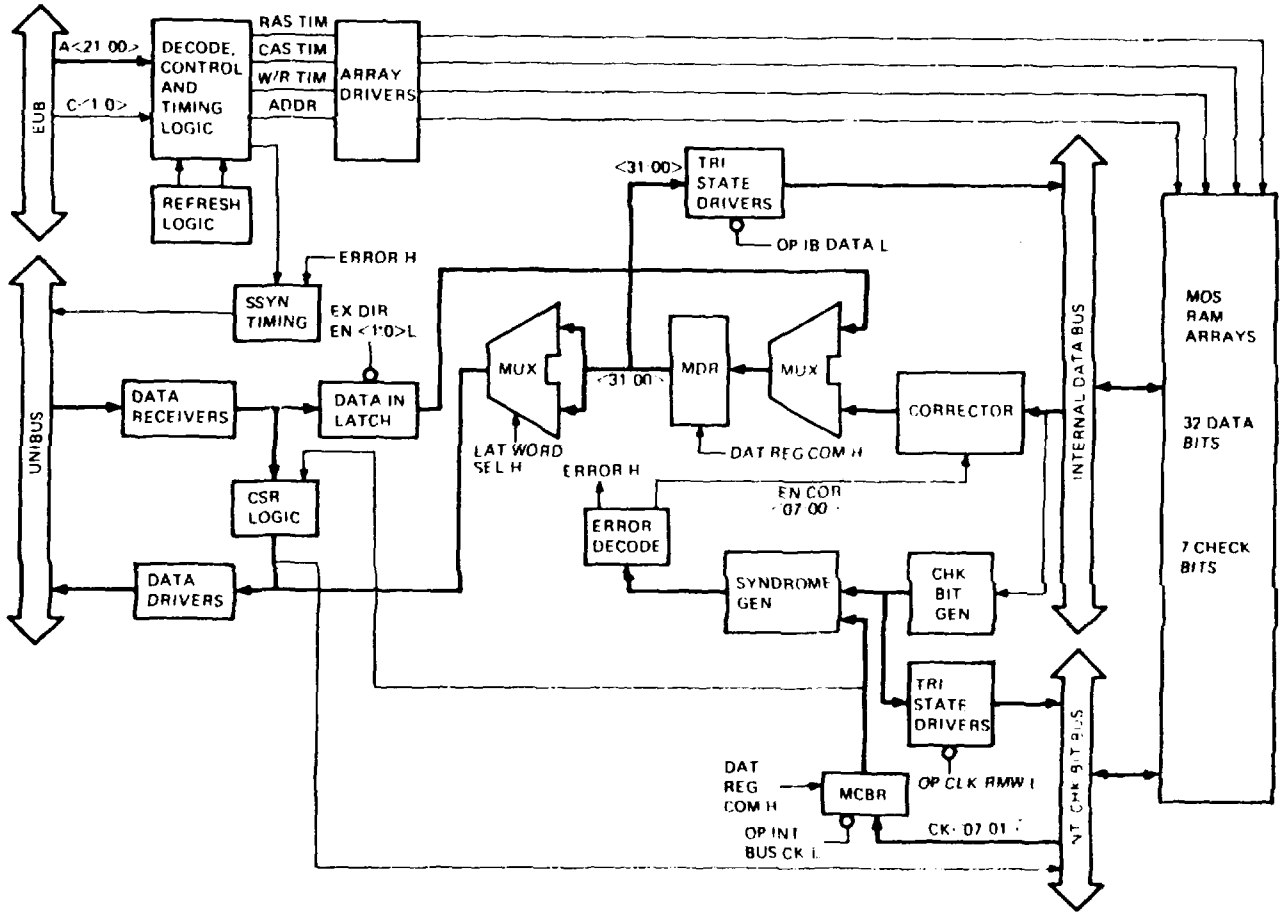


NOTE:
ALTHOUGH THE MOS STORAGE ARRAY IS CONFIGURED IN 39 BIT WORDS, THE BUS MASTER SEES THE MS11-M AS A STANDARD 16 BIT MEMORY.

MS11-M Storage Array

1-13. FUNCTIONAL DESCRIPTION OF COMPUTER (Cont.)

m. MOS. MEMORY (Cont.)



MS11-M Block Diagram

1-101/1-102 (BLANK)

CHAPTER 2
UNIT MAINTENANCE

Section I. REPAIR PARTS, SPECIAL TOOLS; TEST, MEASUREMENT, AND DIAGNOSTIC EQUIPMENT (TMDE); AND SUPPORT EQUIPMENT

2-1. COMMON TOOLS AND EQUIPMENT

a. Army. For authorized common tools and equipment, refer to the Modified Table of Organization and Equipment (MTOE) applicable to your unit.

2-1. COMMON TOOLS AND EQUIPMENT (Cont.)

b. Navy. Navy personnel refer to applicable Tables of Allowance (TA).

c. Air Force. Air Force personnel refer to applicable Tables of Allowance (TA).

2-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

No special tools, TMDE, or support equipment is required for the computer at Unit Maintenance level.

2-3. REPAIR PARTS

No repair parts are required at Unit Maintenance level.

Section II. SERVICE UPON RECEIPT

2-4. UNPACKING

There are no special procedures for unpacking the Computer. However, avoid damaging the container during unpacking operation and report the empty containers through established supply channels or, if applicable, use it to package another unserviceable Computer.

2-5. CHECKING UNPACKED EQUIPMENT

a. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, report the damage on SF-364, Report Of Discrepancy (ROD).

b. Check the equipment against the packing slip to see if the shipment is complete. Report all discrepancies in accordance with the instructions of DA Pam 738-750.

c. Refer to DA Pam 25-30 to see if your equipment has had any MWOs applied.

2-6. PRELIMINARY SERVICING AND ADJUSTMENT OF EQUIPMENT

Not applicable.

Section III. PREVENTIVE MAINTENANCE CHECKS AND SERVICES (PMCS)

2-7. INTRODUCTION

Preventive maintenance procedures help maintain the equipment in a serviceable condition. They include items to be checked and procedures for checking them. The checks and services described in the PMCS table outline inspections that are to be made at specific Monthly (M) and Quarterly (Q) intervals.

a. Routine Checks. The following items are not listed in the PMCS table. Defects that can be found by these checks should be reported and corrected when found.

- •. Cleaning and dusting.
- •. Checking for frayed or loose cables.
- •. Covering unused receptacles.
- •. Checking for loose nuts, bolts, and screws.

b. Explanation of Columns.

(1) Item number column. This column is used as a source of item numbers for the TM Number Column of DA Form 2404, Equipment Inspection and Maintenance Worksheet, in recording results of PMCS.

(2) Interval column. This column specifies the frequency of the check, M for Monthly checks and Q for Quarterly checks.

(3) Item to be inspected column. This column specifies the item that is to be checked.

(4) Procedures column. This column describes the procedure by which the check is to be performed.

NOTE

If your equipment must be in operation all the time, only do items that can be checked and serviced without disturbing operation. Make the complete checks and services when the equipment can be shut down.

2-8. UNIT PMCS TABLE

Item No	Interval		Item To Be Inspected	Procedures
	M	Q		
1	•		End item equipment	Inspect for completeness

Section IV. UNIT TROUBLESHOOTING

2-9. GENERAL

Unit level troubleshooting for the computer is performed in the Force Terminal and consists of on-line BIT to determine system operability. Refer to applicable system Operator Technical Manual to perform BIT.

2-10. TROUBLESHOOTING PROCEDURES

Troubleshooting the computer is limited to running Terminal on-line BIT. Upon completion of corrective action and before returning the computer to service, perform on-line BIT. Refer to the following manuals for computer replacement procedures.

- -TM-11-5895-1218-12 (Navy) EE150-LQ-OMI-010/ Wl11OTRC179Vl (Air Force) TO 31R2-2TRC179-21.

Section V. UNIT MAINTENANCE

2-11. GENERAL

Unit maintenance is limited to replacement of the computer.

2-12. OPERATIONAL CHECK

To check the operational condition of the computer initiate BIT as described in TM 11-5895-1218-12 (Navy) EE150-LQ-OMI-OIO/W110-TRC179V1 (Air Force) TO 31R2-2TRC179-21.

2-13. INSPECTION OF INSTALLED ITEMS

Inspect and insure the UNIBUS Terminator is installed and securely attached to J5 on the computer front panel.

SECTION VI. PREPARATION FOR STORAGE OR SHIPMENT

2-14. GENERAL

NOTE

A faulty or suspected bad CPU unit that has been previously loaded with operational program tapes and cannot be zeroized, is presumed to contain classified data, and therefore must be treated as a sensitive item. Follow local site procedures to store, handle, and transport a classified unit.

a. Army. Prepare the computer for storage in accordance with the procedures in TM 740-90-1.

b. Navy. Refer to NAVSUP PUB 503.

c. Air Force. Refer to AFM 66-267 (storage) and AFR 67-31 (shipment).

2-15. MARKING

The marking on the exterior of the container shall be in accordance with MIL-STD-129H.-

2-5/2-6 (BLANK)

CHAPTER 3
SPECIALIZED REPAIR ACTIVITY (SRA) MAINTENANCE

NOTE
Intermediate Direct Support Maintenance is not allocated for the computer.

Subject — Page

SECTION I. REPAIR PARTS, SPECIAL TOOLS; TEST, MEASUREMENT, AND DIAGNOSTIC EQUIPMENT (TMDE); AND SUPPORT EQUIPMENT

3-1. COMMON TOOLS AND EQUIPMENT

a. Army. For authorized common tools and test equipment, refer to the Modified Table of Organization and Equipment (MTOE) applicable to. your unit.

b. Navy. Navy Personnel refer to applicable Tables of Allowance (TA).

c. Air Force. Air Force reference to applicable Tables of Allowance (TA).

3-2. SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

Special tools, TMDE, and support equipment and their purposes are identified in the Maintenance Allocation Chart, Appendix B.

3-3. REPAIR PARTS

Repair parts used during Intermediate General Support Maintenance are listed and illustrated in the repair Parts and Special Tools List located in TM 11-5895-1308-40P, (Navy) EE610-HD-PLD-010/W110-UYK42V4, (Air Force) TO 31S5-2UYK42-54.

SECTION II. SPECIALIZED REPAIR ACTIVITY TROUBLESHOOTING

3-4. GENERAL

This section provides:

- •. Description of troubleshooting concept.
- •. Description of test setup.
- •. Troubleshooting procedures.
- •. Troubleshooting flow charts.

3-4. GENERAL (Cont.)

Troubleshooting is limited primarily to locating a specific malfunctioning plug-in module or power supply module. Some additional troubleshooting of transition harness is also performed. However, Grandmother Board and Power Supply Back plane problems, once identified, requires return of computer to higher level maintenance.

NOTE

Do not attempt to use the troubleshooting flow charts until you become familiar with the information and procedures in paragraphs 3-5 through 3-10.

3-5. OPERATIONAL CHECK OF THE CPU

INITIAL SETUP

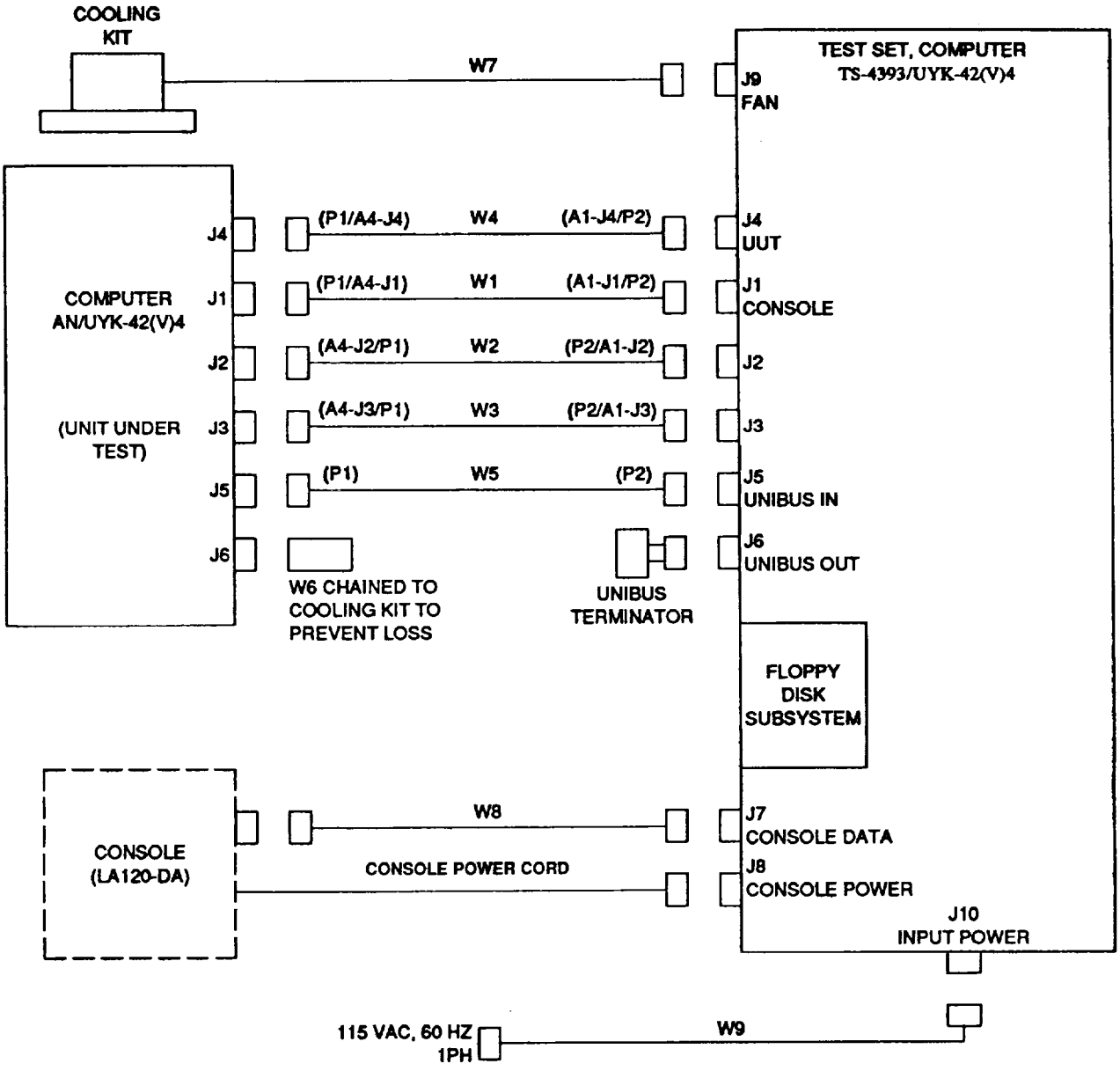
Test Shipment	Requirement Condition
Computer Test Set, TS-4393/UYK-42(V)4, with cables W1 - W9, Diagnostic Software, 109D-C600-4.1, Cooling Kit and Torque Screwdriver Kit UNIBUS Terminator, 109D00320 Console, LA120-DA-WE or equivalent	Equipment connected as shown in Test Setup Diagram. Power removed. Tools Tool Kit, TK-17.
•. Part of TS-4393/UYK-42(V)4	Torque Screwdriver. (2-36 inch. pounds) Work Station Static

NOTE

Alternate consoles can be utilized in place of the LA120-DA. The selected console must maintain the requirements of EIA specification RS-232-C. The part provides full duplex asynchronous communication on a 25 pin connector. Required pin numbers are defined in TM 11-6625-3268-14&P.

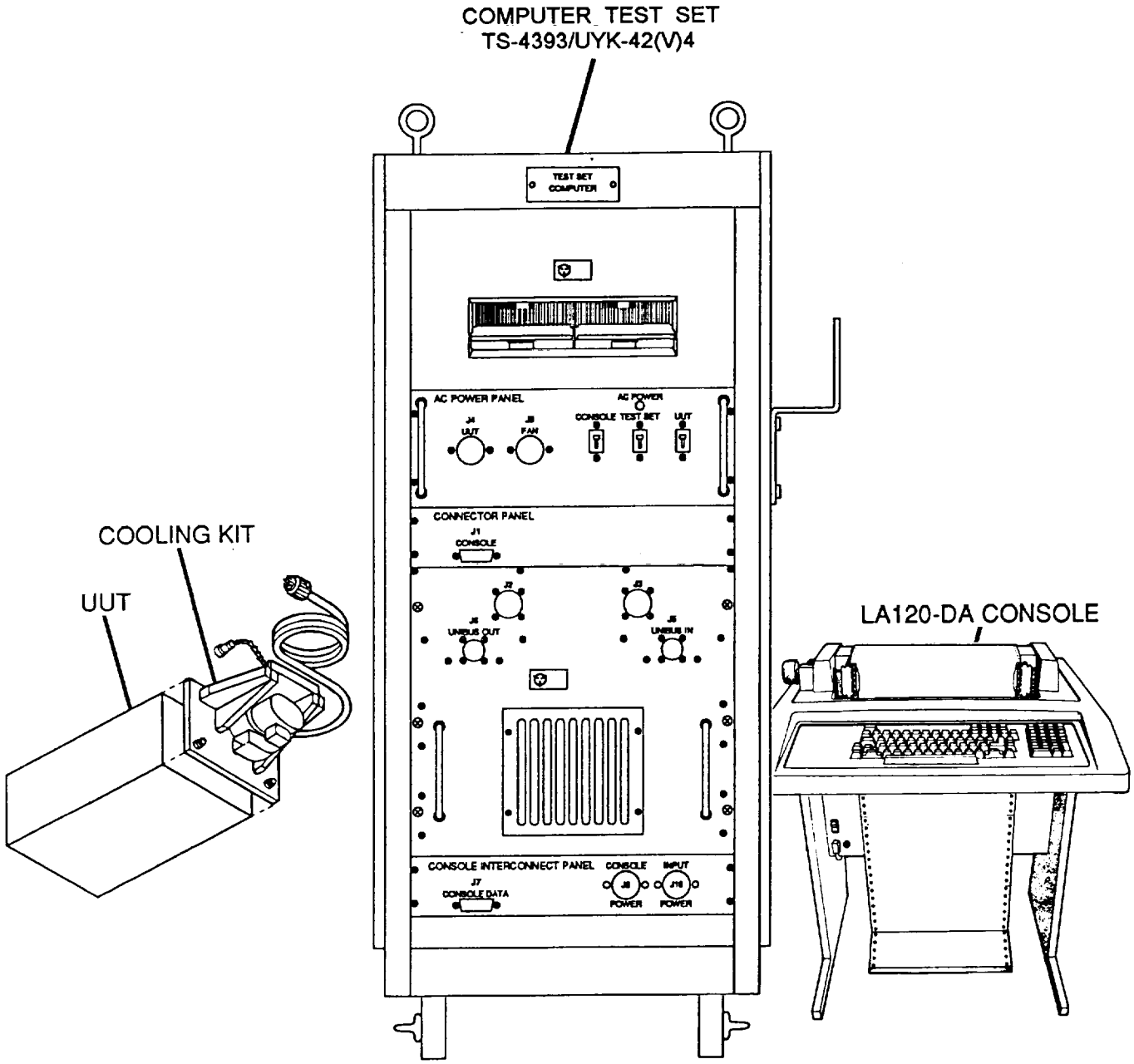
1. Ensure that all elements of the Computer Test Set are present and fully operational.

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)



TEST SETUP DIAGRAM

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)



TEST SETUP ILLUSTRATION

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

2. Ensure that prime power is available.

This equipment contains electrostatic discharge sensitive (ESD) devices. Methods to be followed are specified in DOD-STD-1686 and DOD-HDBK-263.

3. In the UUT (CPU), locate and remove Multifunction Assembly (A1A12) and Console IF module (AlA13). Refer to paragraph 3-13 4. Refer to paragraph 3-16 and locate switch number 8 on switch S102 of A1A12A1 and change to the closed position.

5. Refer to paragraph 3-16 and locate switch number 5 on switch S2 of A1A13 and change to the closed position.

6. Refer to paragraph 3-13 and reinstall AlA12 and A1A13.

Once testing is completed, switches S102 on Multifunction Assembly (A1A12) module and S2 on Console IF (A1A13) module must be reset to original position; otherwise the Computer will not operate properly. Refer to paragraph 3-16 to verify switch settings.

7. Ensure that all other plug-in modules are in place. Refer to paragraph 3-11.

8. Remove UNIBUS Terminator from CPU J5 and connect to Test Set connector J6.

9. Refer to Test Setup Diagram and Test Setup Illustration and install Cooling Kit Assembly on the computer as follows:

a. Position fan at back end of computer and align the top screws in the cooling kit with the threaded holes in the computer.

b. Secure two top and two bottom screws.

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

c. Attach chained dummy connector (W6) to J6 on the computer.

d. Connect cooling kit power cord (W7) to J9 on the Test Set.

10. Connect all cables, connectors, and terminators as listed in table 3-1 The connector reference designators (for example A1-J1/P2) are marked on both ends of the cable.

Table 3-1. Interconnecting Cable List

Cable Number	Test Set	Destination
W1	T/S-J1 (A1-J1/P2)	CPU-J1 (P1/A4-J1)
W2	T/S-J2 (P2/Al-J2)	CPU-J2 (A4-J2/P1)
W3	T/S-J3 (P2/A1-J3)	CPU-J3 (A4-J3/P1)
W4	T/S-J4 (A1-J4/P2)	CPU-J4 (P1/A4-J4)
W5	T/S-J5 (P2)	CPU-J5 (P1)
W8	T/S-J7	CONSOLE Data Connector (25 pin CANNON)
W9	T/S-J10	TEST SET Power Input Cord
-----	T/S-J8	CONSOLE Power Cord

11. Connect the Test Set to the prime power (115 Vac). Check that the Test Set AC POWER light is lit.

12. Turn on Computer Test Set and equipment as follows: a. Set Console Switch on Computer Test Set to the ON position.

b. While holding SET-UP key down, continue pressing BAUD key until 1200 appears in readout.

c. Turn TEST SET switch on Computer Test Set to ON and check for operation of Test Set cooling fan.

d. Set UUT switch on the Computer Test Set to the ON position.

13. Check proper fan operation by feeling for air flow at intake vents along each side of the front of the Computer housing while CPU is running.

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

14. Visually check the CPU front panel ELAPSED TIME indicator to verify that elapsed time indicator is running. Proper ETM operation is indicated by a flashing dot between the first two digits of the readout. Refer to paragraph 3-8.

Do not open the drive door while the diskette is in use; this results in errors.

NOTE

The disk drive is designed for 60 cycle input only, 50 cycle input will result in errors.

15. Visually check the CPU front panel POWER ON LED. The LED is wired directly to +5 VDC. If LED is not on while CPU power is on, it may indicate a faulty power supply. Refer to paragraph 3-8.
16. Check SMI, SMA, and SMS LED's for fault indication and replace module(s), if necessary.

NOTE

System will not auto boot to run diagnostics. The console will print a console prompt ">>>" when the CPU is powered up (step 12d).

NOTE

Instructions to declassify CPU are located in paragraph 3-17.

17. Install diagnostic diskette 109D-C600-4.1 into disk drive "0" (left disk drive) and secure disk drive door. Using the Console, enter commands and respond to displayed prompts as indicated as follows:

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

NOTE

The RX02 disk drive has no operator controls and indicators. The diskette is inserted in a drive after compressing the latch to allow the spring-loaded front cover to open. Place the diskette with the label or top up (the jacket seams are on the bottom) on the drive spindle. Close the front cover which will automatically lock when it is pushed down. When booting the system, listen for audible clicking sounds which indicate the head is moving over the diskette; the RX02 is ready for use.

NOTE

- **Do not expose diskettes to a heat source or sunlight.**
- **Keep the diskettes from magnetic fields.**
- **Do not use paper clips on diskettes.**
- **Do not write on the diskette with an instrument that leaves an impression or flakes.**

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

COMMAND ENTER	DISPLAYED RESULTS PROMPTS	OPRERATOR RESPONSE.
<CTRL P> (simultaneously)		>>>
H <CR>	>>>	

NOTE
If you type a wrong key, type <CTRL P> to restart.

B DYO <CR>	>>>	
	The computer will respond by printing a series of messages and prompts on the console as follows:	
	CLEARING MEMORY	
	CHMYAO XXDP+ DY MONITOR 28K	
	BOOTED VIA UNIT 0	
	ENTER DATE (DD-MMM-YY)	(DD-MMM-YY) <CR>
	RESTART ADDRESS: 153726	
	50 HZ	N <CR>
	LSI?	N <CR>
	THIS IS XXDP+ TYPE "H" OR "H/L" FOR DETAILS	
	Respond to each prompt above as indicated until the prompt "." appears. Then type the following on the console.	
C C600 <CR>	At this point the CPU will automatically run the diagnostics as called for in the chain file. A sample printout is shown in Appendix D.	

18. If unable to boot and execute diagnostics (no printer output) proceed to paragraph 3-8.

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

NOTE

At this point the Computer will automatically run the diagnostics as called for in the chain file as listed in Appendix D. The Console will display/print test status, i.e. error message, with probable faulty module or "end pass," indicating a fully operational UUT. When the final message is displayed on the Console, the operational check is complete.

19. If CPU boots and diagnostics begin to run, allow it to run until one of the following occurs:

    - •. Completion (indicated by END PASS)
    - •. Machine halts due to test failure
    - •. Failure is detected but CPU keeps running.
- •. Error message on printout, with or without END PASS message.
- •. Any message on printout, other than shown in Appendix D

20. Observe console printout to identify any failures. CPU modules are so closely interrelated that a failed test merely indicates that one or more of a group of modules has failed. A recommended order of replacement is given on the printout. Prefix all reference designators on the printout with "AI".

21. Replace the suspected faulty assembly. Refer to paragraph 3-13 for removal and installation instructions for plug-in modules.

NOTE

If a plug-in module with programmable switches is replaced, ensure that the switches are set properly. Refer to paragraph 3-10.

22. Re-run the diagnostics (step 16) and continue replacing modules as specified in the order of replacement called for in the printout until problem is corrected.

3-5. OPERATIONAL CHECK OF THE CPU (Cont.)

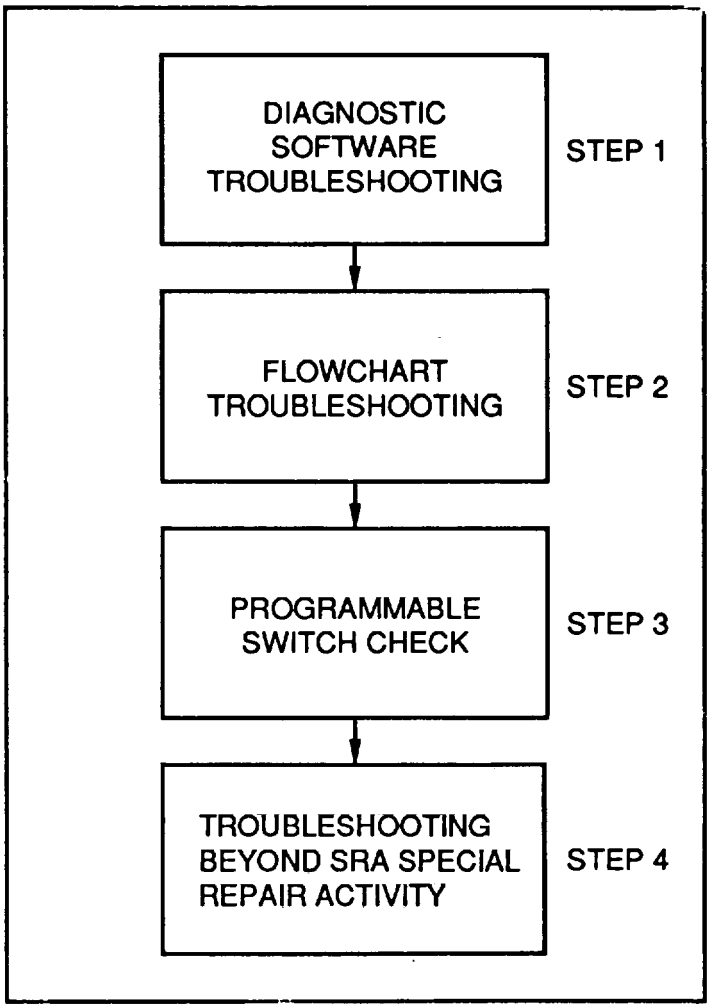
23. If the above troubleshooting and assembly replacement sequence does not correct the problem, refer to higher level of maintenance.

24. If above troubleshooting and assembly replacement does correct problem, re-establish computer integrity (paragraph 3-9).

25. Remove diagnostic diskette from Disk Drive "0". Return diskette to protective envelope and store in dust proof bag, away from heat or magnetic objects.

3-6. TROUBLESHOOTING CONCEPT

To assist in rapid identification and replacement of faulty modules, troubleshooting is organized into four steps as shown below:



3-6. TROUBLESHOOTING CONCEPT (Cont.)

Step 1. DIAGNOSTIC SOFTWARE TROUBLESHOOTING

- The suspect CPU is connected to the Computer Test Set and Console.
- An attempt is made to run diagnostic software to isolate fault.

Step 2. FLOW CHART TROUBLESHOOTING

- Diagnostics may not run.
- Troubleshooting flow charts are used to localize failure and correct to point where-diagnostics will run.
- Diagnostics are run to confirm repair or locate additional faults.

Step 3. PROGRAMMABLE SWITCH CHECK

- If repair is accomplished by replacement of plug-in module that has programmable switches, module may not be faulty.
- Module status is determined by checking and resetting switches and attempting to run diagnostics with suspect module in place.
- If failure is again indicated, module is faulty; otherwise module is good.

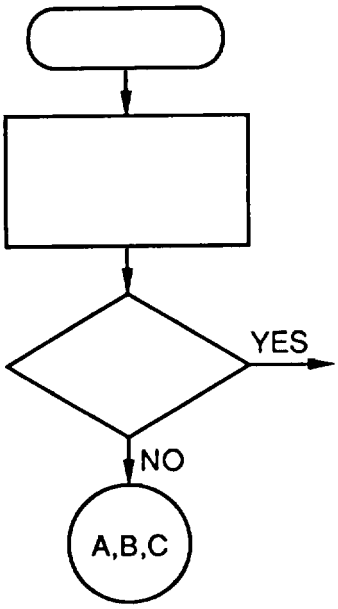
Step 4. TROUBLESHOOTING BEYOND SRA AUTHORIZATION

- If all efforts fail to locate problem, entire unit is forwarded to higher level maintenance.
- If failure is discovered in GMB or Power Supply Back plane, entire unit is forwarded to higher level maintenance.
- If a power supply or plug-in module is determined to be faulty, that assembly is forwarded to higher level maintenance.

3-7. FLOWCHARTS AND HOW TO USE THEM

If unable to bootstrap and execute chain diagnostics (no printer output), refer to Initial Diagnostics Setup (paragraph 3-8.a.). Make observations and follow directions given on flow chart. They will either identify a faulty module or refer you to another paragraph.

Proceed as directed and you should be able to isolate and correct the fault.

SYMBOL	MEANING
	START AND FINISH SYMBOL INDICATES STARTING AND FINISHING POINTS. TASK SYMBOL INDICATES WHAT TO DO AND WHERE TO DO IT. DECISION SYMBOL (YES OR NO) INDICATES THAT A DECISION MUST BE MADE. THE DIRECTION TO GO FROM THE DECISION SYMBOL DEPENDS ON THE DECISION MADE. CONTINUATION SYMBOL INDICATES THAT THE PATH CONTINUES TO OR FROM ANOTHER FLOWCHART.

3-8. FLOWCHART DIAGNOSTICS

INITIAL SETUP

Test Equipment	Equipment Condition
Computer Test Set, TS-4393/UYK-42(V)4 With cables W1 through W9 and Diagnostic Chain Software, 109D-C600-4.1 UNIBUS Terminator, 109D00320 Console, LA120-DA-WE .	Equipment connected as shown in paragraph 3-5. Power removed. Cover removed (paragraph 3-12) Tools Tool Kit, TK-17 Workstation, Static

NOTE

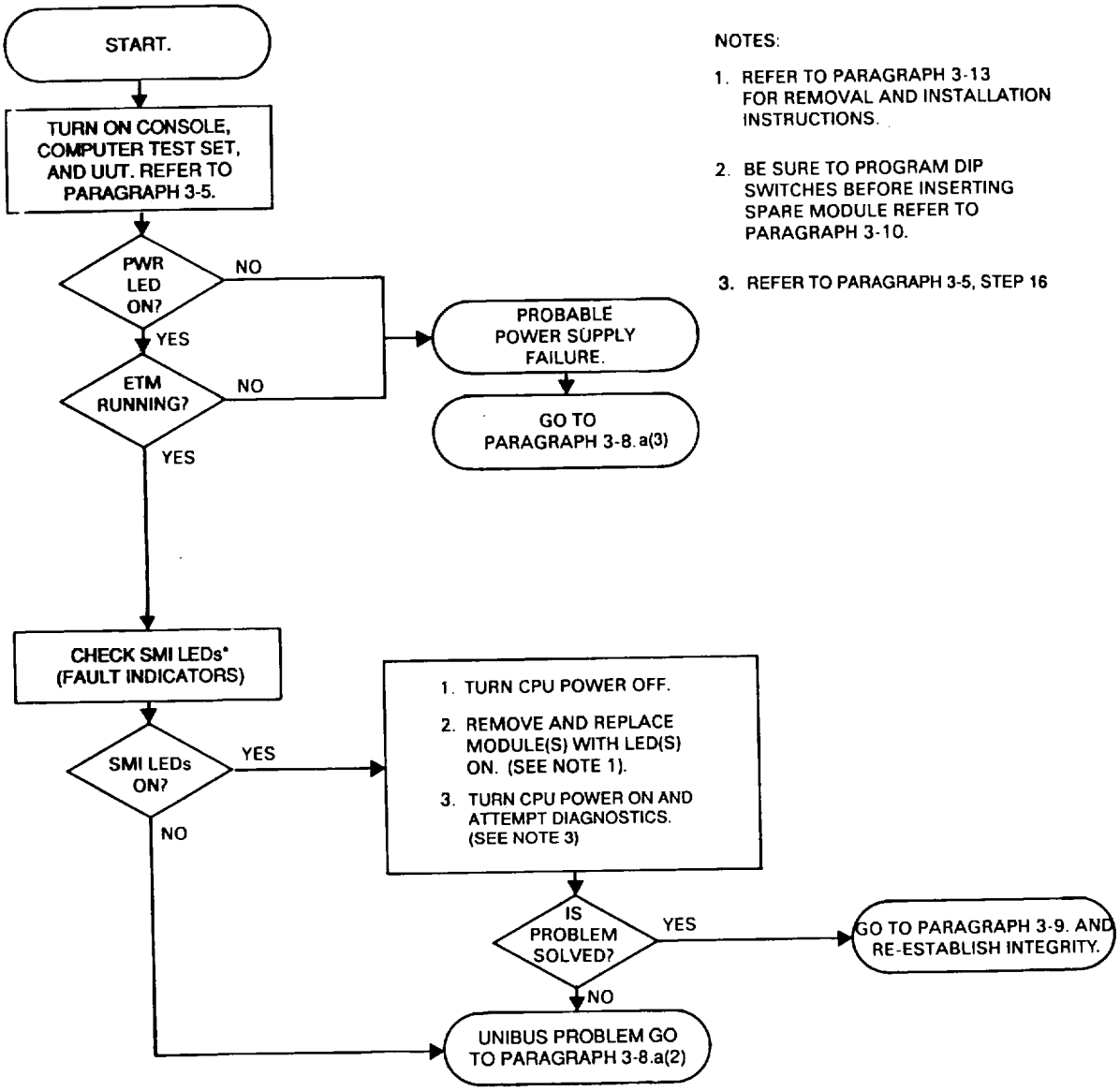
Alternate consoles can be utilized in place of the LA120-DA. The selected console must maintain the requirements of EIA specification RS-232-C. The part provides full duplex asynchronous communication on a 25 pin connector. Required pin numbers are defined in TM 11-6625-3268-14&P.

CAUTION

This equipment contains electrostatic discharge sensitive (ESD) devices. Methods to be followed are specified in DOD-STD-1686 and DOD-Handbook-263.

3-8. FLOWCHART DIAGNOSTICS (Cont.)

a. Unable to Boot CPU Diagnostic
(1) Initial Diagnostic Setup



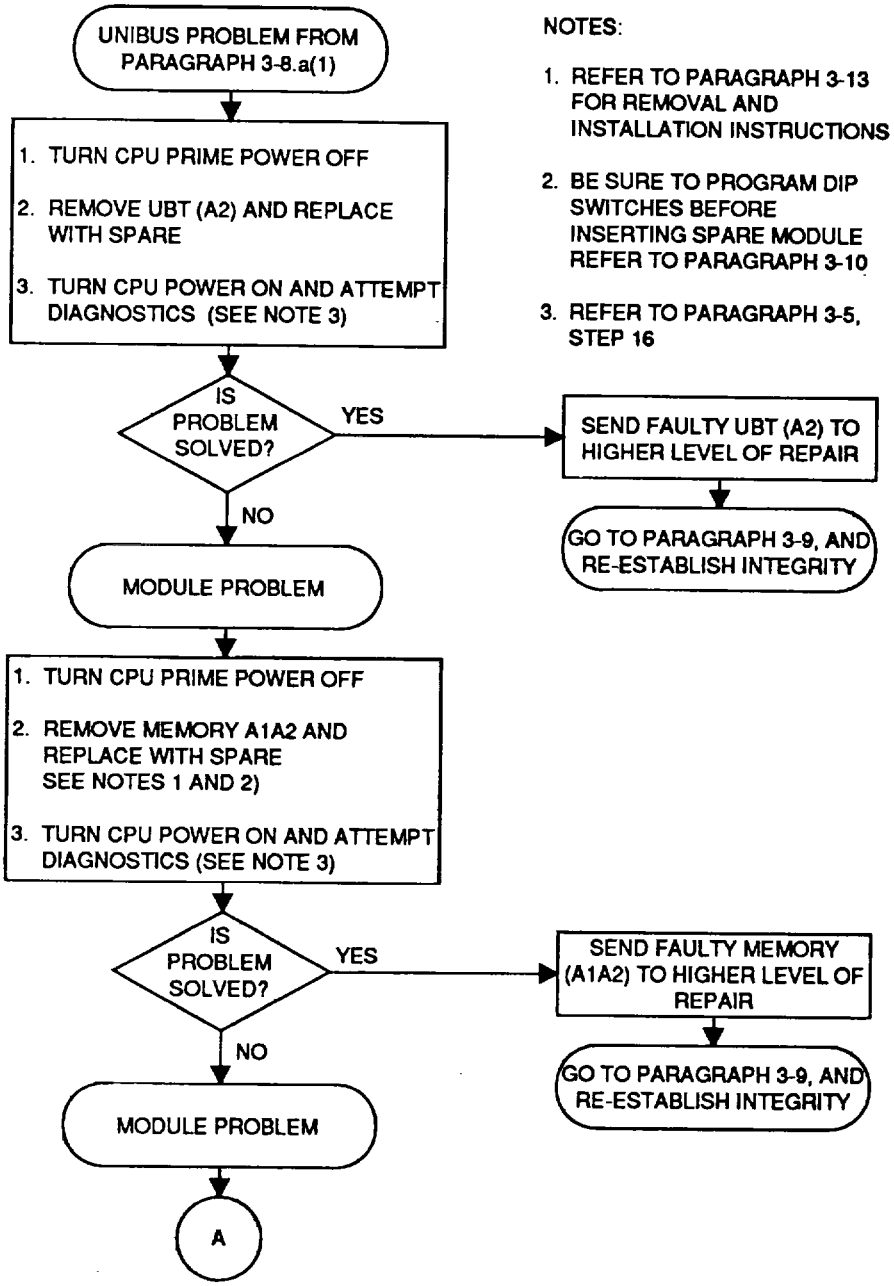
* SMI MODULES ARE SMS(A1A5), SMA(A1A6), AND SMI(A1A7)

NOTE

FOR MAINTENANCE PROCEDURES, REFER TO INDEX AT BEGINNING OF CHAPTER.

3-8. FLOWCHART DIAGNOSTICS (Cont.)

a. Unable to Boot CPU Diagnostic (Cont.)
(2) UNIBUS/Module Troubleshooting.

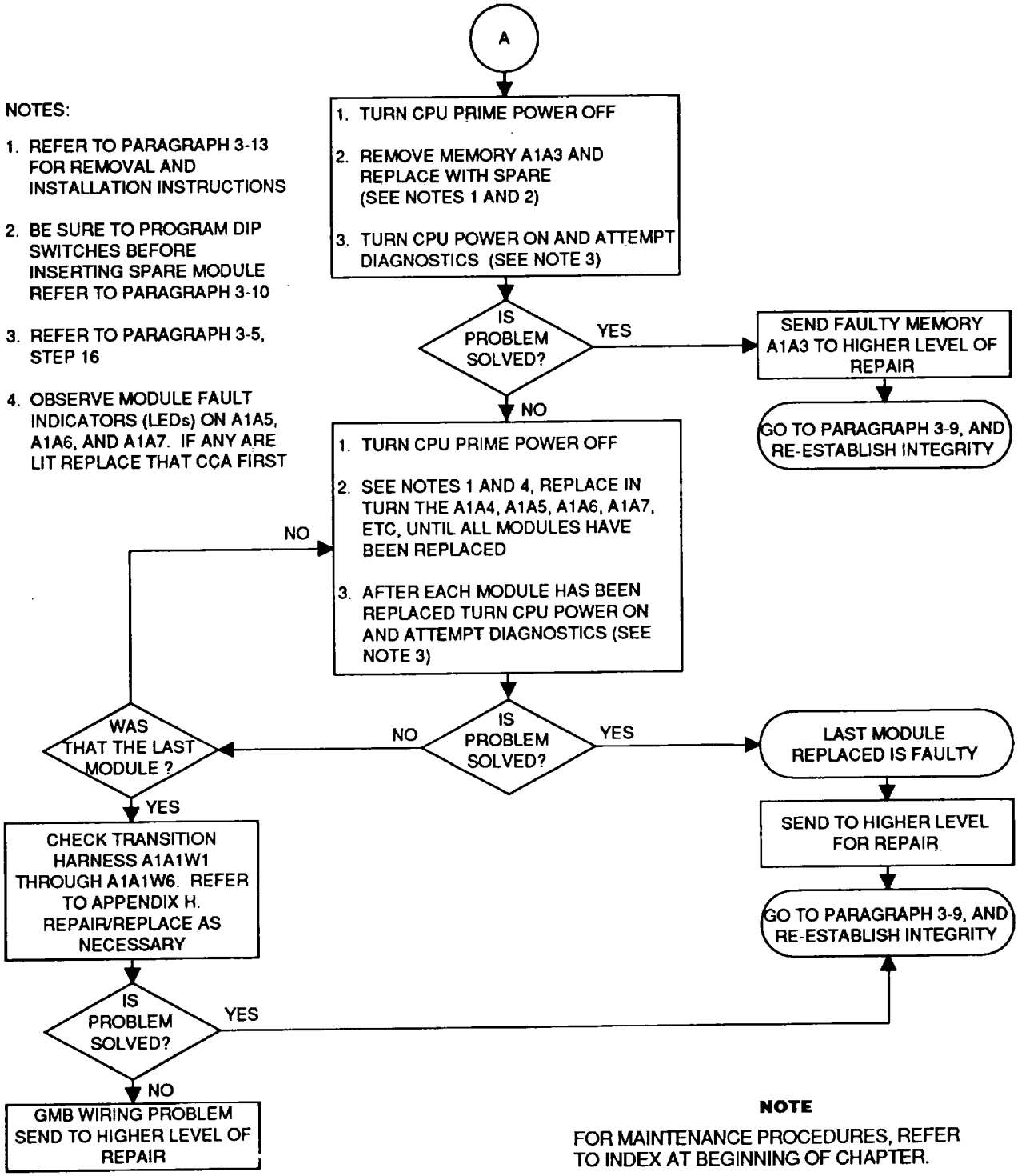


NOTE

FOR MAINTENANCE PROCEDURES, REFER TO INDEX AT BEGINNING OF CHAPTER.

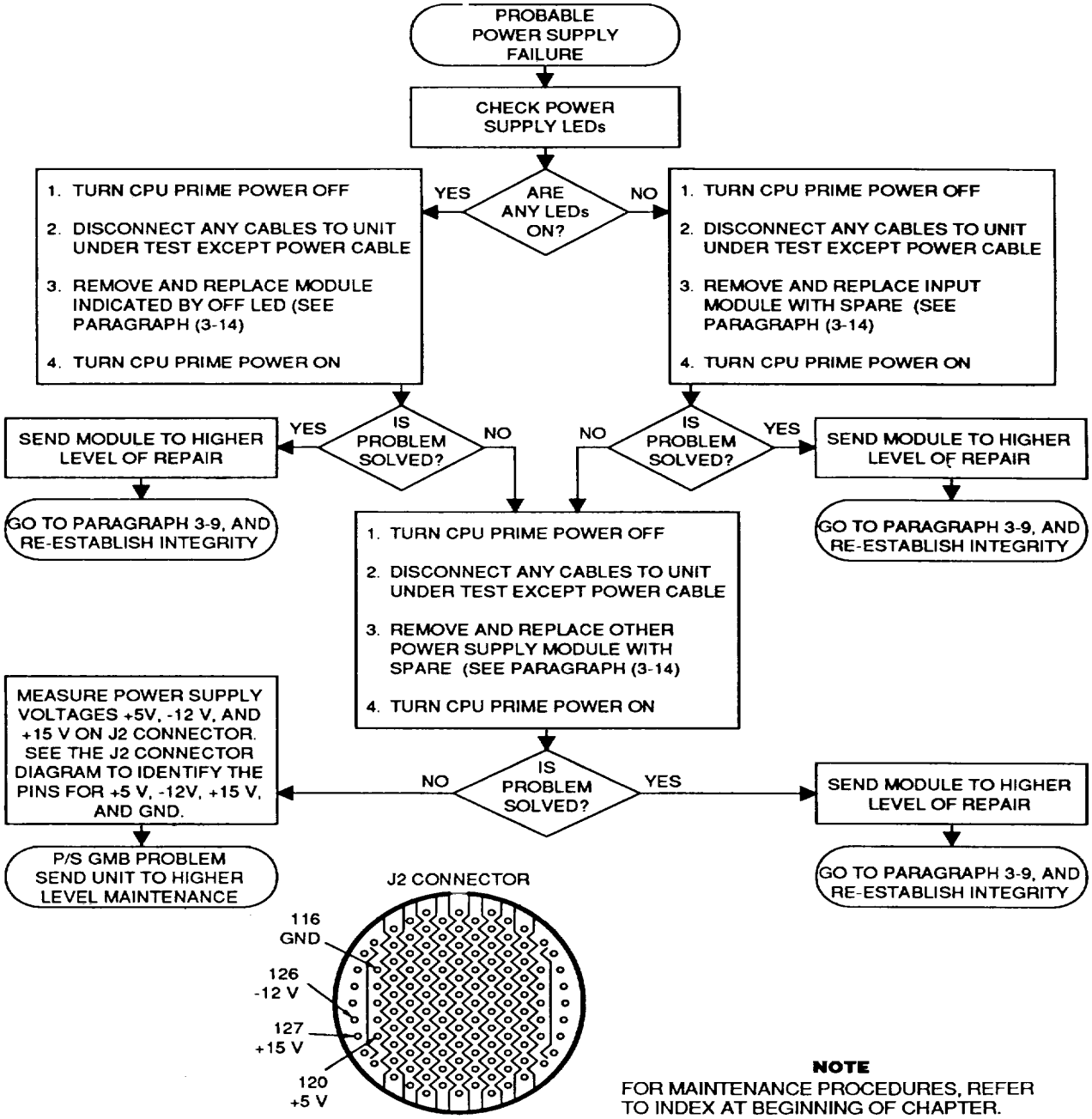
3-8. FLOWCHART DIAGNOSTICS (Cont.)

a. Unable to Boot CPU Diagnostic (Cont.)
(2) UNIBUS/Module Troubleshooting. (Cont.)



3-8. FLOWCHART DIAGNOSTICS (Cont.)

a. Unable to Boot CPU Diagnostic (Cont.)
(3) Power Supply Module Troubleshooting



3-9. RE-ESTABLISH INTEGRITY

INITIAL SETUP

Test Equipment	Equipment Condition
Computer Test Set, TS-4393/UYK-42(V)4, with cables W1 - W9, Diagnostic Software, 109D-C600-4.1, Cooling Kit and Torque Screwdriver Kit UNIBUS Terminator, 109D00320 Console, LA120-DA-WE or equivalent * Part of TS-4393/UYK-42(V)4	Equipment connected as shown in Test Setup Diagram. Power removed. Tools Tool Kit, TK-17. Torque Screwdriver* (2-36 inch. pounds) Work Station Static

CAUTION

This equipment contains electrostatic discharge sensitive (ESD) devices. Methods to be followed are specified in DOD-STD-1686 and DOD-Handbook-263.

Step 1. Return all good modules to their proper slots (Refer to paragraph 3-13.)

Step 2. Refer to paragraph 3-5 and run diagnostics to verify that problem is corrected.

Step 3. Zeroize Computer (paragraph 3-17).

Step 4. Check plug-in modules that have tested faulty (and have programmable switches) in accordance with paragraph 3-10. If module(s) prove faulty, send to higher level for repair.

Step 5. When testing is completed, reset switch (8) on S102 to the open position on the Multifunction Modules (A1A12A1) and Switch 5 on S2 on the Console IF (A1A13);otherwise, the Computer will not operate properly. Refer to paragraph 3-16 to verify switch settings.

3-9. RE-ESTABLISH INTEGRITY (Cont.)

Step 6. Turn off UUT power, Test Set power and Console power, and disconnect tested unit from test setup.

Step 7. Replace top cover assembly. (Refer to paragraph 3-12)

Step 8. Item repaired.

3-10. PROGRAMMABLE SWITCH CHECK

INITIAL SETUP

Tools
Tool Kit, TK-17
Workstation, Static
Torque Screwdriver * (2-36 in.lbs)

Equipment Condition
Module removed
(para. 3-13)

Materials/Parts
3/8 Inch Polyester
Film Tape, Two-Roll
Package, PN 853 (20318)

* Part of TS-4393/UYK-42(V)4

CAUTION

This equipment contains electrostatic discharge sensitive (ESD) devices. Methods to be followed are specified in DOD-STD-1686 and DOD-Handbook-263.

If suspect plug-in module has programmable switches, proceed as follows:

Step 1. Refer to paragraph 3-16 and verify correct programming. Correct switch settings if necessary.

Step 2. Move and reset each switch to help clean the contacts.

Step 3. Install module in accordance with paragraph 3-13.

3-10. PROGRAMMABLE SWITCH CHECK (Cont.)

Step 4. Test applicable unit in accordance with paragraph 3-5.

Step 5. If problem is not solved, remove module in accordance with paragraph 3-13 and send it to higher level maintenance for repair.

Step 6. Install known good module and test unit in accordance with paragraph 3-5.

SECTION III. SPECIALIZED REPAIR ACTIVITY (SRA) MAINTENANCE

3-11. GENERAL

a. Maintenance Philosophy

A faulty CPU is repaired by replacement of one or more plug-in modules; replacement of the UNIBUS terminator; replacement of the power supply modules; or replacement/repair of the transition harnesses.

All modules as well as the UNIBUS terminator must be sent to higher level maintenance repair.

This section contains SRA maintenance procedures for the CPU. The following items are discussed separately:

- Top Cover replacement
- Plug-in Module replacement
- Power Supply Module replacement
- Internal/Transition Harness replacement
- Programmable Switch settings

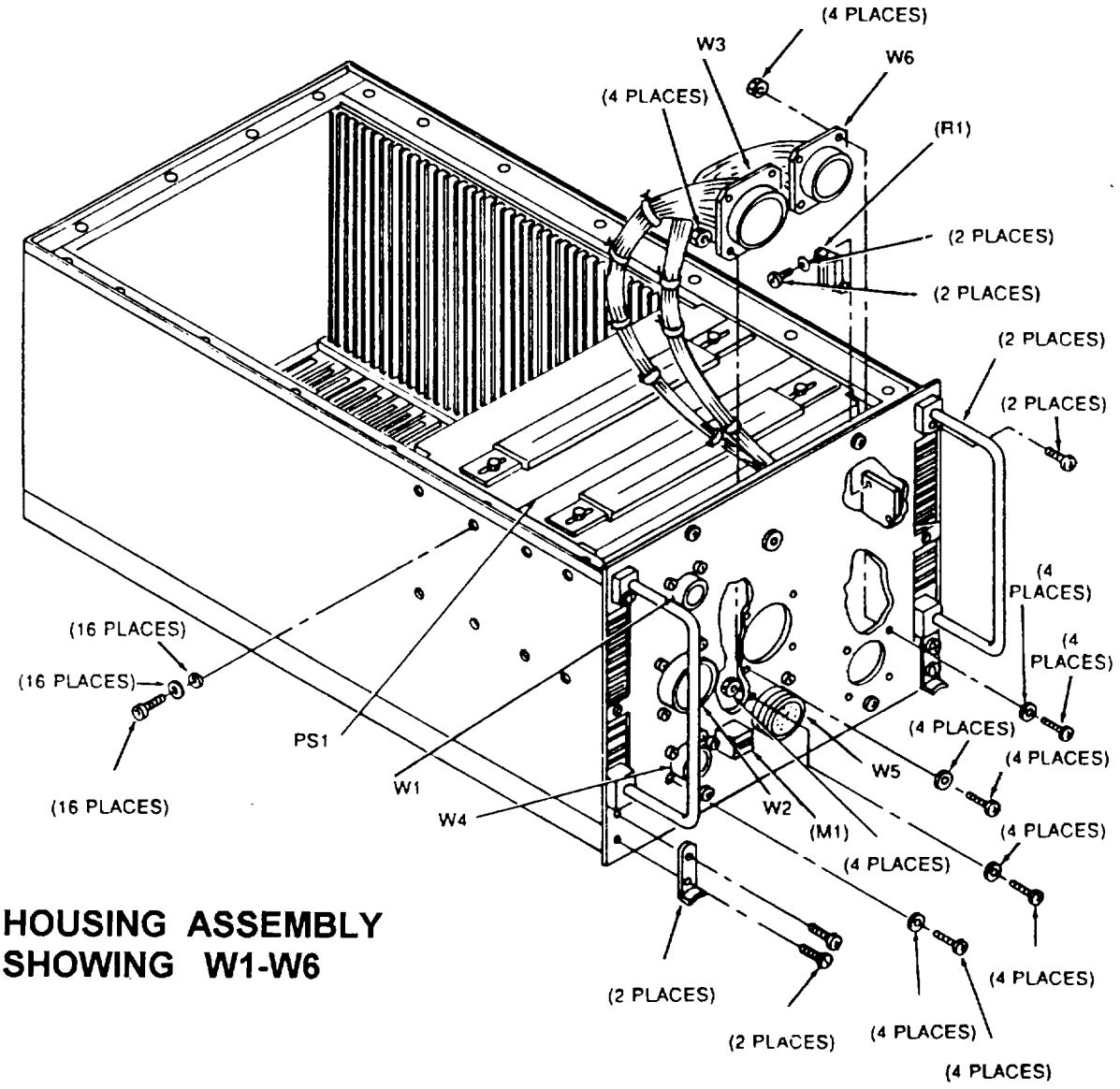
3-11. GENERAL (Cont.)

a. Maintenance Philosophy (cont.)

Disassembly of the CPU is limited to removal of the top and bottom covers, plug-in modules, power supply modules, and harness assemblies. The necessary step-by-step instructions are provided as part of the procedures for removing specific assemblies in paragraphs 3-12 through 3-15.

The location diagrams and cross-reference chart on this and the following pages show the layout of the unit and give complete identification and location information on all assemblies that are replaceable at the general support level.

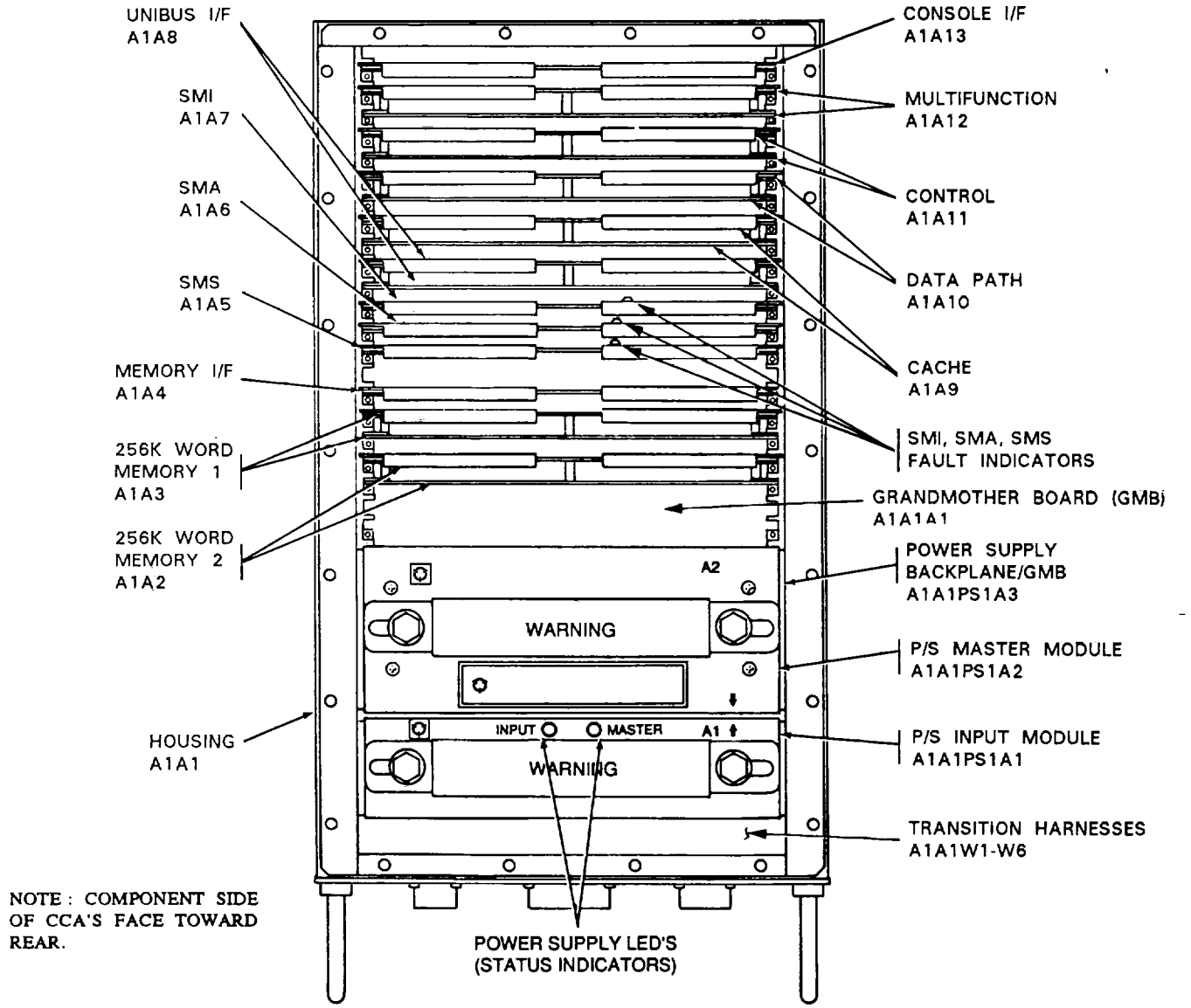
b. Location of Plug-in Modules and Major Assemblies.



HOUSING ASSEMBLY SHOWING W1-W6

3-11. GENERAL (Cont.)

b. Location of Plug-in Modules and Major Assemblies. (cont.)



CPU SHOWN WITHOUT TOP COVER

3-11. GENERAL (Cont.)

c. Assembly Cross-reference Chart

REF DES	SHORT NAME	PART NO	CATALOG NO.
A1A13	Console I/F	109D04302-202,-201*	M2-8408 (SPEC)
A1A12	Multifunction	109D04670-201	M2-8403 (SPEC)
A1All	Control	109D04304-202,-102*	M2-8402 (SPEC)
A1A10	Data Path	109D04480-401,-301*	M2-8404
A1A9	Cache	109D04520-201	M2-8405
A1A8	UNIBUS IF	A3028411**	M2-8406F
A1A7	SMI	A3028350	NA
A1A6	SMA	A3028351	NA
A1A5	SMS	A3028352	NA
A1A4	Memory I/F	109D04460-103,-302*	M2-8407
A1A3	256K word Memory 1	109D04878-201	M2-3009A(1)
A1A2	256K word Memory 2	109D04878-201	M2-3009A(2)
AlA1-PS1A3	P/S Backplane	A3086890, A3028418*	NA
AlA1-PS1A2	Master Module	A3028416	NA
AlA1-PSlA1	Input Module	A3028417	NA
AlA1	Housing Assembly	A3086889, A3028370*	NA
Al	CPU	A3028400	NA
A2	UBT	109D00320-203	NA

NOTE

Module part numbers are located on the identification label/plate only.

* Alternate configuration.
**P/N 109D08005-501 appears on module identification label/plate.

3-12. REPLACEMENT OF TOP COVER INITIAL SETUP

INITIAL SETUP

Tools
Tool Kit, TK-17
Workstation, Static
Material /Parts
Housing Assembly, A3086889 or, Housing Assembly, A3028370*

Equipment Condition
All power removed.

CAUTION

This equipment contains electrostatic discharge sensitive (ESDS) devices. Methods to be followed are specified in DOD-STD-1686 and DOD-Handbook-263.

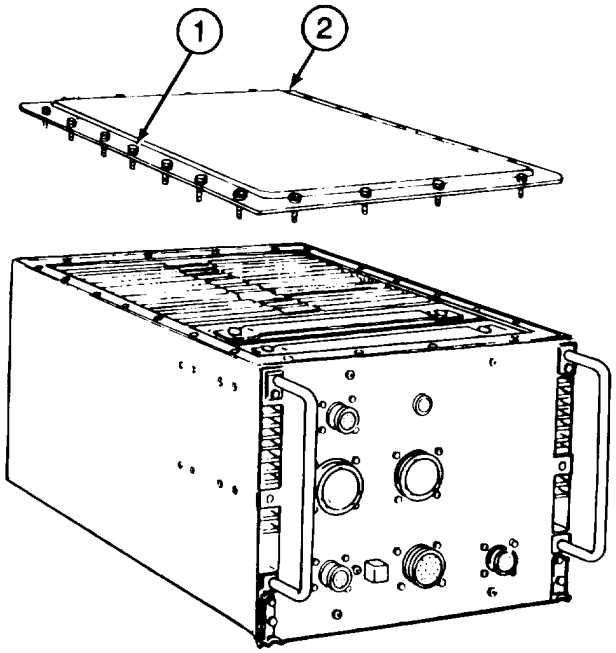
REMOVAL

Step 1. Loosen 22 captive screws G securing top cover and remove top cover .

REPLACEMENT

Step 2. Replace top cover Q on housing with marking TOP FRONT towards front panel connectors. Secure with 22 captive screws.

- Alternate configuration



3-13. REPLACEMENT OF PLUG-IN MODULES INTIAL SETUP

INITIAL SETUP

Tools
Tool Kit, TK-17
Torque Screwdriver
(supplied with
TS-4393/UYK-42(V)4)

Equipment Condition
All power removed.
Cover removed
(paragraph 3-12).

Material/Parts
256K Word Memory 1 and 2,
A1A3,A1A2, 109D04878-201
Memory I/F, A1A4, 109D04460-103
SMS, A1A5, A3028352
SMA, A1A6, A3028351
SMI,A1A7, A3028350

UNIBUS IF, A1A8, A3028411
Cache, A1A9, 109D04520-201

Material/Parts
Data Path, A1A10, 109D04480-401, or
Data Path, A1A10, 109D04480-301*
Control, A1A11, 109D04304-202,or
Control, A1A11, 109D04304-102*
Multifunction, A1A12, 109D04670-201
Console I/F, A1A13, 109D04302-202,or
Console I/F, A1A13, 109D04302-201*

CAUTION

This equipment contains electrostatic discharge sensitive (ESD) devices. Methods to be followed are specified in DOD STD 1686 and DOD Handbook 263.

REMOVAL

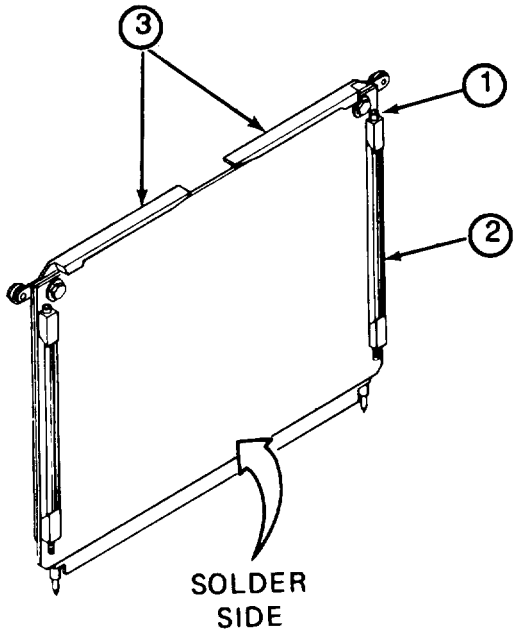
Step 1. Locate module to be removed. (Refer to paragraphs 3-ll.a. and b.).

Step 2. Use 3/32 hex on Torque Key and loosen all locking screws Q on all wedgelocks Q (two on memory modules and two chassis mount screws, four on other two-board modules and two on one- board modules) of board to be removed.

NOTE
Loosen screws no more than five turns, maximum.

*Alternate configuration

3-13. REPLACEMENT OF PLUG-IN MODULES (Cont.)



NOTE

Memory modules each have two chassis mounted card retainer screws in addition to two wedge-locks. Chassis mount screws must be loosened before removing memory modules.

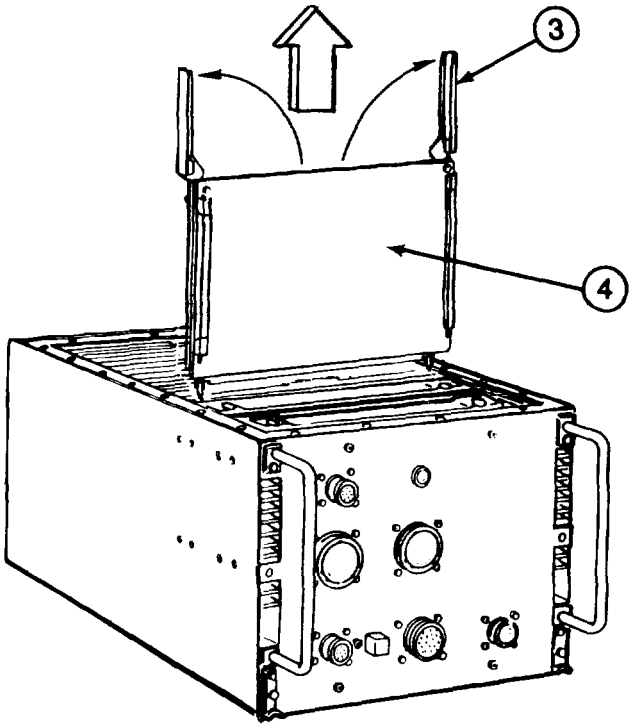
Step 3. Slowly swing both module extractor handles (3) to the open (vertical) position simultaneously.

3-13. REPLACEMENT OF PLUG-IN MODULES (Cont.)

Step 4. Grasp both module extractor handles (3) and carefully pull the module (5) upward until it clears module slots.

NOTE

If more than one module is removed, tag each module with its reference designation (e.g., AlA2, A1A3). This will help ensure that the module is reinstalled in the correct slot.



REPLACEMENT

Step 1. Refer to paragraph 3-11.a. and b. to determine proper slot. (Same as the old one if you just removed a faulty module.)

Step 2. Slide module (4) into guide slots (5) with component side toward rear.

Step 3. While supporting module with one hand, use tweezers (5) to guide wedgelocks (2) into guide slots .

3-13. REPLACEMENT OF PLUG-IN MODULES.(Cont.)

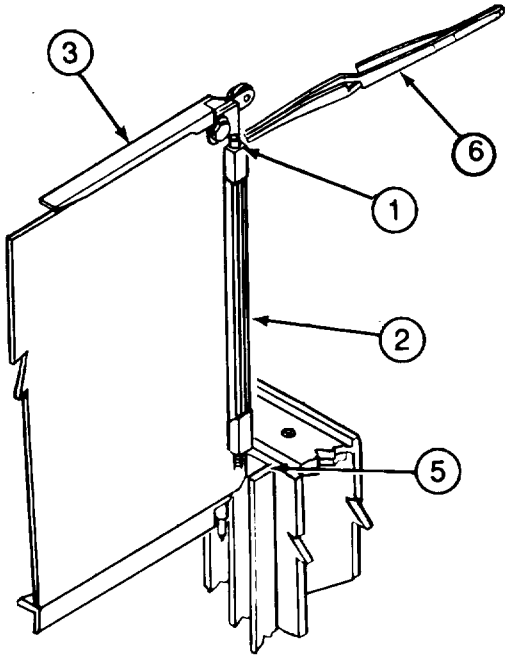
Step 4. Push down until rollers of module extractors (3) enter the guide slots (5).

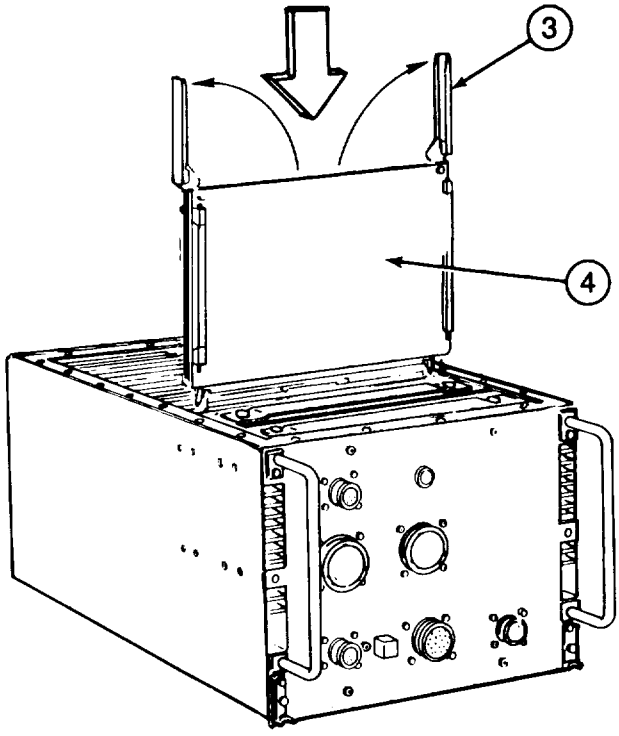
CAUTION

When performing next step, do not attempt to force module plug into its connector. If stiff resistance is met, remove module and check for bent pins or other obstruction. Clear obstruction, straighten pins, or replace module as necessary.

Step 5. Press module (4) down into guide slots (5).

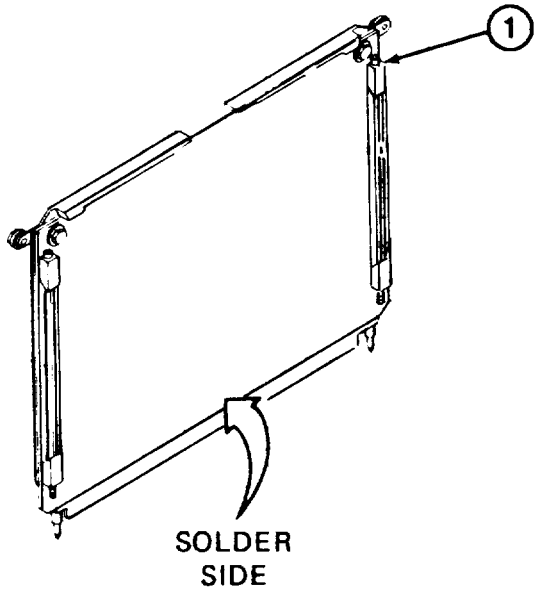
Step 6. Firmly press the extractor handles (3) down to closed (horizontal) position.





3-13. REPLACEMENT OF PLUG-IN MODULES.(Cont.)

Step 7. Tighten all locking screws (1) (two on one-board modules, two on memory modules and two chassis mount screws, and four on other two-board modules) to secure module. Torque locking screws (1) to 5.5 to 6.5 inch pounds and chassis mount screws to 1 to 2 inch pounds.



3-14. REPLACEMENT OF POWER SUPPLY MODULES.

INITIAL SETUP

Tools
Tool Kit, TK-17
Workstation, Static

Equipment Condition
All power removed.
Cover removed.

Materials/Parts
Master Module, A3028416
Input Module, A3028417

3-14. REPLACEMENT OF POWER SUPPLY MODULES.(Cont.)

CAUTION

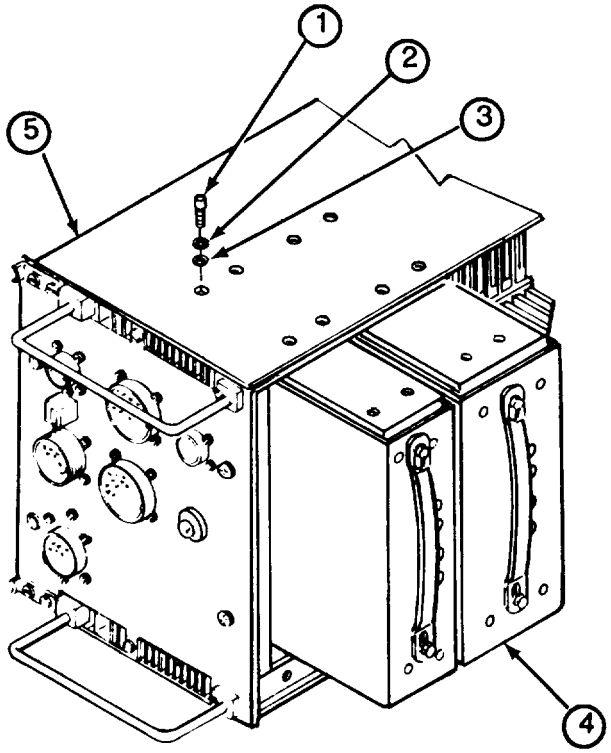
This equipment contains electrostatic discharge sensitive (ESDS) devices. Methods to be followed are specified in DOD STD 1686 and DOD Handbook 263.

REMOVAL

Step 1. Remove and retain eight (4 on each side) socket head screws (1), lockwashers (2), and flat washers (3) securing power supply module (4) on each side of housing (5)

Step 2. Turn unit on its side and grasp power supply module (4) strap handle and carefully slide power supply module (4) out of housing (5)

Step 3. Repeat steps 1. and 2. for other power supply module if necessary.



3-14. REPLACEMENT OF POWER SUPPLY MODULES.(Cont.)

REPLACEMENT

Step 1. Place housing (5) with top up.

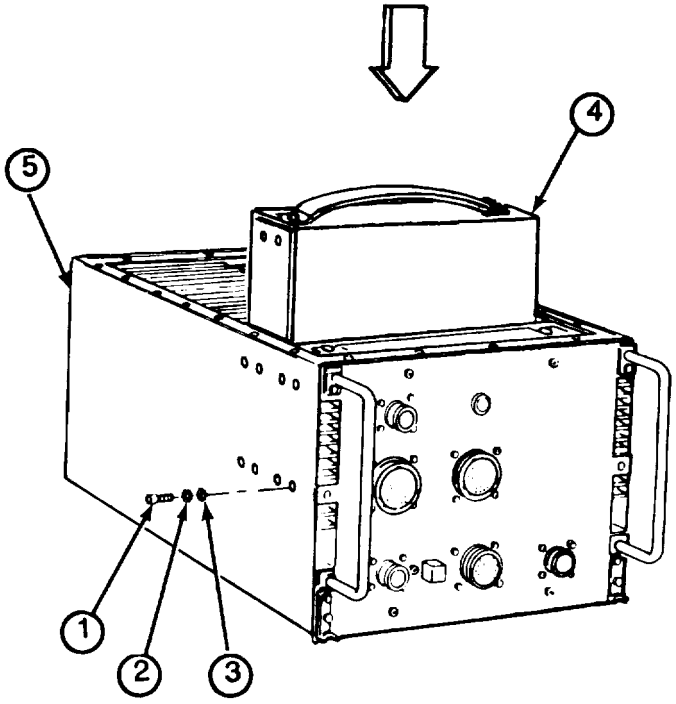
CAUTION

When performing next step, do not attempt to force module plug into its connector. If stiff resistance is met, remove module and check for bent pins or other obstruction. Clear obstruction, straighten pins, or replace module as necessary.

Step 2. Carefully slide power supply module (4) into housing (5) from the top so that the connector pins engage properly.

Step 3. Press power supply module (4) into housing and alternately secure with eight socket head screws (1), lockwashers (2), and flat washers (3) retained during removal. Once power supply module is properly in place tighten all screws.

Step 4. Repeat steps 2. and 3 for other module, if necessary.



3-15. REPLACEMENT OF INTERNAL CABLES THAT CONNECT TO FRONT PANEL CONNECTORS

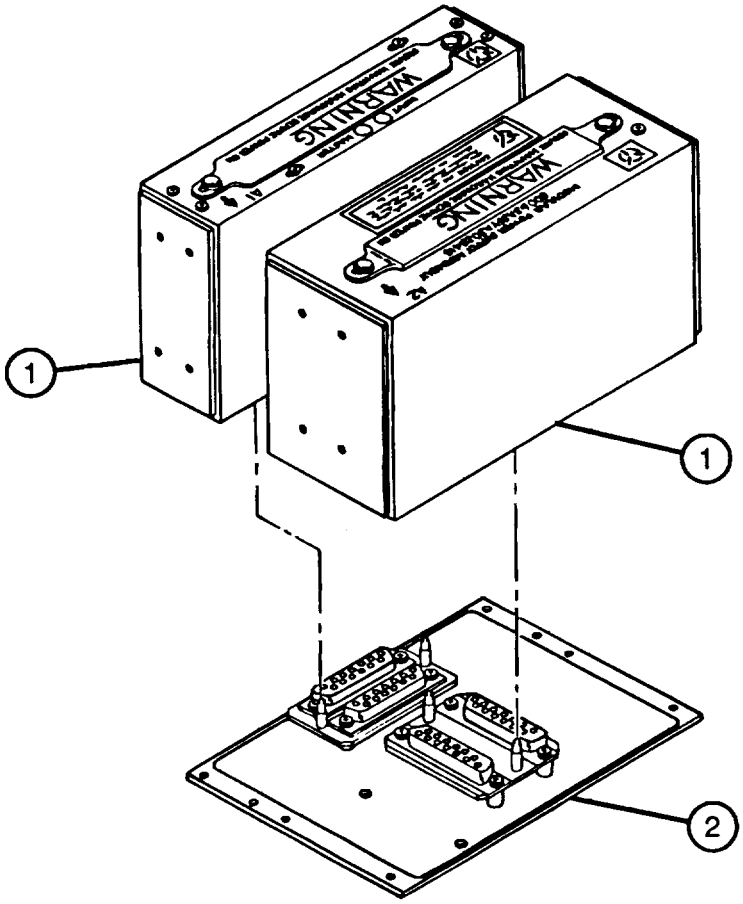
CAUTION

This equipment contains electrostatic discharge sensitive (ESDS) devices. Methods to be followed are specified in DOD STD 1686 and DOD Handbook 263.

REMOVAL

Step 1. Remove top cover. (Refer to paragraph 3-12.)

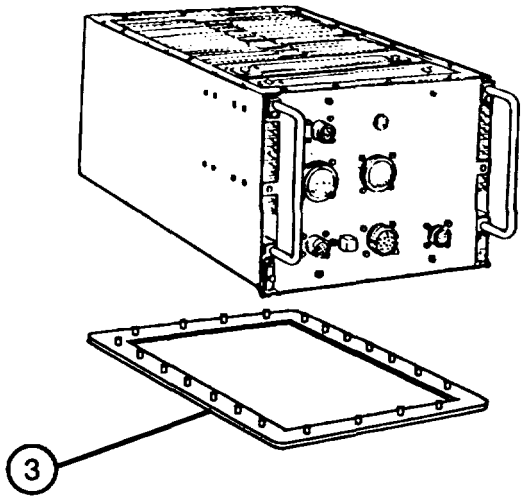
Step 2. Remove Power Supply Modules (1) from power supply backplane assembly (2) .(Refer to paragraph 3-14.)



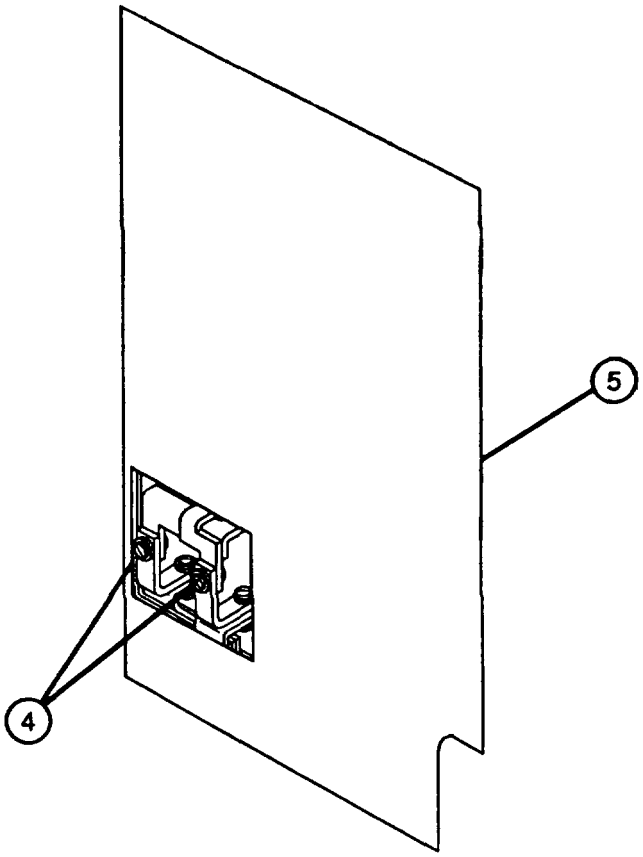
3-15. REPLACEMENT OF INTERNAL CABLES THAT CONNECT TO FRONT PANEL CONNECTORS (Cont.)

Step 3. Remove two Memory Boards. (Refer to paragraph 3-13.)

Step 4. Turn unit on side and remove bottom cover by loosening 22 captive screws (3)

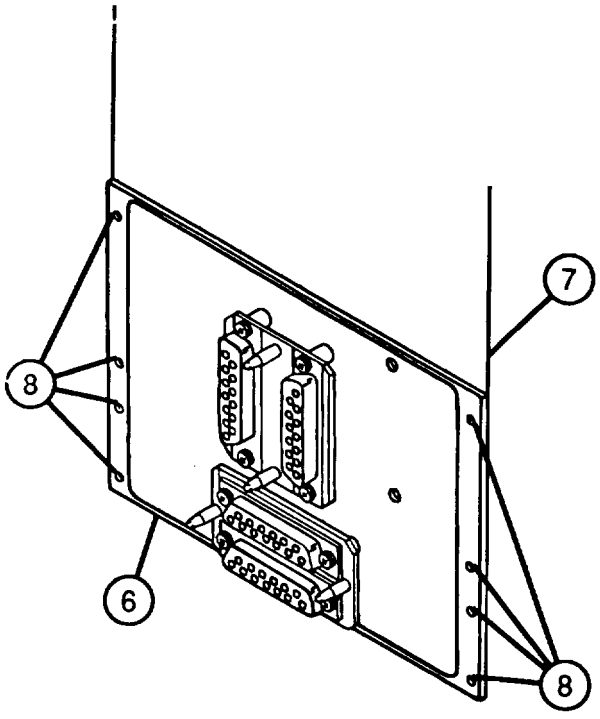


Step 5. Remove the two screws (4) that hold the power supply backplane assembly in place. These screws are accessed from the bottom side of the grandmother board (5).



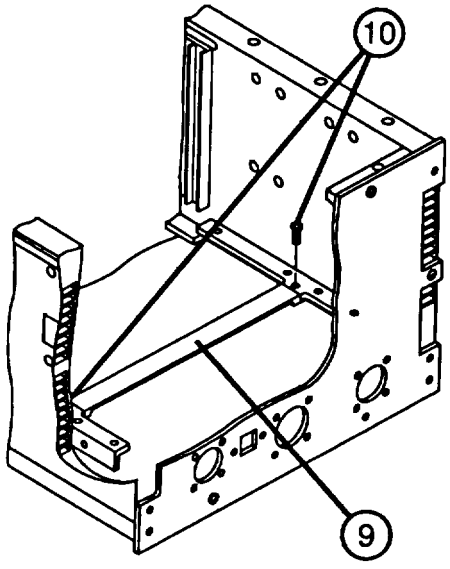
3-15. REPLACEMENT OF INTERNAL CABLES THAT CONNECT TO FRONT PANEL CONNECTORS (Cont.)

Step 6. Turn the unit upright and remove 8 screws (8) securing power supply backplane (6) to chassis (7).



Step 7. Swing back power supply backplane out of the way to access the internal cables. Secure in upright position with masking tape.

Step 8. Locate the stabilizer bar (9) that covers the cables. Remove the two counter sunk screws (10) that hold the bar in place, and remove the bar.

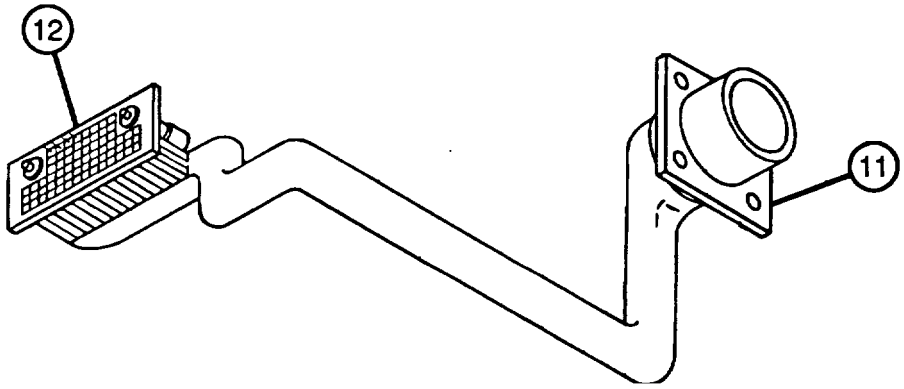


3-15. REPLACEMENT OF INTERNAL CABLES THAT CONNECT TO FRONT PANEL CONNECTORS (Cont.)

Step 9. Disconnect cable connectors from front panel by removing the self locking nuts (11) that attaches each cable connector to the front panel.

Step 10. Unseat connector by loosening captive mounting screws (12)

Step 11. Where required, cut the lacing cord on the cable to be removed so that the cable can be properly removed from the unit.



REPLACEMENT:

Step 1. Connect cable connectors (11) to front panel by replacing the self locking nuts that attaches each cable connector to the front panel.

Step 2. Seat connector by tightening captive mounting screws.

Step 3. Replace the stabilizer bar (9) by screwing two screws (10) that hold the bar in place.

Step 4. Swing back power supply backplane into place.

Step 5. Secure power supply backplane (6) by screwing in (8) screws.

Step 6. From the bottom of the unit, replace the two screws (4) that hold the power supply backplane in place.

NOTE
Use locktight on these two screws.

Step 7. Replace bottom cover by tightening 22 captive screws (3).

Step 8. Replace all Plug-In Modules. (Refer to paragraph 3-13.).

Step 9. Replace Power Supply Modules. (Refer to paragraph 3-14.)

Step 10. Replace top cover. (Refer to paragraph 3-12.)

3-16. PROGRAMMABLE SWITCH SETTING

INTIAL SETUP

Tools
Pointed Tool
Workstation, Static

Equipment Condition
All power removed.
Cover removed
(para. 3-12).
Module removed
(para. 3-13).

Material /Parts

256K Word Memory 2, A1A2, 109D04878-201
256K Word Memory 1, A1A3, 109D04878-201
Memory I/F, A1A4, 109D04460-103
UNIBUS IF, A1A8, A3028411
Cache, A1A9, 109D04520-201
Control, A1A11, 109D04304-202, or
Control, A1A11, 109D04304-102*
Multifunction Board A, A1A12A1, 109D04512-103, or
Multifunction Board A, A1A12A1, 109D04512-102*
Multifunction Board B, A1A12A2, 109D04513-102
Console I/F, A1A13, 109D04302-202, or
Console I/F, A1A13, 109D04302-201*

* Alternate configuration

CAUTION

This equipment contains electrostatic discharge sensitive (ESD) devices. Methods to be followed are specified in DOD-STD-1686 and DOD-Handbook-263.

Since signals on the UNIBUS are applied to all modules in parallel, certain modules must be pre-programmed so they will respond only to signals destined for that module. Dual-In-Line Package (DIP) switches are provided on the modules for this purpose. These switches, which resemble DIP microcircuits, contain 8 or 10 SPST switches each.

The tabulation following this paragraph lists CPU modules with programmable switches. Each switch is located, and the proper switch settings specified, in the succeeding illustrations. To set a programmable switch, proceed as follows:

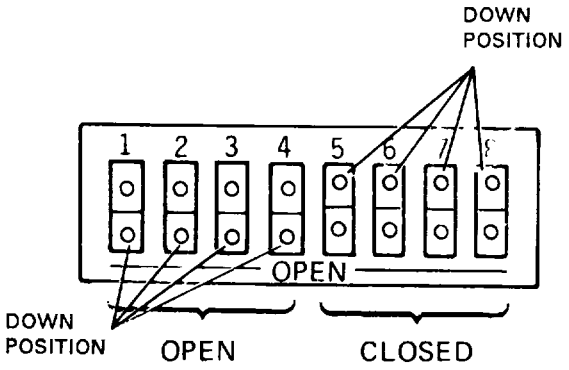
3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

Step 1. Remove and discard the tape (1) covering the dip switch to be programmed.

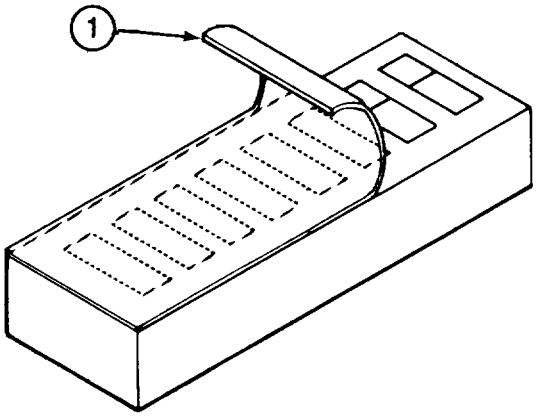
CAUTION

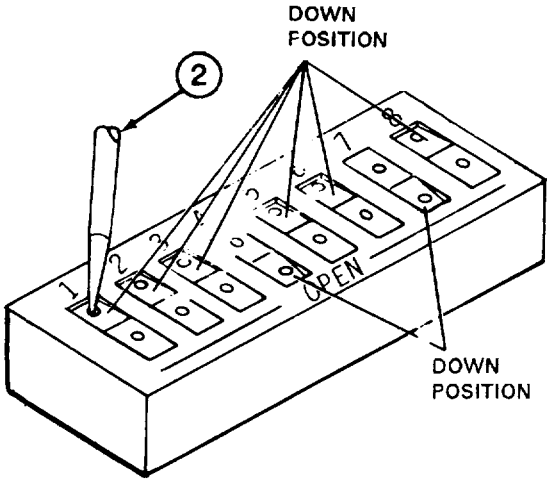
Do not use a pencil or ball point pen to perform the next step.

Step 2. Using a pointed tool (2), push each of the 8 or 10 rocker switches to its OPEN (marked) or closed (not marked) positions as specified in the appropriate illustration. The OPEN position provides a logic 1 and the closed position a logic 0.



LOGIC: 11110000





LOGIC: 00010010

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

Step 3. Cover the DIP switch with a new piece of tape, using polyester film tape, item 1, Appendix C.
Step 4. Repeat procedure for all DIP switches on the module being programmed.

NOTE

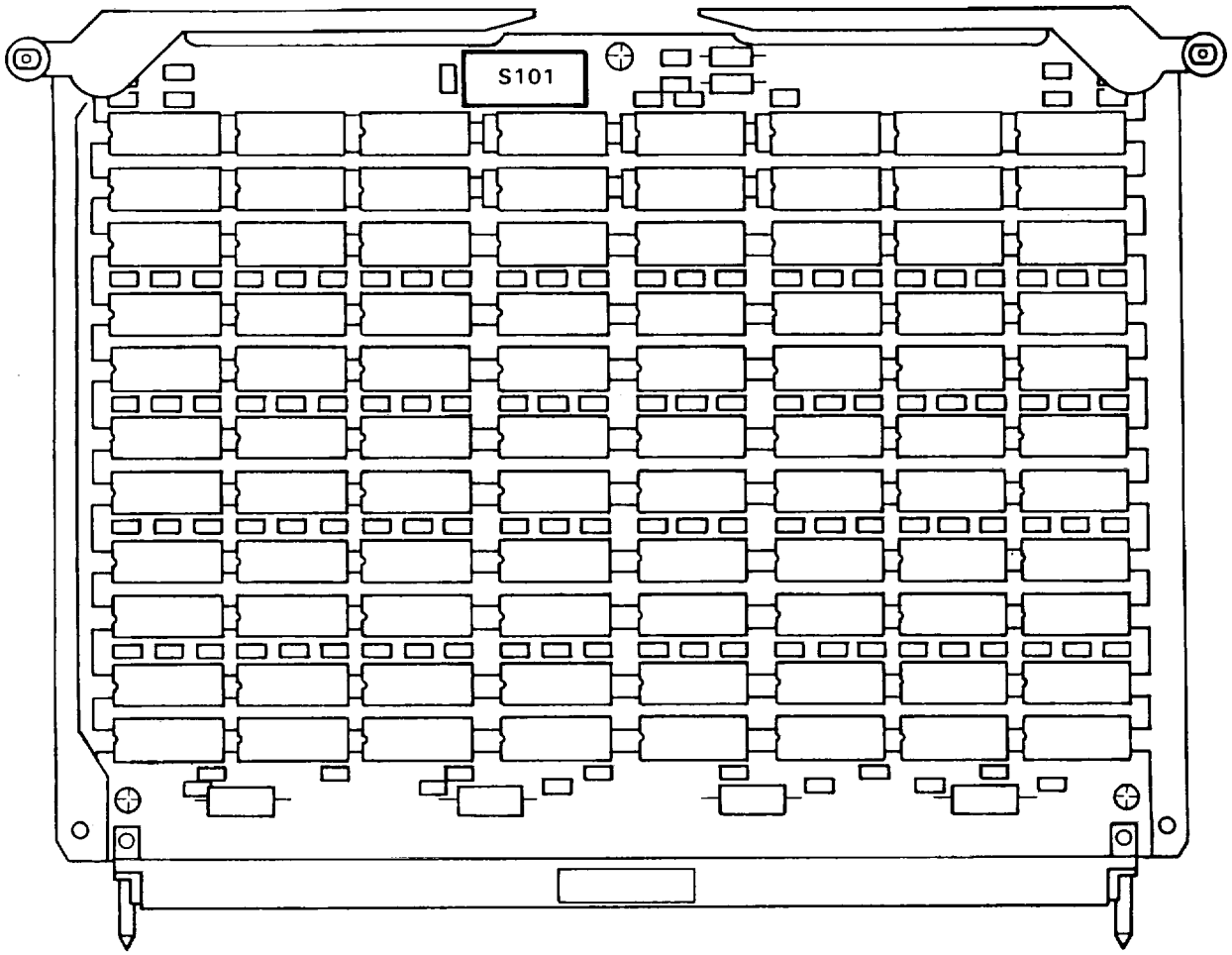
All programmable switches are accessible without disassembling the module except switch S201 on A1A12A2. That switch is located on board B of the two-board Multifunction module, and is hidden by board A. The necessary disassembly to gain access to this switch is not authorized at the SRA. If the module is still suspect after checking (and resetting if necessary) the three switches on board A, send the module to higher level maintenance for repair.

MODULES WITH PROGRAMMABLE SWITCHES

Reference Designation	Common Name
A1A2	256K Word Memory 2
A1A3	256K Word Memory 1
A1A4	Memory I/F
A1A8	UNIBUS IF
A1A9	Cache
A1A11	Control
A1A12A1 (BOARD A)	Multifunction A
A1A12A2 (BOARD B)	Multifunction B
A1A13	Console I/F

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

a. 256K Word Memories 1&2 (..A3 & A2) (109D04878-201)

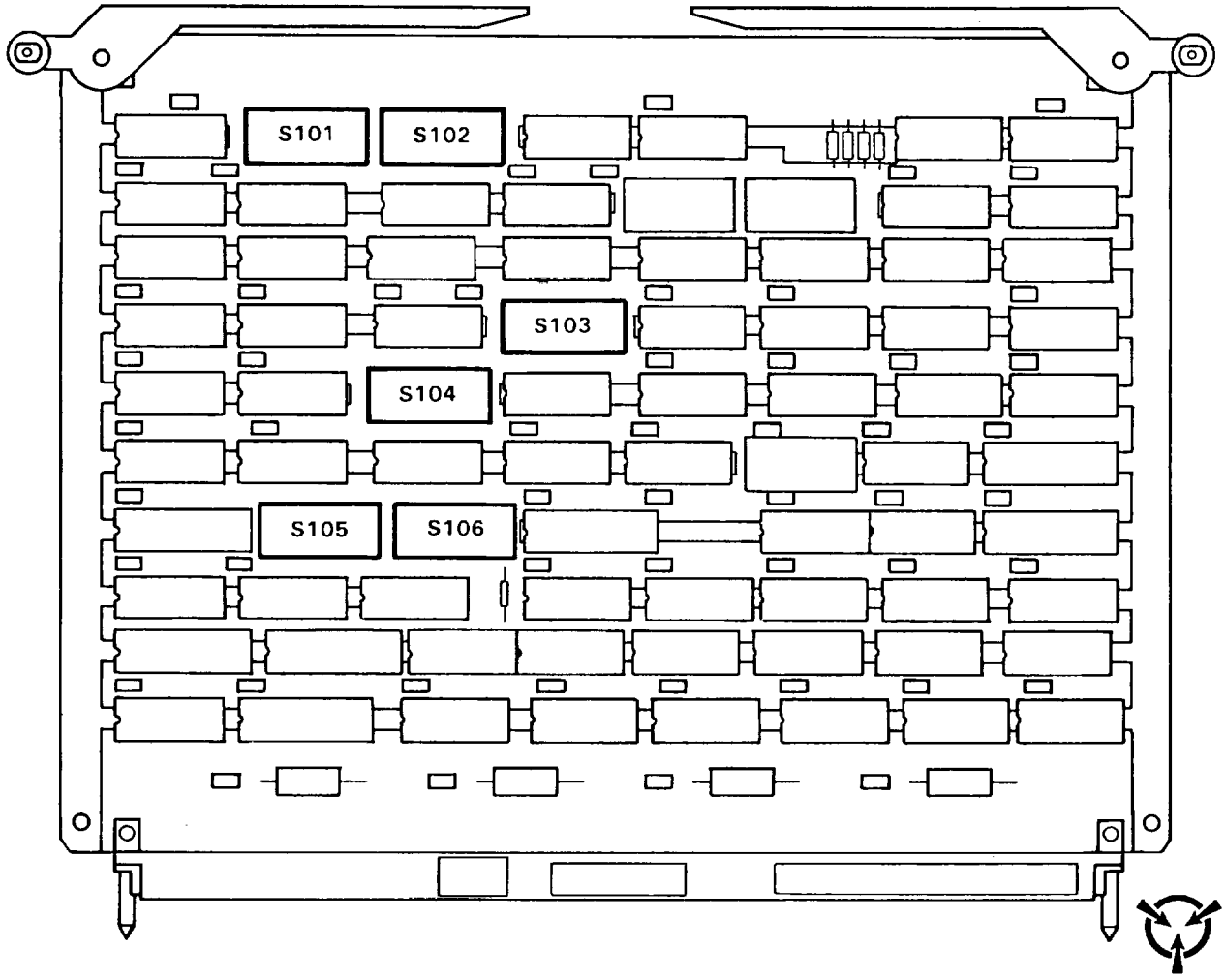


REFERENCE DESIGNATION	SWITCH SETTINGS S101
A1A3 (Memory 1)	00111011
A1A2 (Memory 2)	10111011

LEGEND: 1 = OPEN, 0 = CLOSED

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

b. Memory I/F (..A4) (109D04460-103)

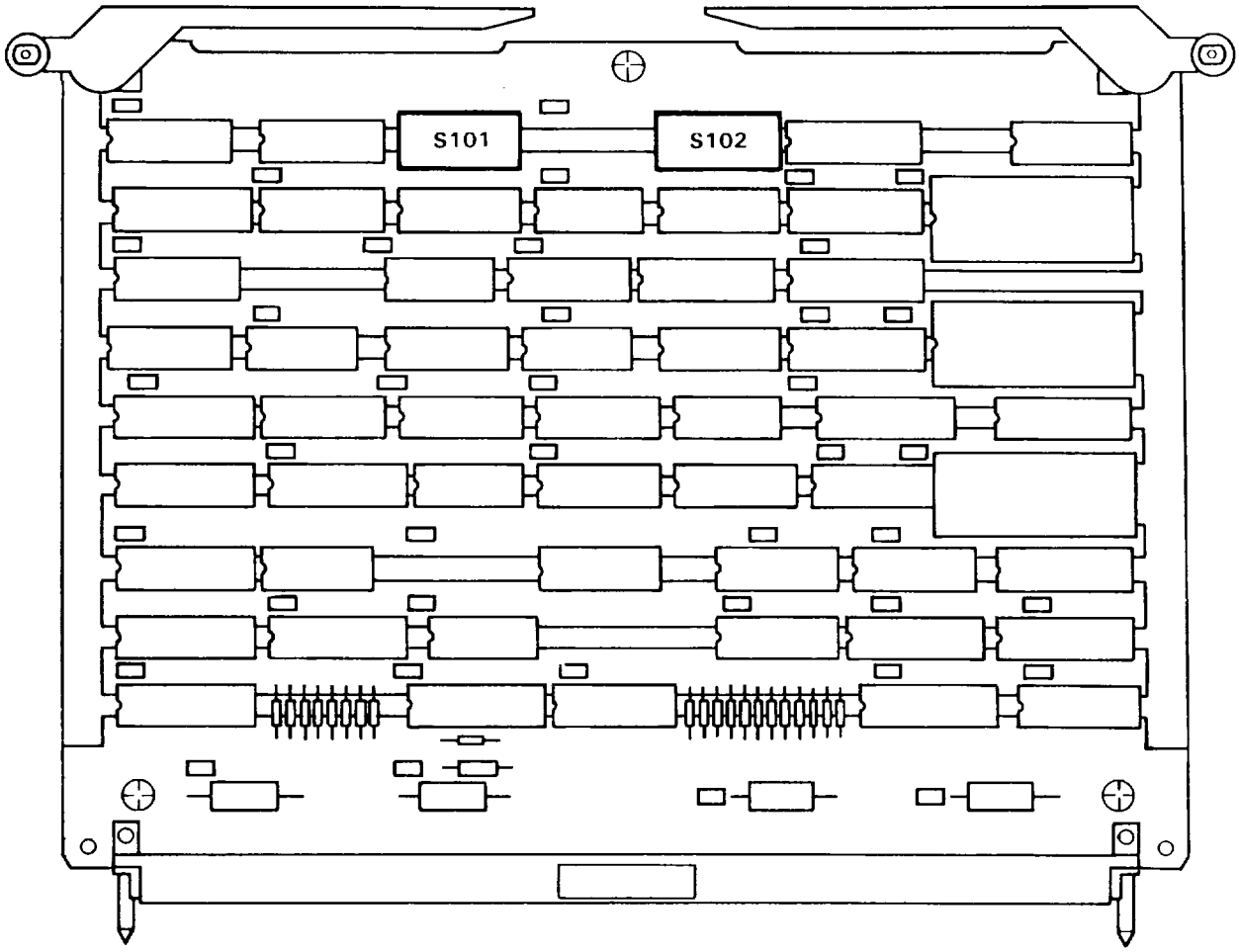


REFERENCE DESIGNATION	SWITCH SETTINGS					
	S101	S102	S103	S104	S105	S106
A1A4	01000000	11000111	01000000	01000000	00100000	00000000

LEGEND: 1 = OPEN, 0 = CLOSED

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

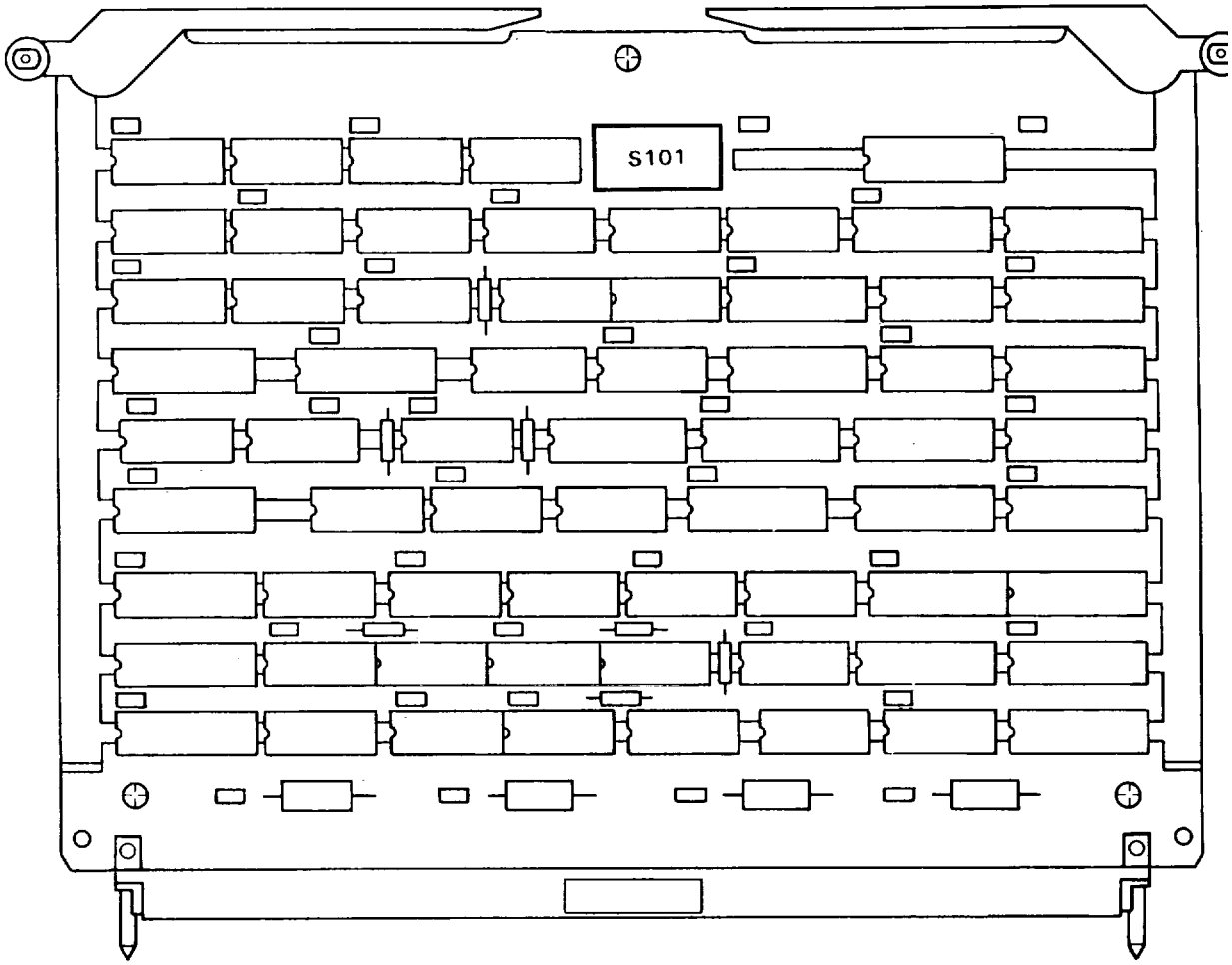
c. UNIBUS IF (..A8) (A3028411)



REFERENCE DESIGNATION	SWITCH SETTINGS	
	S101	S102
A1A8	10001111	11111100

LEGEND: 1 = OPEN, 0 = CLOSED

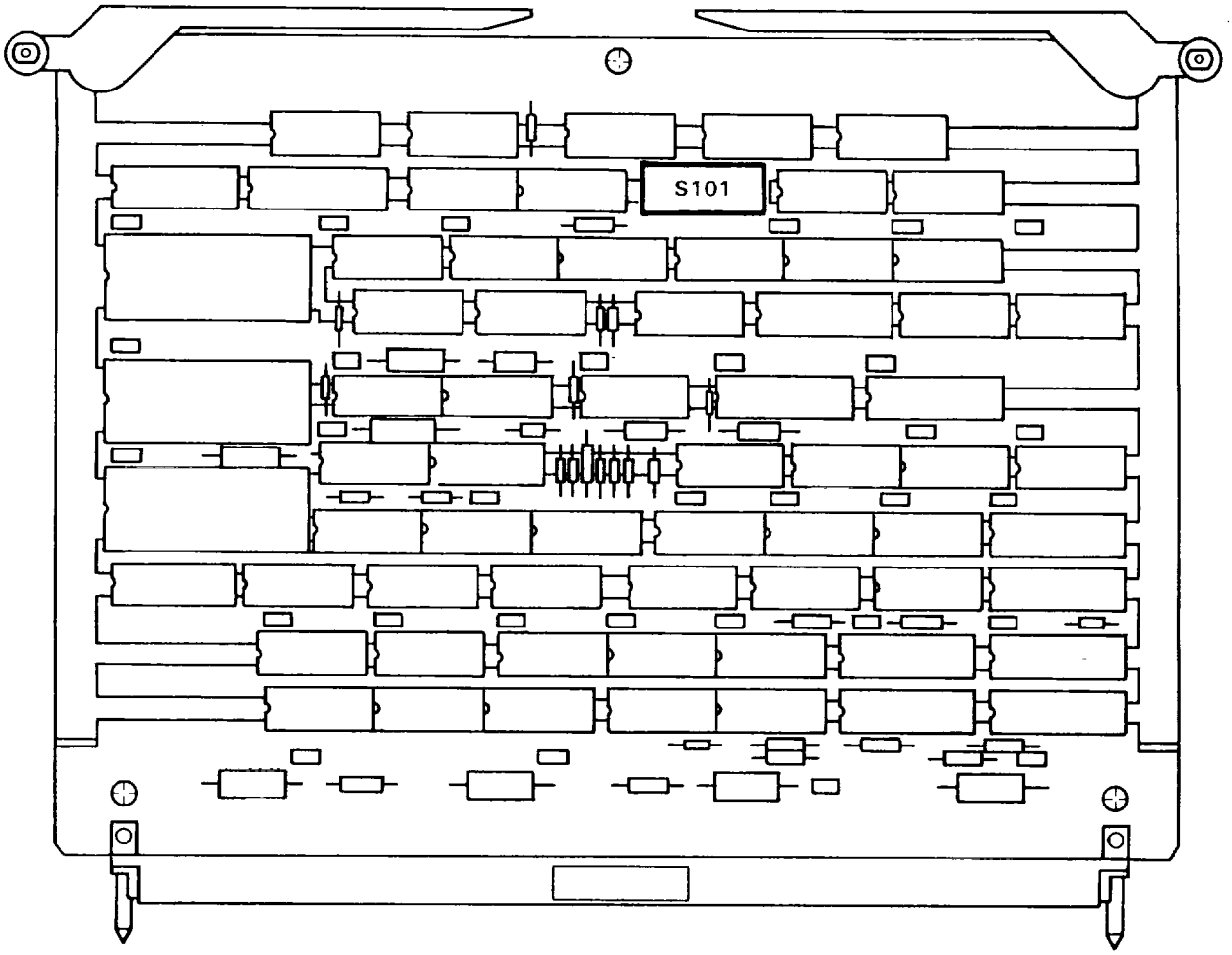
3-16. PROGRAMMABLE SWITCH SETTING (Cont.)
d. Cache (..A9) (109D04520-201)



REFERENCE DESIGNATION	SWITCH SETTINGS S101
A1A9	11111111

LEGEND: 1 = OPEN, 0 = CLOSED

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)
e. Control (..A11) (109D04304-202)

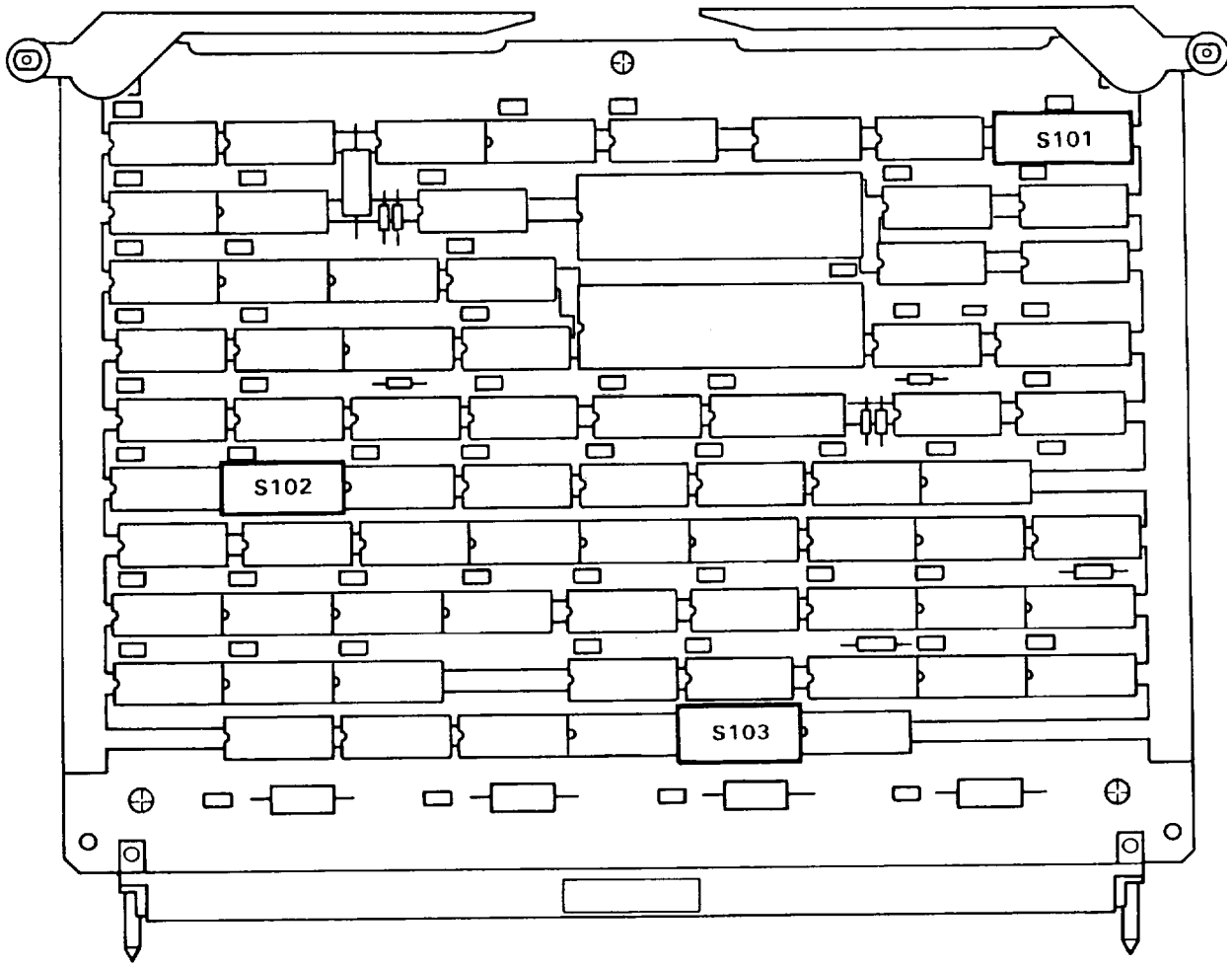


REFERENCE DESIGNATION	SWITCH SETTINGS S101
A1A11	01111111

LEGEND: 1 = OPEN, 0 = CLOSED

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

f. Multifunction A (..A12A1) Circuit Card Assembly



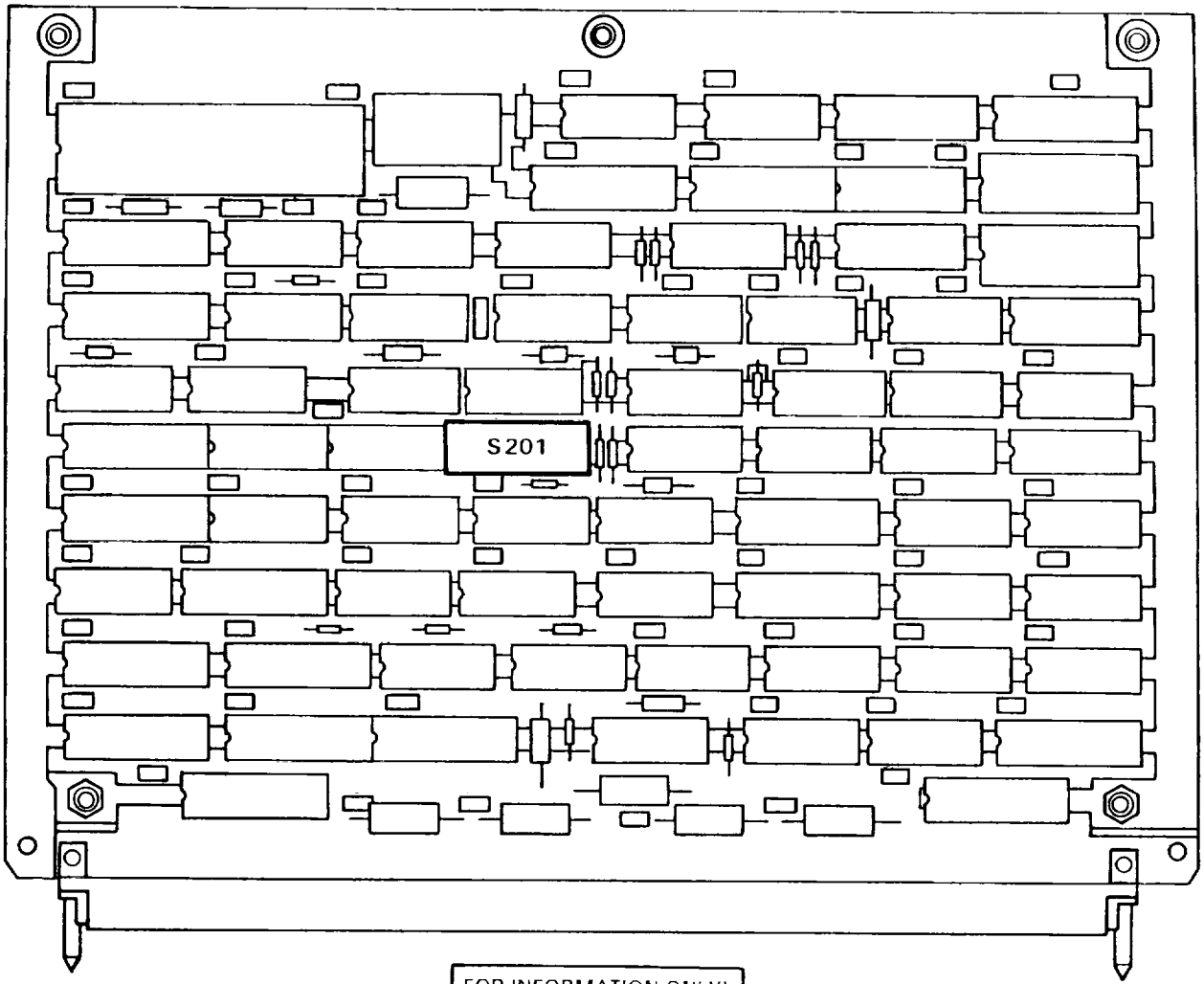
REFERENCE DESIGNATION	SWITCH SETTINGS		
	S101	S102	S103
A1A12A1	1110111011	11010111	01100111

LEGEND: 1 = OPEN, 0 = CLOSED

1→0 for test set-up only

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

g. Multifunction B (..A12A2) Circuit Card Assembly



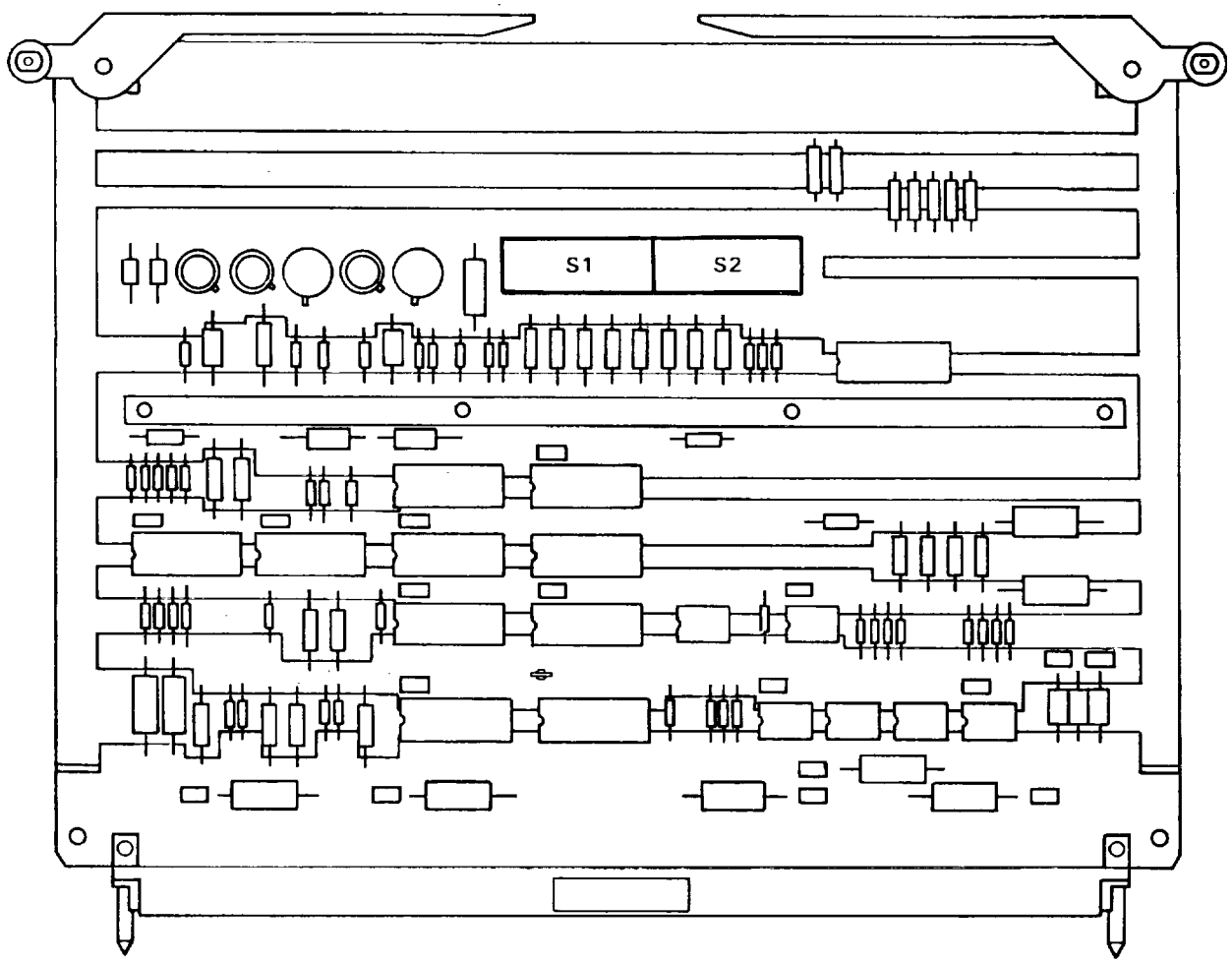
FOR INFORMATION ONLY! BOARD NOT ACCESSIBLE AT GENERAL SUPPORT LEVEL

REFERENCE DESIGNATION	SWITCH SETTINGS
	S201
A1A12A2	00101011

LEGEND: 1 = OPEN, 0 = CLOSED

3-16. PROGRAMMABLE SWITCH SETTING (Cont.)

h. Console I/F (..A13) (109D04302-202)



REFERENCE DESIGNATION	SWITCH SETTINGS	
	S1	S2
A1A13	1111111111	1100111111

LEGEND: 1 = OPEN, 0 = CLOSED

1→0 for test set-up only

SECTION IV. COMPUTER ZEROIZATION

3-17. ZEROIZATION OF THE COMPUTER

INITIAL SETUP

Test Equipment
Computer Test Set, TS-4393/UYK-42(V)4,
with cables W1 - W9,
Zeroization Software 109D-C600-5.0,
Cooling Kit and Torque Screwdriver Kit
UNIBUS Terminator, 109D00320
Console, LA120-DA-WE or equivalent

Equipment Condition
Equipment connected as shown in Zeroization Setup Diagram.

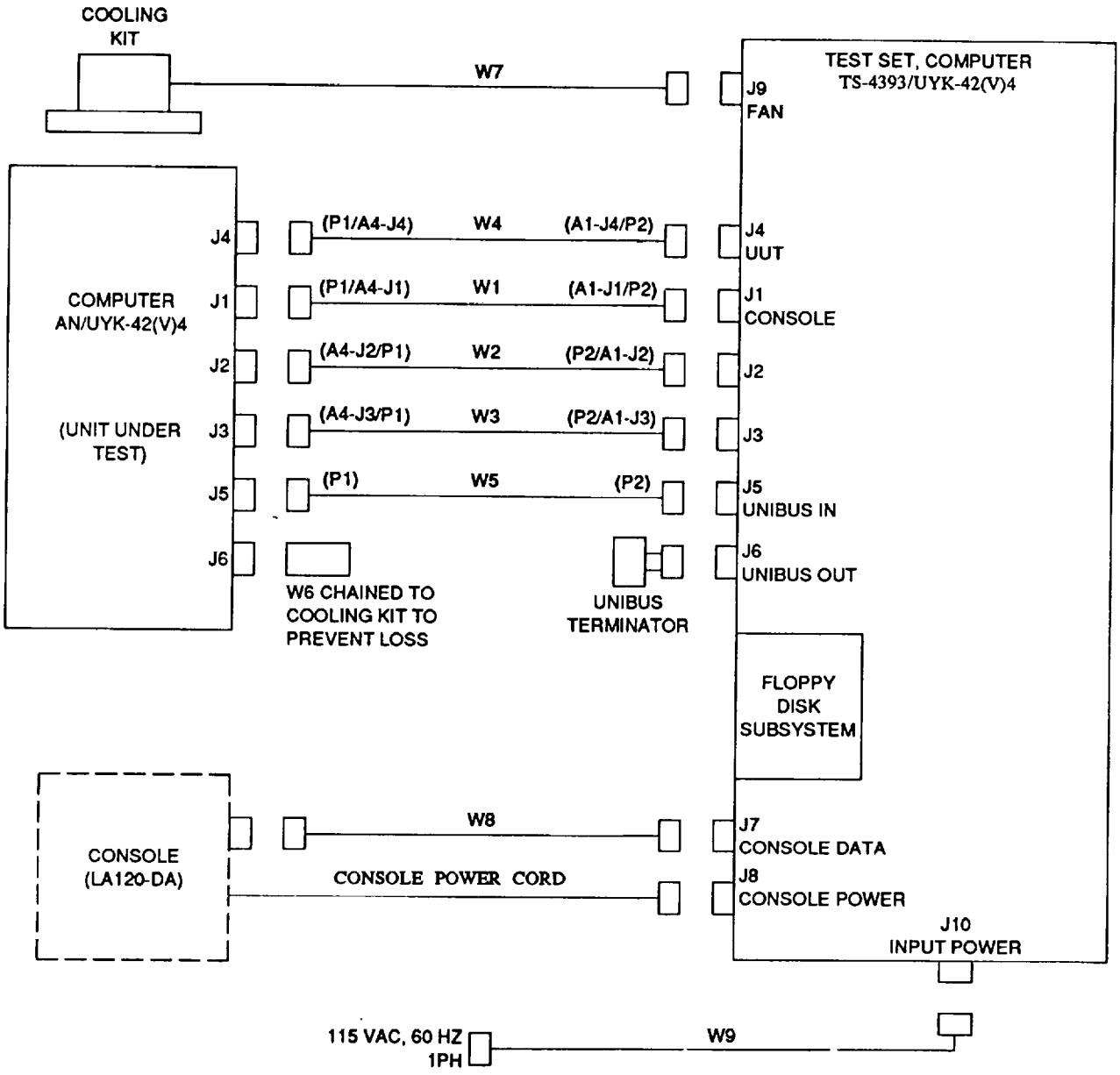
Tools
Tool Kit, TK-17.
Torque screwdriver*
(2-36 inch. lbs)
Work Station Static

* Part of TS-4393/UYK-42(V)4

NOTE

Alternate consoles can be utilized in place of the LA120-DA. The selected console must maintain the requirements of EIA specification RS-232-C. The part provides full duplex asynchronous communication on a 25 pin connector. Required pin numbers are defined in TM 11-6625-3268-14&P.

3-17.ZEROIZATION OF THE COMPUTER (Cont.)



ZEROIZATION SETUP DIAGRAM

ZEROIZATION SETUP DIAGRAM

3-17. ZEROIZATION OF THE COMPUTER (Cont.)

To erase the contents of the memory of computers returned for repair, proceed as follows:

1. Perform steps 1-13 of paragraph 3-5.

NOTE

System will not autoboot to run zeroing procedure. The console will print a console prompt ">>>" when the CPU is turned on.

2. Install zeroizing diskette 109D-C600-5.0 into disk drive "O" (left disk drive) and secure disk drive door.Using the Console, the operator must enter commands and respond to displayed prompts as indicated as follows:

3-17.ZEROIZATION OF THE COMPUTER (Cont.)

COMMAND P.NTER	DISPTLAYF.D RESUT.TS PROMPTS	OPERATOR RRSPONSE
<CTRL P> (simultaneously)	>>>	
H <CR>	>>>	

NOTE

If you type type a wrong key, type <CTRL P> to restart.

B DYO <CR>	>>>	
	The computer will respond by printing a series of messages and prompts on the console as follows: CLEARING MEMORY CHMDYCO XXDP+ DY MONITOR 28K BOOTED VIA UNIT 0 28K UNIBUS SYSTEM ENTER DATE (DD-MMM-YY) (DD-MMM-YY) <CR> RESTART ADDRESS: 152010 THIS IS XXDP+ TYPE "H" OR I"H/L" FOR HELP Respond to each prompt above as indicated until the prompt "." appears. Then type the following on the console.	
L ZERO.BIN <CR>		
	When the "." prompt appears for the second time.	
S 200 <CR>	The Sequence listed in Appendix F now prints out at the console while the zeroizing program is running and memory locations are cleared. When "NEW" = displays press <CR>	

3.If unable to boot and execute zeroing procedure (no printer output), the computer may be faulty. Proceed to para. 3-5, and perform the operational and fault isolation procedures for the CPU.

3-17. ZEROIZATION OF THE COMPUTER (Cont.)

4. If computer boots and zeroing runs, allow it to run for approximately two (2) hours until the completion is signaled by the messages in Appendix F.

NOTE

At this point the Computer will automatically run the zeroizations as listed in Appendix F. The Console will display/print test status, i.e. Memory type/location indicating a fully zeroized UUT. When the final message is displayed on the Console, the zeroization is complete.

5. When the zeroizing program is complete, the following sequence halts the computer so memory locations can be examined.

COMMAND ENTER	DISPLAYED RESULTS PROMPTS
<CTRL P> <CR>	Selects Console mode
H <CR>	Halts program

6. To examine a selected memory address locations in each segment for zeroization, type E 105020 <CR>.The zeroized address should print out as 177777 in each case. A list of other addresses to be checked to verify zeroization is given in Appendix G.

3-17. ZEROIZATION OF THE COMPUTER (Cont.)

NOTE

If a zeroize verification problem occurs, (i. e., the value read back is not what was expected, or the zeroizing procedure stops short), then one or all CCA's may contain classified data. This indicates that the UUT cannot be successfully zeroized, and must be repaired by cleared personnel. When the operator wants to restart the zeroize program, go to step 2.

NOTE

If a faulty CCA is the 256K Word Memory(AlA2 or A1A3), SMS(A1A5), SMA(A1A6), SMI(AlA7), Cache (A1A9), or Control(A1All); then that CCA must be treated as if it contains classified data and returned to the next higher repair level for fault isolation and repair. Applicable procedures for the handling and shipment of classified material must be followed.

7. Remove zeroizing diskette from Disk Drive "O". Return diskette to protective envelope and store in dust proof bag, away from heat or magnetic objects.

CAUTION

Once zeroization and any other testing is completed, both the Console I/F module (A1A13) and Multifunction assembly (A1A12) must be removed and switches S2 and S102 must be reset to their original position. Other- wise, the computer will not operate properly in the Terminal/System.

8. When testing is completed, reset rocker switch 8 on S102 on the Multifunction Module (A1A12) and rocker switch 5 on S2 on the Console I/F (A1A13); Otherwise, the computer will not operate properly in the Terminal/System.
9. Turn off UUT power, Test Set power and Console power.

APPENDIX A
REFERENCES

A-1. SCOPE

This appendix lists publications that are referenced in this manual that contain information applicable to the maintenance of the Computer, Digital, AN/UYK-42(V)4.

A-2. PUBLICATIONS

Air Force Equipment Improvement Recommendations ..... AFR 900-4

Air Force Equipment Maintenance ..... AFR 66-1

Compromising Emanations Laboratory Test ..... NACSEM 5100
Standards/Electro-Magnetics

Consolidated Index of Army Publications and ..... DA Pam 25-30
Blank Forms

Department of the Army Maintenance Forms ..... DA Pam 738-750

Depot Maintenance Work Requirement for ..... DMWR 11-5895-1207
AN/UYK-42 (V) 3

Discrepancy in Shipment Report (DISREP) ..... SF 361

Electrostatic Discharge Control Handbook DOD-HDBK-263
for Protection of Electrical and
Electronic Parts, Assemblies, and
Equipment (excluding Electrically-
Initiated Explosive Devices)

ESD Control Program for Protection of DOD-STD-1686
Electrical and Electronic Parts,
Assemblies, and Equipment

Expendable Items (Except Medical Class V, Repair ..... CTA 50-970
Parts, and Heraldic Items)

A-2. PUBLICATIONS (Cont.)

General Support Maintenance Repair ..... Army TM 11-5895-1207-40P
Parts and Special Tools ..... Navy EE610-BA-PLG-010/E120-UYK42(V)3
List (Including Depot Maintenance ..... AF TO 31S5-2UYK42-44
Repair Parts and Special Tools) for
Computer, Digital AN/UYK-42(V)3
General Support Maintenance Manual ..... Army TM 11-5895-1207-40
for Computer, Digital ..... Navy EE610-BA-MMA-010/E120-UYK-42V3
AN/UYK-42(V)3 ..... AF TO 31S5-2UYK42-42
(NSN 7021-01-181-2483)
General Support Maintenance Repair ..... Army TM 11-5895-1308-40P
Parts and Special Tools ..... Navy EE610-HD-PLD-010/WllO-UYK42(V)4
List (Including Depot Maintenance ..... AF TO 31S5-2UYK42-54
Repair Parts and Special Tools) for
Computer, Digital AN/UYK-42(V)4
Maintenance Data Collection System ..... AFM 66-267
Operators and Unit Maintenance Manual for ..... Army TM 11-5895-1218-12
Communications Terminals ..... Navy EE150-LQ-QMI-010/W110-179V1
AN/TRC-179(V)l & AN/TRC-179(V)3 ..... AF TO 31R2-2TRC179-21
Operators, Unit, Direct Support and ..... Army TM 11-6625-3268-14&P
General Support Maintenance ..... Navy EE133-CA-OMI-010/TS-4293UYK-42(V)4
Manual Including Repair Parts ..... AF TO 33D7-3-336-1
and Special Tools List for
Test Set, Computer TS-4393/UYK-42(V)4
Preparation for Storage or Shipment ..... TM 740-90-1
Procedure for Destruction of Electronic Material ..... TM 750-244-2
to Prevent Enemy Use
Quality Deficiency Report ..... SF 368
Recommended Changes to Publications and Blank ..... DA Form 2028
Forms
Report of Discrepancy (ROD ..... SF 364
Technical Order System Publication Improvement ..... AFTO Form 22
Unsatisfactory Equipment Reporting ..... TO 00-35D-54

APPENDIX B
MAINTENANCE ALLOCATION CHART

Section I. INTRODUCTION

B-1. GENERAL

This appendix provides a summary of the maintenance operations for the Computer, Digital AN/UYK-42(V)4. It authorizes levels of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

B-2. MAINTENANCE FUNCTION

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i. e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counter

i. Repair. The application of maintenance services (inspect, test, service, replace) or other maintenance actions to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part subassembly, module (component or assembly), end item, or system. This function include the trial and error replacement of running spare type items such as fuses and lamps.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

B-3. COLUMN ENTRIES

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4. Maintenance Level. Column 4 specifies, by the listing of a work time figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that mainte-

nance function at the indicated level of maintenance. If the number or complexity of the tasks within the listed maintenance function vary at different maintenance levels, appropriate work time figures will be shown for each category. The number of task-hours specified by the work time figure represents the average time required to restore an item (assembly, subassembly, component, module, end item, or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

UNIT
C - Operator/Crew
0 - Organizational/Unit
INTFRMEDIATE
F - Direct Support
H - General Support
DEPOT
L - Special Repair Activity
D - Depot

e Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

B-4. TOOL AND TEST EQUIPMENT REQUIREMENTS (SECT. III)

e. Tool or Test Equipment Reference Code. The numbers in this column coin the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Level. The codes in this column indicate the maintenance level allocated to tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

B-5. REMARKS (SECT. IV)

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

SECTION II MAINTENANCE ALLOCATION CHART
FOR
AN/UYK-42 (V)4

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL UNIT C	UNIT O	INTERMEDIATE F	INTERMEDIATE H	DEPOT D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
00	COMPUTER, DIGITAL	REPLACE		0.1					
	AN/UYK-42(V)4	TEST		0.1					A,B
	(A3023763)	TEST				L(1.5)		1,11,12,23	C,D,H
		REPAIR				L(1.0)		2-5,23	C,D,H
		TEST				3.5		1,11,12, 22	H
		REPAIR					3.0	2-5,14,23	H
01	CENTRAL PROCESSING	REPLACE				L(0.05)			
	UNIT ASSEMBLY AI	TEST				L(1.5)		1,11,12,23	B,C,D,H
	(A3028400)	REPAIR				L(1.0)		2-5,23	B,C,D,H
		TEST					3.5	1,11,12, 22	H
		REPAIR					3.0	2-5,14,23	H
0101	HOUSING ASSEMBLY A1AI	TEST					2.0	9,10,11,22	H
	(A3086889)	REPAIR					1.0	5,14,23	H
010101	GRANDMOTHER CIRCUIT CARD	REPLACE					1.0	5,23	H
	ASSEMBLY (A3086887) AIA1A1	TEST					1.0	9,10,11,22	B,H
		REPAIR					1.5	14,23	H
010102	POWER SUPPLY, MODULE	TEST				L(1.0)		1,11,12	B,H,I
	(A3028415) A1AIPS1	TEST					1.0	53,57-61	H
		REPAIR				L(1.0)		5,23	B,H,I
		REPAIR					1.5	5,23	H
01010201	INPUT BASIC MODULE	REPLACE				L(0.2)		2,3,5,23	D,H
	(A3028417) AIAIPS1A1	TEST					2.0	53,57-62	H
		REPAIR					2.0	5,14,23	H
0101020101	LINEAR BIAS ASSEMBLY	TEST					X		B
	(A3087172) A1A1PS1A1A4	REPAIR					X		B
01010201011	CIRCUIT CARD ASSEMBLY	REPLACE					0.5	5,23	H
	(A3087054) A1A1PS1AIA4A2	TEST					x		B
		REPAIR					x		B
01010201012	CIRCUIT CARD ASSEMBLY	REPLACE					0.5	5,23	H
	(A3087056) AIA1PS1A1A4A1	TEST					x		B
		REPAIR					X		B
0101020102	HOUSEKEEPING ASSEMBLY	TEST					X		B
	(A3087231) A1A1PS1A1A3	REPAIR					X		B
01010201021	CIRCUIT CARD ASSEMBLY	REPLACE					0.5	5,23	H
	(A3087079) 1AIAPSIAIA3A1	TEST					X		B
		REPAIR					X		B
01010202	MASTER BASIC MODULE	REPLACE					L(0.2)	2,3,5,23	D,H
	(A3028416) A1A1PSIA2	TEST					2.0	53,57-62	H
		REPAIR					2.0	5,14,23	H
0101020201	REGULATOR-I ASSEMBLY	TEST					X		B
	(A3087243) A1A1PSIAA2A	REPAIR					X		
01010202011	CIRCUIT CARD ASSEMBLY	REPLACE					1.0	5,23	B,H
	(A3087064) AIA1PSIA2A2A2	TEST					X		B
		REPAIR					X		B
01010202012	CIRCUIT CARD ASSEMBLY	REPLACE					1.0	5,23	H
	(A3087067) A1AIPSiA2AZA1	TEST					X		B
		REPAIR					X		B
0101020202	POWER REGULATOR-I ASSEMBLY	TEST					X		B
	(A3087219) A1AIPSIAZA7	REPAIR					x		B

• Alternate Configuration

NV-15-102-101
110686

SECTION II MAINTENANCE ALLOCATION CHART
FOR
AN/TYK-42(V)4

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL UNIT C	UNIT O	INTERMEDIATE F	INTERMEDIATE H	DEPOT D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
0101020203	POWER REGULATOR-II ASSEMBLY	TEST					X		B
	A3087244) A1A1PS1A2A3	REPAIR					X		B
01010202031	CIRCUIT CARD ASSEMBLY	REPLACE					1.0	5,23	H
	(A3087065) A1AIPS1A2A3A1	TEST					X		B
		REPAIR					X		B
01010202032	CIRCUIT CARD ASSEMBLY	REPLACE					1.0	5,23	H
	(A3087068) AlA1PS1A2A3A2	TEST					x		B
		REPAIR					X		B
0101020204	CIRCUIT CARD ASSEMBLY	REPLACE					1.0	5,23	H
	(A3087060) AlA1PS1A2A6	TEST					X		B
		REPAIR					X		B
0101020205	CIRCUIT CARD ASSEMBLY	REPLACE					1.0	5,23	H
	(A3087062) AlAlPSlA2A5	TEST					x		B
		REPAIR					X		B
0101020206	CIRCUIT CARD ASSEMBLY-5V DRIVE	REPLACE					1.0	5,23	H
	(A3087069) AlA1PSlA2A4	TEST					X		B
		REPAIR					X		B
01010202061	CIRCUIT CARD ASSEMBLY	TEST					X		B
	(A3087075) AlA1PS1A2A4A1	REPAIR					X		B
		REPLACE					1.0	5,23	H
01010202062	CIRCUIT CARD ASSEMBLY	TEST					X		B
	(A3087077) A1A1PSlA2A4A2	REPAIR					X		B
		REPLACE					1.0	5,23	H
01010203	BACKPLANE ASSEMBLY	REPLACE					1.0	5,23	F,H
	(A3086890) A1AIPS1A3	TEST					1.0	9,10,22	B
010103	SYSTEM CONSOLE HARNESS	REPLACE				L(0.5)		5,23	D
	ASSEMBLY (A3028396) A1A1W1	TEST				L(O.2)		11	D
		REPAIR				L(l.0)		5,23	D
010104	I/O-A HARNESS ASSEMBLY	REPLACE				L(0.5)		5,23	D
	(A3028422) A1AlW2	TEST				L(O.2)		11	D
		REPAIR				L(1.0)		5,23	D
010105	I/0 HARNESS ASSEMBLY	REPLACE				L(O.5)		5,23	0
	(1090D04418-202) AlA1W3	TEST				L(0.2)		11	D
		REPAIR				L(1.0)		5,23	D
010106	INPUT POWER CABLE ASSENBLY	REPLACE				L(0.5)		5,23	D
	(A3028360) A1A1W4	TEST				L(O.2)		11	D
		REPAIR				L(1.0)		5,23	D
010107	UNIBUS HARNESS ASSEMBLY	REPLACE				L(0.5)		5,23	D
	(109D04434-202) A1A1W5	TEST				L(0.2)		11	D
		REPAIR				L(1.0)		5,23	D
010108	HARNESS ASSEMBLY	REPLACE				L(0.5)		5,23	D
	(A3028363) AlAI16	TEST				L(0.2)		11	D
		REPAIR				L(1.0)		5,23	D
0101A*	HOUSING ASSEMBLY	TEST					2.0	9,10,11,22	G,H
	(A3028370) A1A1	REPAIR					1.0	5,14,23	G,H
010101A*	GRANDMOTHER CIRCUIT CARD	REPLACE					1.0	5,23	G,H
	ASSEMBLY (A3028354) A1AlAl	TEST					1.0	9-11,22	B,G,H
		REPAIR					1.5	14,23	G,H

NV-15-102-101
110686

• Alternate Configuration

SECTION II MAINTENANCE ALLOCATION CHART
FOR
AN/UYK-42(V)4

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL UNIT C	UNIT O	INTERMEDIATE F	INTERMEDIATE H	DEPOT D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
010102A	POWER SUPPLY, MODULE (A3028415) AiA1PS1	SAME AS 010102							
01010201A	INPUT BASIC MO)ULE (A3028417) AIA1PS1A2	SAME AS 01010201							
01010202A	MASTER BASIC MODULE (A3028416) AlA1PS1A3	SAME AS 01010202							
01010203A*	BACKPLANE ASSEMBLY (A3028418) A1AlPSlA4	REPLACE TEST					1.0 1.0	5,23 9,10,22	F,G,H B
010103A	SYSTEM CONSOLE HARNESS ASSEMBLY (A3028396) AIAI1W1	SAME AS 010103							
010104A	I/O-A HARNESS ASSEMBLY (A3028422) AlAlW2	SAME AS 010104							
010105A	1/O0 HARNESS ASSEMBLY (109D004418-202) AIA1W3	SAME AS 010105							
010106A	INPUT POWER CABLE ASSEMBLY (A3028360) A1AiW4	SAME AS 010106							
010107A	UNIBUS HARNESS ASSEMBLY (109004434-202) A1AlW5	SAME AS 010107							
010108A	HARNESS ASSEMBLY (A3028363) AlA1W6	SAME AS 010108							
0102	MOS MEMORY CIRCUIT CARD ASSEMBLY (109004878-201) AIA2, A1A3	REPLACE TEST 24-26,28 REPAIR				L(O.2)	 2.0 2.0	2,4,5,23 1,12,15, 5,14,23	D,H H,J H
010201	MOS MEMORY CIRCUIT CARD ASSEMBLY (109004592-102) A1AZA1, AlA3A1	REPLACE TEST REPAIR					1.0 X x	5,14,23	H B B
010202	MOS MEMORY CIRCUIT CARD ASSEMBLY (109D004593-305) A1A2A2, A1ASA2	REPLACE TEST REPAIR					1.0 X X	5,14,23	H B B
010202A*	NOS MEMORY CIRCUIT CARD ASSEMBLY (109D04593-404) A1AZA2, A1ASA2	REPLACE TEST REPAIR					1.0 X X	5,14,23	G,H B B
0103	MEMORY I/F CIRCUIT CARD ASSEMBLY (109004460-103) A1A4	REPLACE TEST REPAIR				L(0.2)	 2.0 2.0	2,4,5,23 1,12,17,21, 27-32 5,14,23	D,H E,H,J E,H
0103A*	MEMORY I/F CIRCUIT CARD ASSEMBLY (109D04460-302) A1A4	REPLACE TEST REPAIR				L(O.2)	 2.0 2.0	2,4,5,23 1,12,17,21, 27-32 5,14,23	D,G,H E,G,H,J E,G,H
0104	UNIBUS IF MODULE (A3028411) A1A8	REPLACE TEST REPAIR				L(0.2)	 2.0 2.0	2,4,5,23 1,12,16-21, 27,28 5,14,23	D,H H,J H

NV-15-102-101
110686

• Alternate Configuration

SECTION II MAINTENANCE ALLOCATION CHART
FOR
AN/IYK-42(V)4

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL UNIT C	UNIT O	INTERMEDIATE F	INTERMEDIATE H	DEPOT D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
010401	UIBSUS A CIRCUIT CARD ASSEMBLY (109004370-103) A1ASA1	REPLACE REPAIR TEST					1.0 X X	5,14,23	H B B
010401A*	UNIBUS A CIRCUIT CARD ASSEMBLY (109004370-302) A1AIA1	REPLACE REPAIR TEST					1.0 X X	5,14,23	G,H B B
010401B*	UWIBUS A CIRCUIT CARD ASSEMBLY (109004370-401) A1A8A1	REPLACE REPAIR TEST					1.0 X x	5,14,23	G,H B B
010402	UNIBUS B CIRCUIT CARD ASSEMBLY (109004368-102) A1A8A2	REPLACE REPAIR TEST					1.0 X X	5,14,23	N B B
0105	CACHE CIRCUIT CARD ASSEMBLY (109004520-201) A1A9 27,28,33-36	REPLACE TEST REPAIR				LCO.2)	 2.0 2.0	2,4,5,23 1,12,17,21, 5,14,23	D,H E,H,J E,H
010501	CACHE CIRCUIT CARD ASSEMBLY A (109D04522-102) A1A9A1	REPLACE TEST REPAIR					1.0 X X	5,14,23	H B B
010502	CACHE CIRCUIT CARD ASSEMBLY B (109D004523-103) AIA9A2	REPLACE TEST REPAIR					1.0 X X	5,14,23	N B B
010502A*	CACHE CIRCUIT CARD ASSEMBLY B (109004523-202) AIA9A2	REPLACE TEST REPAIR					1.0 X X	5,14,23	G,H B B
0106	DATA PATH CIRCUIT CARD ASSEMBLY (109D04480-401) AIAO1 27,28,37-40	REPLACE TEST REPAIR				L(O.2)	 2.0 2.0	2,4,5,23 1,12,17,21, 5,14,23	D,H E,H,J E,H
010601	DATA PATH A CIRCUIT CARD ASSEMBLY (109004482-301) A1lOA1	REPLACE TEST REPAIR					1.0 x X	5,14,23	H B B
010602	DATA PATH B CIRCUIT CARD ASSEMBLY (109004483-102) AIA1OA2	REPLACE TEST REPAIR					1.0 x X	5,14,23	N B B
0106A*	DATA PATH CIRCUIT CARD ASSEMBLY (109D04480-301) A1A10 27,28,37-40	REPLACE TEST REPAIR				L(O.2)	 2.0 2.0	2,4,5,23 1,12,17,21, 5,14,23	D,G,H E,G,H,J E,G,H
010601A*	DATA PATH A CIRCUIT CARD ASSEMBLY (109004482-301) A1AIOA1	REPLACE TEST REPAIR					1.0 X	5,14,23 X	G,H B B
010602A*	DATA PATH B CIRCUIT CARD ASSEMBLY (109004483-201) AlAIOA2	REPLACE TEST REPAIR					1.0	5,14,23 X X	G,H B B
0107	CONTROL MODULE ASSEMBLY (109004304-202) A1All	REPLACE TEST REPAIR					L(0.2) 2.0 2.0	2,4,5,23 1,12,17,21, 28,41-44 5,14,23	D,H E,Y E,H

• Alternate Configuration

NV-15-102-101
110686

SECTION II MAINTENANCE ALLOCATION CHART
FOR
AN/UYK-42(V)4

(1) GROUP NUMBER	(2) COMPONENT ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE LEVEL UNIT C	UNIT O	INTERMEDIATE F	INTERMEDIATE H	DEPOT D	(5) TOOLS AND EQUIPMENT	(6) REMARKS
010701	CONTROL A CIRCUIT CARD ASSEMBLY (109DO4366-203) A1A11A1	REPLACE					1.0	5,14,23	H
		TEST					X		B
		REPAIR					X		B
010702	CONTROL B CIRCUIT CARD ASSEMBLY (109D04492-105) AlA11A2	REPLACE					1.0	5,14,23	N
		TEST					X		B
		REPAIR					X		B
0107A*	CONTROL MODULE ASSEMBLY (109D04304-102) A1A11	REPLACE				L(0.2)		2,4,5,23	D,G,H
		TEST					2.0	1,12,17,21, 28,41-44	E,G,H,J
		REPAIR					2.0	5,14,23	E,G,H
010701A*	CONTROL A CIRCUIT CARD ASSEMBLY (109D04366-103) A1A11Al	REPLACE					1.0	5,14,23	G,H
		TEST					X		B
		REPAIR					X		B
010701B*	CONTROL A CIRCUIT CARD ASSEMBLY (109D04366-202) AA11A11	REPLACE					1.0	5,14,23	G,H
		TEST					X		B
		REPAIR					X		B
010701C*	CONTROL A CIRCUIT CARD ASSEMBLY (109004366-102) A1AI1A1	REPLACE					1.0	5,14,23	G,H
		TEST					X		B
		REPAIR					X		B
010702A*	CONTROL B CIRCUIT CARD ASSEMBLY (109D4492-204) AlAIlA2	REPLACE					1.0	5,14,23	G,H
		TEST					X		B
		REPAIR					X		B
010702B*	CONTROL B CIRCUIT CARD ASSEMBLY (109D04492-105) AlA11A2	REPLACE					1.0	5,14,23	G,H
		TEST					X		B
		REPAIR					x		B
0108	MODULE ASSEMBLY I/F (109004670-201) AIA12	REPLACE				L(0.2)		2,4,5,23	D,H
		TEST					2.0	1,12,17,21, 27,28,45-48	E,H,J
	REPAIR						2.0	5,14,23	E,H
010801	MULTIFUNCTION A CIRCUIT CARD ASSEMBLY (109004512-103) A1A12Al	REPLACE					1.0	5,14,23	H
		TEST					x		B
		REPAIR					X		B
010801A*	HULTIFUNCTION A CIRCUIT CARD ASSEMBLY (109D04512-102) AlA12A	REPLACE					1.0	5,14,23	G,H
		TEST					X		B
		REPAIR					X		B
010802	MULTIFUNCTION B CIRCUIT CARD ASSEMBLY (109D04513-102) A1A12A2	REPLACE					1.0	5,14,23	H
		TEST					X		B
		REPAIR					X		B
0109	CONSOLE I/F MODULE CIRCUIT CARD ASSEMBLY (109D04302-202) AlA13	REPLACE				L(O.2)		2,4,5,23	D,H
		TEST					2.0	1,12,17,21, 28,49-52	E,H,J
		REPAIR					2.0	5,14,23	E,H
0109A*	CONSOLE I/F MODULE CIRCUIT CARD ASSEMBLY (109004302-201) A1A13	REPLACE					L(O.2)	2,4,5,23	D,G,H
		TEST					2.0	1,12,17,21, 28,49-52	E,G,H,J
		REPAIR					2.0	5,14,23	E,H
0110	SMS CIRCUIT CARD ASSEMBLY (A3028352) AlA5	REPLACE					L(O.2)	2,4,5,23	D,H
		TEST					2.0	1,6,8,11, 12,15,28	H,J
		REPAIR					2.0	5,14,23	H

• Alternate Configuration

NV-15-102-101
110686

SECTION II MAINTENANCE ALLOCATION CHART
FOR
AN/UYK-42 (V)4

(1)	(2)	(3)	(4) MAINTENANCE LEVEL					(5)	(6)
			UNIT		INTERMEDIATE		DEPOT		
GROUP NUMBER	COMPONENT ASSEMBLY	MAINTENANCE FUNCTION	C	O	F	H	D	TOOLS AND EQUIPMENT	REMARKS
0111	SMA CIRCUIT CARD ASSEMBLY (A3028351) A1A6	REPLACE				L(0.2)		2,4,5,23	D,H
		TEST					2.0	1,6,7,11, 12,15,28	H,J
		REPAIR					2.0	5,14,23	H
0112	SMI CIRCUIT CARD ASSEMBLY (A3028350) A1A7	REPLACE				L(O.2)		2,4,5,23	D,H
		TEST					2.0	1,6,11,12, 13,15,28	H,J
		REPAIR					2.0	5,14,23	H
02	UNIBUS TERMINATOR A2 (109000320'203)	REPLACE				L(0.05)			D,H
		TEST					1.5	11,54;56	H
		REPAIR					2.0	5,11,14,23	H

• Alternate Configuration

NV-15-102-101
110686

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR
AN/UYK-42(V)4

(1) TOOL OR TEST EQUIPMENT REF CODE	(2) MAINTENANCE LEVEL	(3) NOMENCLATURE	(4) NATIONAL/NATO STOCK NUMBER	(5) TOOL NUMBER
1	L, D	TEST SET, COMPUTER TS-4293/UYK-42(V)4	6625-01-238-7972	NORDEN P/N
		CONSISTING OF:		109D006300-101
		SMI TEST CARD		109006320-101
		8-INCH DISK DRIVE (WU/CONTROLLER CCA)		DEC RXZ11-BA
		MEMORY POWER LOOP		109D06316-101
		BACKPLANE		DEC DD11-DK
		EXPANDER CHASSIS		DEC BA11-KU
		UNIBUS ADAPTER		
		UNIBUS CABLE (VS)		109DO0209-000A
		CONSOLE CABLE (W1)		109006312-101
		POVER CABLE, AC (W4)		109D06315-101
		CABLE, I/O TEST (UW2)		109D06313-101
		CABLE, I/O TEST (W3)		109006314-101
		CABLE, RS232		BC2D-25
		DIAGNOSTIC CHAIN SOFTWARE		1090-C600-4.1
		ZEROIZE SOFTWARE		109D-C600-5.0
		Fan Assembly W/Adapter Plate And Power Cable		109006307-101
		POWER CABLE, AC TEST SET		109D006317-101
2	L, D	TORQUE SCREWDRIVER W/CASE & BITS (2-36 IN.-LB.)		CAL 36/4K
3	L, D	BIT, TORQUE SCREWDRIVER (9/64 IN. HEX.)		P/O #2
4	L, D	BIT, TOROUE SCREWDRIVER (3/32 IN. HEX.)		P/O #2
5	L, D	TOOL KIT, ELECT. TK-17 (INCL. METRIC)	5180-01-195-0855	JENSEN JTK-17RN
6	D	COMPUTER MODULE TEST ADAPTER		NORDEN T04400-525
7	D	COMPUTER SMA MODULE TEST PROGRAM		WORDEN A3028351
8	D	COMPUTER SMS MODULE TEST PROGRAM		NORDEN A3028352
9	D	COMPUTER HOUSING ASSY. TEST CABLE SET		NORDEN TOO510-010
10	D	COMPUTER HOUSING ASSY. TEST PROGRAM		NORDEN REGNET 2
11	L, D	MULTIMETER, DIGITAL AN/USN-486	6625-01-145-2430	FLUKE 8050A-01
12	L, D	CONSOLE, PRINTER		DEC LA120-DA
13	D	COMPUTER SMI MODULE TEST PROGRAM		NORDEN A3028350
14	D	MAINTENANCE KIT, PCB NX-10879/G	5895-01-267-9473	PACE MODEL RNR 8007-0117
15	D	IN-CIRCUIT TESTER		GENRAD GR 2272
16	D	COMPUTER UNIBUS INT. MKD. TEST PROGRAM	NORDEN D8005	
17	D	UNIVERSAL ADAPTER	6625-01-164-0542	NORDEN T00500-155
18	D	EXTENDER CARD ASSEMBLY		NORDEN T00500-474
19	D	CERTIFICATION TOOL		NORDEN T00500-745
20	D	CERTIFICATION TEST PROGRAM		NORDEN T5474
21	D	STATIC FUNCTIONAL TESTER		GENRAD GR 1795

NV-15-102-102
110686

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR
AN/UYK-42 (V)4

(1) TOOL OR TEST EQUIPMENT REF CODE	(2) MAINTENANCE LEVEL	(3) NOMENCLATURE	(4) NATIONAL/NATO STOCK NUMBER	(5) TOOL NUMBER
22	D	CONTINUITY TESTER		DIT-MCO 9100
23	L, D	WORKSTATION, STATIC	4910-01-087-3458	3H 8021
24	D	TEST PROGRAM (512K WORD HME)		NORDEN 109D04592
25	D	TEST FIXTURE PROGRAM		NORDEN 109D004593
26	D	TEST FIXTURE (512K WORD MEN)		UCRD T0"L00-555-101
27	D	OSCILLOSCOPE AN/USM-488	6625-01-187-7847	TEK 2235L
28	D	CONPUTER, DIGITAL AN/UYK-42(V)4	5895-01-205-6149	A3023763
29	D	TEST PROGRAM (MEN I/F)		NORDEN D4460
30	D	TEST FIXTURE (MEN I/F)		NORDEN T00500-450
31	D	CERTIFICATION TOOL		NORDEN T00500-725
32	D	CERTIFICATION TEST PROGRAM		NORDEN T5450
33	D	TEST PROGRAM (CACHE ASSEMBLY)		NORDEN D4520
34	D	TEST FIXTURE (CACHE ASSEMBLY)		NORDEN T00500-486
35	D	CERTIFICATION TOOL		NORDEN 500500-755
36	D	CERTIFICATION TEST PROGRAM		NORDEN T5486
37	D	TEST PROGRAM (DATA PATH)		NORDEN D4480
38	0	TEST FIXTURE (DATA PATH ASSEMBLY)		NORDEN T00500-462
39	D	CERTIFICATION TOOL		NORDEN T00500-735
40	D	CERTIFICATION TEST PROGRAM		NORDEN T5462
41	D	TEST PROGRAM (CONTROL ASSEMBLY)		NORDEN D4304
42	D	TEST FIXTURE (CONTROL ASSEMBLY)		NORDEN T00500-468
43	D	CERTIFICATION TOOL		NORDEU 500500-740
44	D	CERTIFICATION TEST PROGRAM		NORDEN T5468
45	D	TEST PROGRAM (RULTIFUNCTION ASSEMBLY)		NORDEN D4670
46	0	TEST FIXTURE (MULTIFUNCTION)		NORDEN T00500-480
47	D	CERTIFICATION TOOL		UORDEN T00500-750
48	D	CERTIFICATION TEST PROGRAM		NORDEN T5480
49	D	TEST PROGRAM (CONSOLE I/F)		NORDEN D4302
50	D	TEST FIXTURE (CONSOLE I/F)		NORDEN T00500-456
51	D	CERTIFICATION TOOL		NORDEN f00500-730
52	D	CERTIFICATION TEST PROGRAM		NORDEN T5456
53	0	TEST SET, POWER SUPPLY		NRO 00510-005-101
54	D	TEST FIXTURE (UNIBUS TERMINATOR)		1DE 5-060- 101

NV-15-102-102
110686

SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR
AN/UYK-42 (V)4

(1) TOOL OR TEST EQUIPMENT REF CODE	(2) MAINTENANCE LEVEL	(3) NOMENCLATURE	(4) NATIONAL/NATO STOCK NUMBER	(5) TOOL NUMBER
55	D	POWER SUPPLY PP-8202/G	6130-00-160-0827	HP 627B8
56	D	POWER SUPPLY		HP-6255A
57	D	TEST CABLE, POWIER SUPPLY		NORDEN TOO510-004
58	D	OSCILLOSCOPE, STORAGE		HP-1741A
59	D	POWER DECADE RESISTOR		CLAROSTAT 240-C
60	D	COOLING FAN		
61	D	HEAT SINK PLATES		
62	D	POWER SUPPLY MODULE ALA1PS1		A3028415

NV-15-102-102
110686

SECTION IV
REMARKS
AN/UYK-42 (V)4

REFERENCE CODE	REMARKS
A	System/Terminal on-line BIT provides indication of faulty unit.
B	Test/repair as part of next higher assembly
C	Consists of fault isolation/replacement of defective module/subassembly including Unibus Terminator.
D	Special Repair Activity (SRA).
E	Refer to DMWR 11-5895-1207 for test/repair procedures.
F	Non-repairable item.
G	Alternate configuration.
H	Electro-static sensitive item.
I	Consists of fault isolation to, and replacement of, Basic and Master Basic Module
J	Also requires module be dynamically exercised in CPU Test Setup using TS-4293/UYK-42(V)4 in known good processor.

APPENDIX C
EXPENDABLE/DURABLE SUPPLIES AND MATERIALS LIST

Section I. INTRODUCTION

C-1. SCOPE

This appendix lists expendable/durable supplies and materials you will need to operate and maintain the CPU. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

C-2. EXPLANATION OF COLUMNS

a. Column(1). Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e. ., "Use cleaning compound, item 5, App. E").

b. Column(2), Level. This column identifies the lowest level of maintenance that requires the listed item.

C - Operator/Crew
0 - Organizational Maintenance
F - Direct Support Maintenance
H - General Support Maintenance

c. Column(3). National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column(4), Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parentheses followed by the part number.

e. Column(5), Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

(1) ITEM NUMBER	(2) LEVEL	(3) NATIONAL STOCK NUMBER	(4) DESCRIPTION	(5) UNIT OF MEAS.
1	H		3/8 inch Polyester Film Tape, two-roll package, PN 853 (20318)	ea.

APPENDIX D
AN/UYK-42(V)4 DIAGNOSTIC CHAIN PRINTOUT
(SAMPLE PRINTOUT OF DIAGNOSTICS)

```
;    THIS DIAGNOSTIC CHAIN IS USED TO TEST THE  AN/UYK-42(V)4 PROCESSOR UNIT.
;
;    DUE TO THE HIGH DEGREE OF INTERCONNECTION BETWEEN THE CPU MODULES IT MAY BE NECESSARY ;
     TO REPLACE AN ANCILLARY MODULE INSTEAD OF THE SPECIFIC MODULE UNDER TEST.   A
;    RECOMMENDED ORDER OF REPLACEMENT IS INCLUDED WITH EACH TEST.
;
;    A FAILURE IS INDICATED IF THE SPECIFIED TEST TIME IS EXCEEDED, OR A PRINTOUT OTHER THAN
;    SPECIFIED IS OUTPUT.   REFER TO THE AN/UYK-42(V)4 MAINTENANCE  MANUAL FOR AN EXAMPLE OF ;A
COMPLETED CHAIN PRINTOUT AND TROUBLESHOOTING PROCEDURES.
;
;    IF A FAILURE OCCURS, REMOVE AND REPLACE MODULES IN THE ORDER GIVEN IN THE INTRODUCTION
;    TO THE FAILING TEST.
;
;    THE TOTAL TEST TIME IS APPROXIMATELY 18 MINUTES.
;
;    11/44 CPU/EIS TEST
;    TIS PROGRAM TESTS THE CPU MODULES
;    (All,A10,A12,A10O,A9,A8).  IT WILL PRINT 'END OF
;    CKKAAAO 11/44 CPU/EIS' WHEN SUCCESSFULLY COMPLETED.
;    TEST TIME IS APPROX.  10 SEC.
R KKAAAO/2

END OF CKKAAAO 11/44 CPU/EIS
END OF CKKAAAO 11/44 CPU/EIS
```

```
;    11/44 TRAPS TEST
;    THIS PROGRAM TESTS THE CPU MODULES
;    (All,A10O,A9,A8,A12,A13).  IT WILL PRINT 'END OF
;    CKKABAO 11/44 TRAPS' WHEN SUCCESSFULLY COMPLETED.
;    TEST TIME IS APPROX.  10 SEC.
R KKABAN/2
CKKABAO 11/44 TRAPS
NO FLOATING POINT OPTION PRESENT
NO CIS OPTION PRESENT
END OF CKKABAO 11/44 TRAPS
END OF CKKABAO 11/44 TRAPS
;    11/44 MEMORY MANAGEMENT PART 1 THIS PROGRAM TESTS
;    THE CPU DATA PATH MODULE (A10,All,A8,A9,A12,A4).   IT
;    WILL PRINT 'END PASS' WHEN SUCCESSFULLY COMPLETED.
;    TEST TIME IS APPROX.  15 SEC.
R KKTAB1/2
CKKTAB 11/44 MEM MGMT PRT A
END PASS #1TOTAL ERRORS SINCE LAST REPORT0
END PASS #2TOTAL ERRORS SINCE LAST REPORT0
;    11/44 MEMORY MANAGEMENT PART 2
;    THIS PROGRAM TESTS THE CPU DATA PATH MODULE
;    (A10,All,A8,A9,A12,A4).   IT WILL PRINT 'END PASS'
;    WHEN SUCCESSFULLY COMPLETED.
;    TEST TIME IS APPROX.  10 SEC.
R KKTBCO/2
CKKTBCO 11/44 MEM MGMT PRT B
END PASS #1TOTAL ERRORS SINCE LAST REPORTO
END PASS #2TOTAL ERRORS SINCE LAST REPORTO
```

```
;     11/44 UBI BOOT DIAGNOSTIC
;     THIS PROGRAM TESTS THE CPU UNIBUS INTERFACE MODULE
;     (A8,A10,All,A12,A9,A4,A2,A3).   IT WILL PRINT 'END
;     PASS' WHEN SUCCESSFULLY COMPLETED.
;     TEST TIME IS APPROX.  15 SEC.
R ZM9BDM/2

CZM9BDO M9312/1144 UBI BOOT

DIAG.  ROM (E20) (FOR 11-44 UBI: E58)CO

BOOTSTRAP ROM ENTRY POINTS AND DEVICE CODES

     LOC.                NO DIAG.            RUN DIAG.           DEVICE CODE

ROM 1(E48)               173004              173006                CT

ROM 2(E49)               173204              173206                DY

ROM 3(E50)               173404              173406                DM

ROM 4(E59)               173604              173606                DX

PSEUDO POWER-FAIL VECTOR ADR./NEW PC   173024 165024

END PASS
END PASS

;
;     11/44UBI MAP DIAGNOSTIC
;     THIS PROGRAM TESTS THE CPU UNIBUS INTERFACE MODULE
;     (A8,All,A10,A12,A9,A4,A2,A3).   IT WILL PRINT 'END
;     PASS' WHEN SUCCESSFULLY COMPLETED.
;     TEST TIME IS APPROX.  30 SEC.
R KKUAAO/2
CKKUAAO 11/44 UBI MAP
END PASS #          1        TOTAL ERRORS SINCE LAST REPORT          0
END PASS #          2        TOTAL ERRORS SINCE LAST REPORT          0
.5K RESTORED
```

```
;     11/44 MULTIFUNCTION DIAGNOSTIC
;     THIS PROGRAM TESTS THE CPU MULTIFUNCTION AND CONSOLE
;     INTERFACE MODULES (A12,All,A.10,A13,A8,A9).  IT WILL
;     PRINT 'END PASS' WHEN SUCCESSFULLY COMPLETED.
;     TEST TIME IS APPROX.  25 SEC.
;
R ZDLD01/2
CZDLDEO DL11-W,1144 MFM SLU
02 DEVICES UNDER TEST
END PASS
END PASS
;
;
;
;     11/44 KK1llB CACHE DIAGNOSTIC
;     THIS PROGRAM TESTS THE CPU CACHE MODULE
;     (A9,A2,A3,A4,All,A10).   IT WILL PRINT 'END PASS'
;     WHEN SUCCESSFULLY COMPLETED.
;     TEST TIME IS APPROX.  1:15 MIN.

R KKKAAN/2

CKKKAAO 11-44 KK1B CACHE
RMI REGISTER (G5179) NOT USED-SKIP HI ORDER BIT ADDRESS TEST

UNIBUS EXERCISER NOT USED- DMA TESTS NOT PERFORMED

END OF PASS E1
END OF PASS #2
```

```
;
;
;  ----------------------------------------------------------------------------------------------------
;
;    MS11 L/M MEMORY DIAGNOSTIC
;    THIS PROGRAM TESTS THE 11/44 MEMORY AND MEMORY
;    INTERFACE MODULES (A2,A3,A4,A9,A10,All,A12).  IT WILL
;    PRINT 'END PASS' WHEN SUCCESSFULLY COMPLETED.
;    TEST TIME IS APPROX.  11 MIN.
R ZMSD01/2

    CZMSDA
        11/44 CACHE AVAILABLE
CSR NUMBER 0 CONTROLS TOO MANY BANKS
CSR NUMBER 1 CONTROLS TOO MANY BANKS
        512K OF MS11-M
        512K WORDS OF MEMORY TOTAL
        MEMORY CONFIGURATION MAP

           1          2          3                4          5                6          7
             0 1 2 3 4 5 6 7 0 1 2 3 4 5 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 01 2 3 4 567 0 1 2 3 45 67 01 2 3
ERRORS
CPU MAP    1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
INTRLV      ------------------------------------------------
MEMTYPE    MMMMMMMMMMMMMMMMMMMMMMMMMMMMMMMM
CSR        0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
PROTECT PP
           0          1          2                3          4                5          6
             4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 23 4 56 7 0 12 3 4 5 6 7 0 1 2 3 4 5 67
ERRORS
CPU MAP
INTRLV
MEMTYPE
CSR
PROTECT
PROGRAM RELOCATED - ECC TESTS INHIBITED
END PASS #QV    1
PROGRAM RELOCATED - ECC TESTS INHIBITED
END PASS #    2.5K RESTORED
```

```
; ------------------------------------------------------------------------------------------------------
;    SERIAL MULTIPLEXED INTERFACE(SMI) TESTS
;    THESE PROGRAMS TEST THE SMI MODULES (A7,A6,A5).
;    EACH WILL PRINT 'END PASS' WHEN SUCCESSFULLY
;    COMPLETED.
;    TEST TIME FOR SUPRV1 IS APPROX.  40 SEC.
;    TEST TIME FOR XRSIZ2 IS APPROX.  50 SEC.
;
R SUPRV1/2

REGENCY NET SMI DIAGNOSTIC SUPERVISOR

I-O CARD 0 IS PRESENT AND ACTIVE

I-O CARD 1 IS PRESENT AND ACTIVE

I-O CARD 2 IS NOT PRESENT

I-O CARD 3 IS NOT PRESENT

END PASS #1

END PASS #2
;
R XRSIZ2/2

REGENCY NET SMI IO DATA BLOCK TRANSFER

STATUS AFTER 'DRIVER ALIVE'
CNSTATIOSTAT   IO   ID    REG15
000000  000000   042041   000000

END PASS #1
END PASS #2

;
;    ---------------------------------------------------------------------------
;    END OF AN/UYK-42(V)4 DIAGNOSTIC CHAIN
;    ---------------------------------------------------------------------------
;
```

APPENDIX E
MODULE INTERCHANGEABILITY

E-1. SCOPE

This appendix lists the module interchangeability of Computer, Digital, AN/UYK-42 (V) 4.

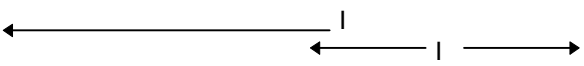
E-2. MODULE INTERCHANGEABILITY

The three digit suffix at the end of each NORDEN P/N was established as a means of denoting revision levels. The first digit change was used to denote product improvements and to aid the manufacturer in identifying rework and create an assembly number that could be used to track the costs of and ECN incorporation. When the criteria of interchangeability could not be met, then a new family number was created. The third digit was to basically denote a cleanup of PCB boards to eliminate jumpers.

The following charts provide the change history of each Regency Net module/CCA that is also in the AN/UYK-42(V) computer family. Included is the three digit suffix when it was created and the interchangeability with other versions of the module. For example 109D04480-301 can be replaced with a -401, however the -401 should not be replaced by a -301.

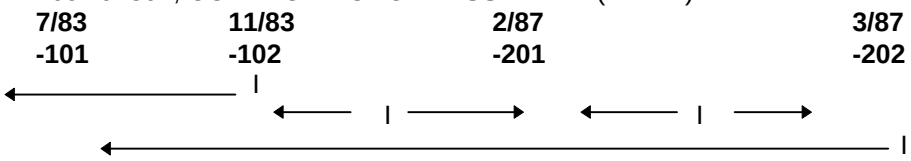
E-2 MODULE INTERCHANGEABILITY (Cont.)

109D04302, CONSOLE I/F MODULE CCA (A1A13)

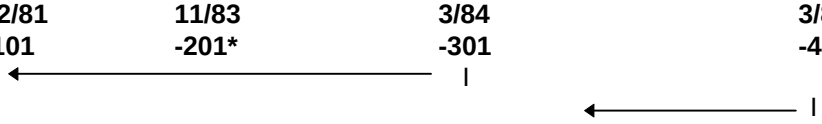


109D04670, MODULE ASSEMBLY I/F (MULTIFUNCTION) (A1A12)

109D04304, CONTROL MODULE ASSEMBLY (A1A11)



109D04480, DATA PATH CCA (AlA10)

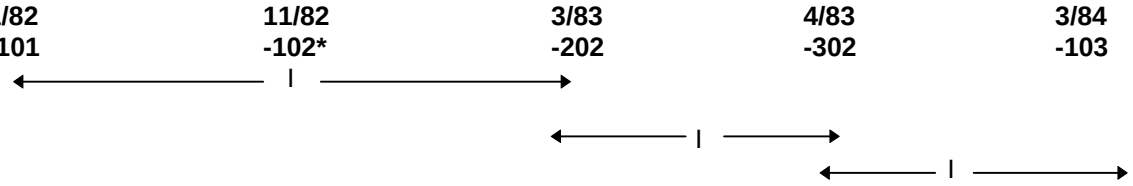


I= Interchangeability
*= Never Shipped

E-2 MODULE INTERCHANGEABILITY (Cont.)

109D04520, CACHE CCA (A1A9)

109D04460, MEMORY I/F CCA (A1A4)



109D04878, MOS (256K Word) MEMORY CCA (A1A2, A1A3)

I= Interchangeability
*= Never Shipped

APPENDIX F
AN/UYK-42(V)4 DECLASSIFICATION (ZEROIZING) SOFTWARE PRINTOUT

NOTE

When the prompt NEW = is given, the Computer will stop the zeroizing process. The operator must then manually enter a carriage return <CR> to resume the zeroizing of the Computer.

```
* * * PDP-11/44 DECLASSIFICATION UTILITY   * *
ASSUMED MEMORY SIZE: 512K WORD (1 MEGABYTE)
DECLASS PRAMETER                                        CONDITION
  ------------------------------------------------------
CONTINUE AFTER ERROR ..... DISABLE
ERROR HANDLING ..... REPORT
DETAILED ERROR REPORTING  ..... DISABLED
RING BELL ON ERROR  ..... DISABLED
DECLASS SMI  ..... ENABLED
DECLASS MAIN MEMORY ..... ENABLED
DECLASS CACHE MEMORY ..... ENABLED
PROGRAM RELOCATION  ..... ENABLED
RUNTIME ERROR COUNT LIMIT ..... NONE
SWR = 000000
NEW =
STARTING CACHE MEMORY DECLASSIFICATION...
**
CACHE MEMORY DECLASSIFICATION COMPLETED

MEMORY BANKS TO BE DECLASSIFIED (DECIMAL): 0 TO 31

STARTING MAIN MEMORY DECLASSIFICATION
**
**
**
**
        5 BANKS COMPLETED
**
**
**
**
**
```

```
            10 BANKS COMPLETED
      **
      **
      **
      **
      **
            15 BANKS COMPLETED
      **
      **
      **
      **
            20 BANKS COMPLETED
      **
      **
      **
      **
      **
            25 BANKS COMPLETED
      **
      **
      **
      **
      **
            30 BANKS COMPLETED

      ATTEMPTING PROGRAM RELOCATION TO MEMORY BANK 1
      ***PNO ERROGRAM AREA RELOCATED***
      **
            ALL BANKS COMPLETED

      STARTING SMI DECLASSIFICATION

      SMI DECLASSIFICATION COMPLETED
      ******************************************************
      ***  DECLASSIFICATION COMPLETED    ***
      *** NO ERRORS DETECTED              ***
      ***                  (NOT RESTARTABLE)   ***
      ******************************************************
      NOTE: TEST TIME IS APPROX.  2HRS.

      CONSOLE
      17777707 005134
>>>
```

APPENDIX G
AN/UYK-42(V)4 ADDRESSES FOR VERIFICATION OF DFCI ASSIFICATION (7FRO171NG)

To verify that the memory circuits of the computer have been zeroized (declassified) type the following addresses (commands) on the console. The response (printout) to each address is to be 177777, indicating that the address is all one's (zeroed).

COMMANDCOMMAND

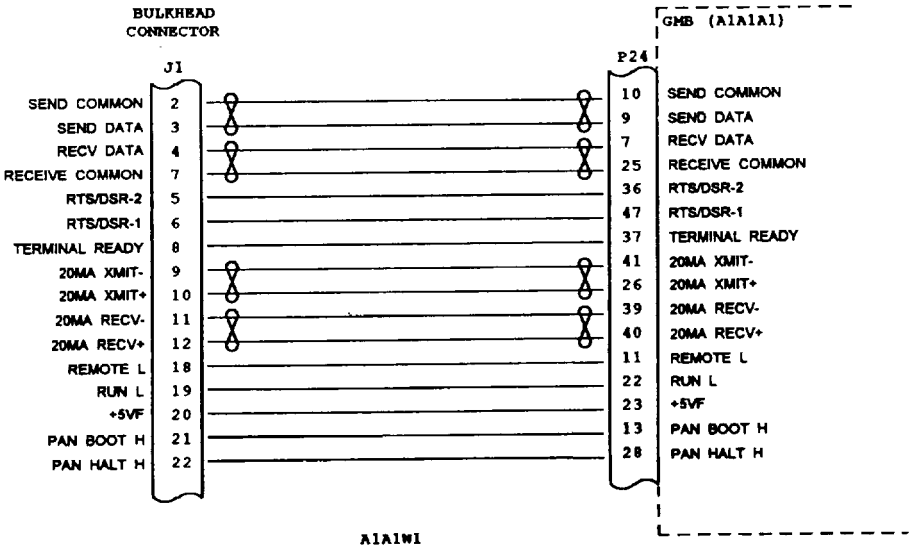
E 105020<CR>
E 206444<CR>
E 306512<CR>
E 407032<CR>
E 510100<CR>
E 611660<CR>
E 711722<CR>
E 1012630<CR>
E 1114672<CR>
E 1214746<CR>
E 1316304<CR>
E 1421536<CR>
E 1522354<CR>
E 1627436<CR>
E 1731062<CR>
E 2000000<CR>
E 2031400<CR>
E 2131760<CR>
E 2233236<CR>
E 2333530<CR>
E 2440252<CR>
E 2540602<CR>
E 2641116<CR>
E 2752370<CR>
E 3062126<CR>
E 3163250<CR>
E 3263546<CR>
E 3364106<CR>
E 3467164<CR>
E 3570102<CR>
E 3671340<CR>
E 3777776<CR>

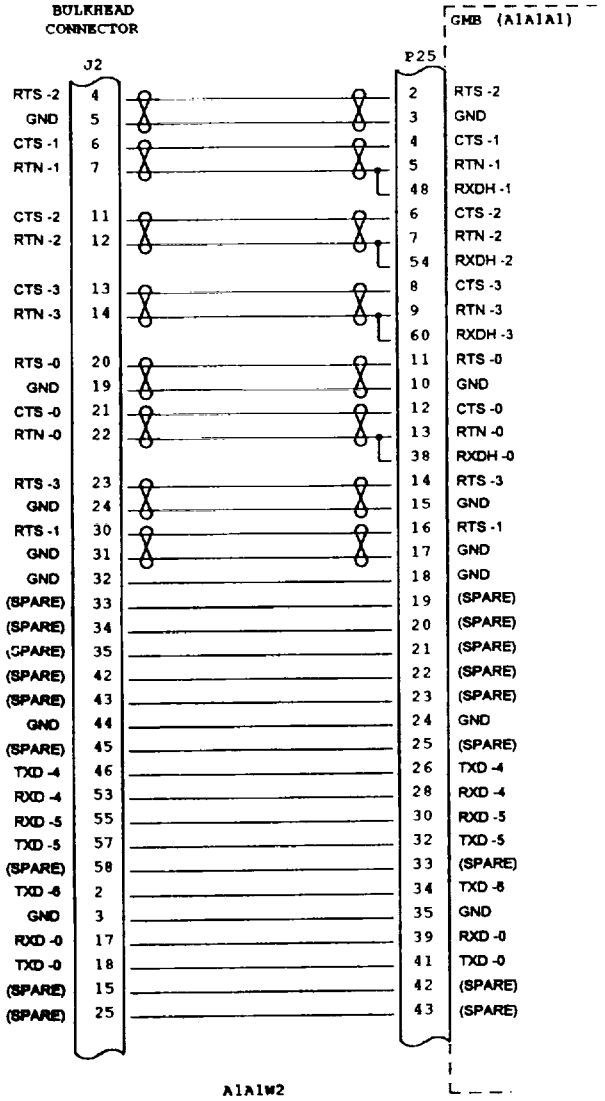
APPENDIX H
COMPUTER, DIGITAL INTERCONNECTING DIAGRAM

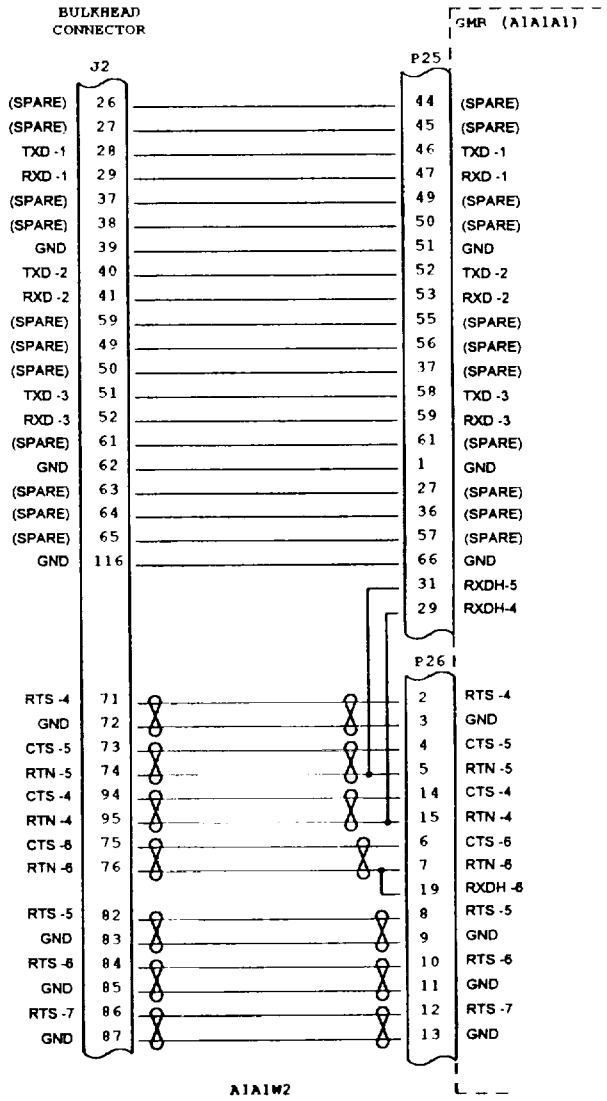
TABLE I

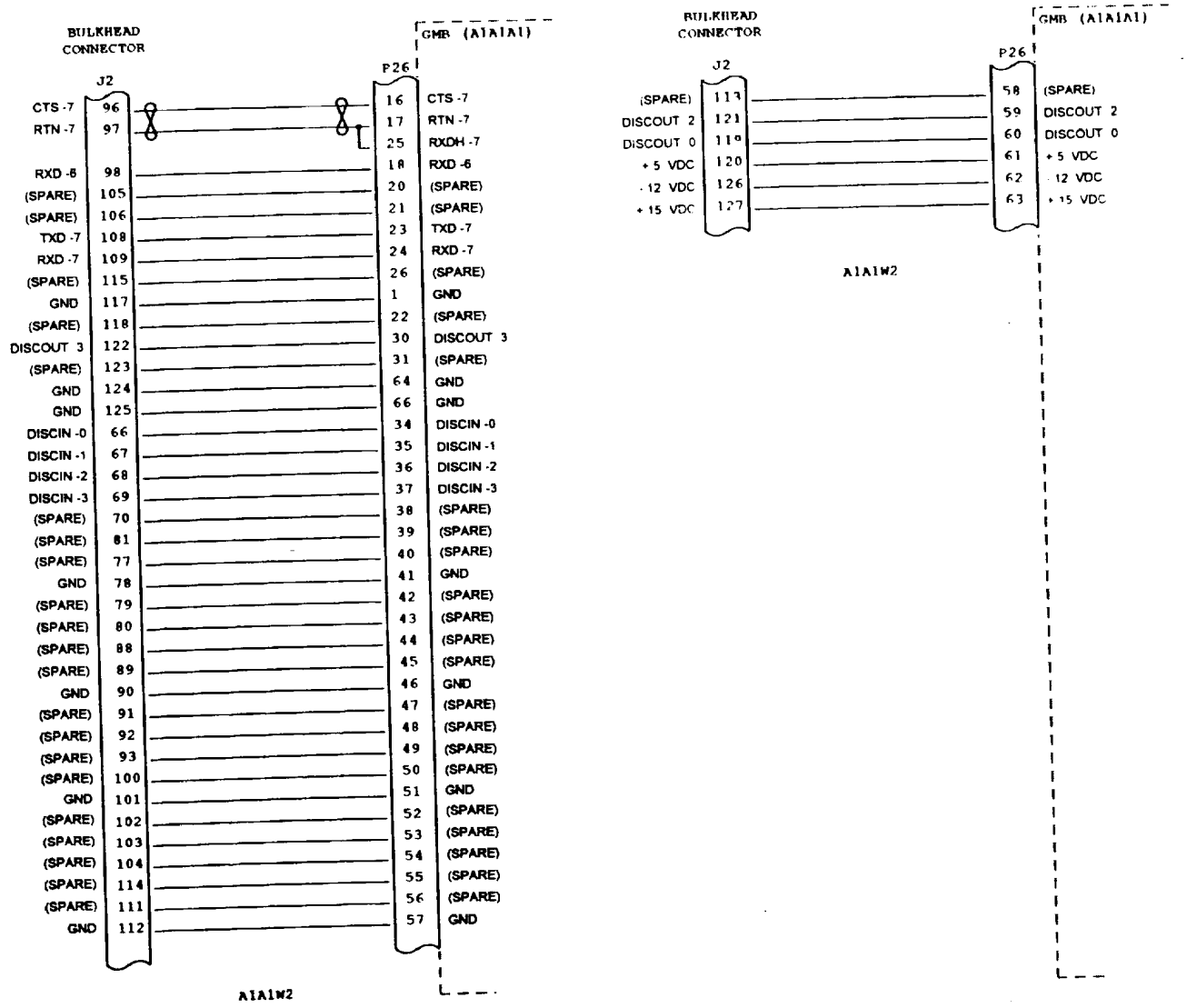
ASSEMBLY CROSS REFERENCE TABLE		
REFERENCE DESIGNATION	ASSEMBLY NUMBER	WIRE LIST
A1A1W1	A3028396	A3028397
A1A1W2	A3028422	A3028421
A1A1W3	109D04418-202	109D04419
A1A1W4	A3028360	A3028362
A1A1W5	109D04434-202	109D04435
A1A1W6	A3028363	A3028361 A3028399
A1A1A1	A3086887 ALT A3028354	A3086896
A1A1PS1A3	A3086890 ALT A3028418	A3025783

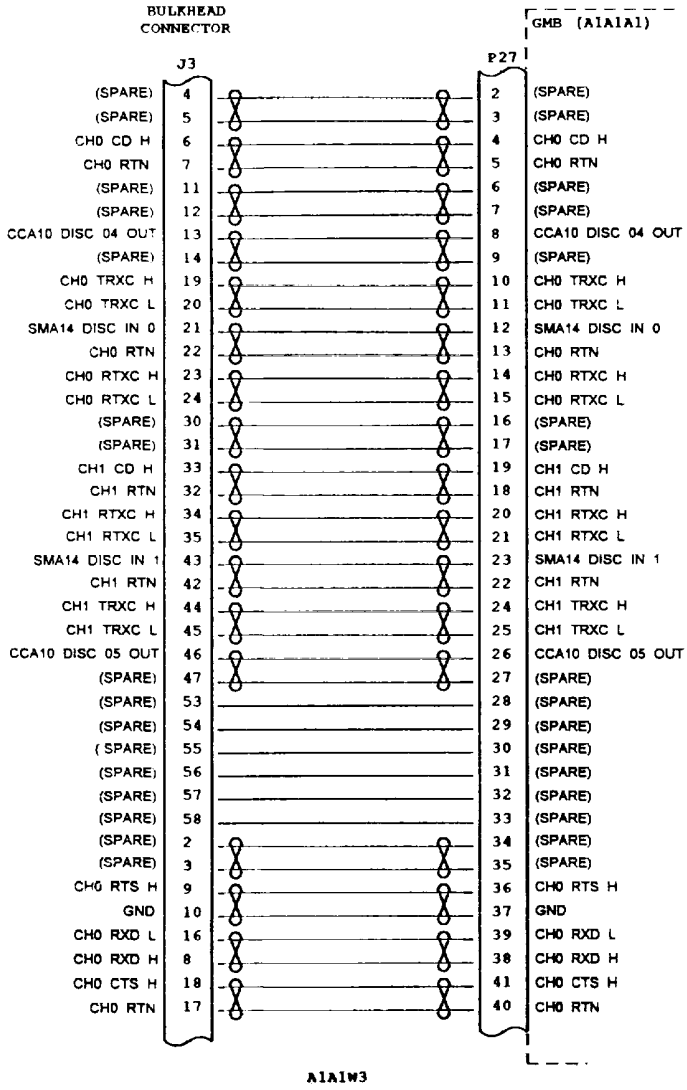
NOTES:
1. REFERENCE DESIGNATIONS ARE SHOWN FOR INFORMATION ONLY .
2. THIS ITEM REQUIRES SPECIAL HANDLING AND PROCESING IAW DOD-STD-1686 AND DOD-RHDB-263 TO PREVENT DAMAGE FROM BLECTROSTATIC DISCHARGE TRANSIENTS.
3. CHARCTERS UNDERLINED DENOTE LOER CASE.
4. FOR RELATED ASSEMBLY AND WIRE LIST DOCUMENTS, REFER TO ASSEMBLY CROSS REFERENCE TABLE {TABLE I).
5. TWISTED PAIR WIRES ARE INDICATED BY THE SYMBOL ↑ OR ↑ TP
6. PINS NOT SHOWN ARE NO CONNECTS (NC)

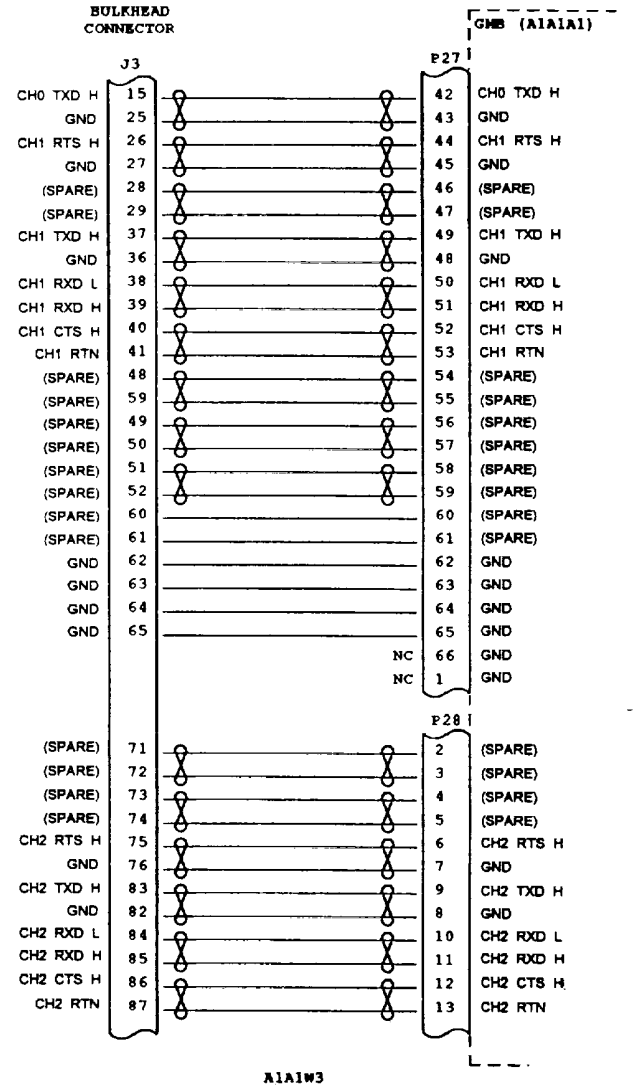


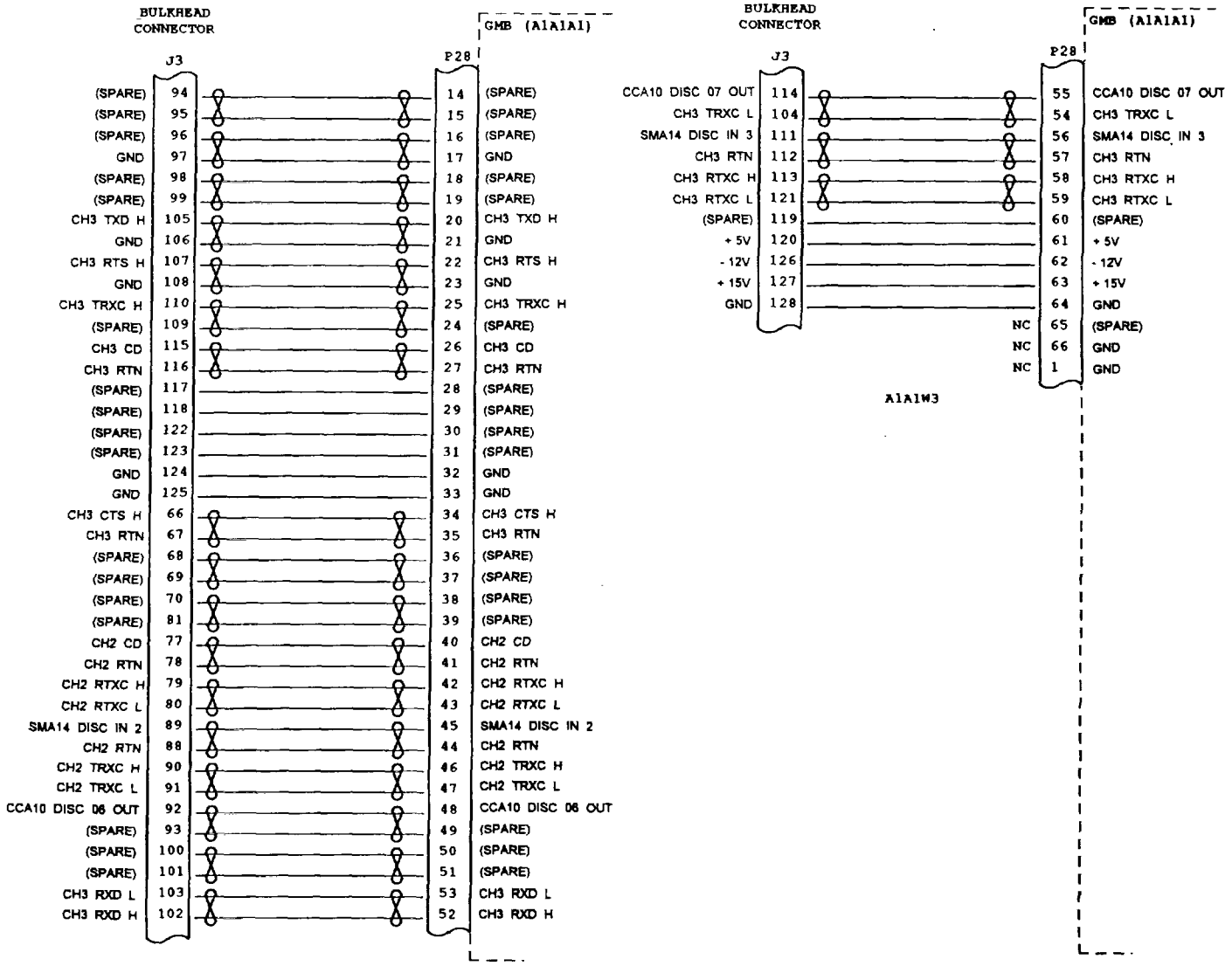

BULKHEAD CONNECTOR
J2
GMB (A1A1A1)
P25
RTS -2 4
GND 5
CTS -1 6
RTN -1 7
CTS -2 11
RTN -2 12
CTS -3 13
RTN -3 14
RTS -0 20
GND 19
CTS -0 21
RTN -0 22
RTS -3 23
GND 24
RTS -1 30
GND 31
GND 32
(SPARE) 33
(SPARE) 34
(SPARE) 35
(SPARE) 42
(SPARE) 43
GND 44
(SPARE) 45
TXD -4 46
RXD -4 53
RXD -5 55
TXD -5 57
(SPARE) 58
TXD -6 2
GND 3
RXD -0 17
TXD -0 18
(SPARE) 15
(SPARE) 25
2 RTS -2
3 GND
4 CTS -1
5 RTN -1
48 RXDH -1
6 CTS -2
7 RTN -2
54 RXDH -2
8 CTS -3
9 RTN -3
60 RXDH -3
11 RTS -0
10 GND
12 CTS -0
13 RTN -0
38 RXDH -0
14 RTS -3
15 GND
16 RTS -1
17 GND
18 GND
19 (SPARE)
20 (SPARE)
21 (SPARE)
22 (SPARE)
23 (SPARE)
24 GND
25 (SPARE)
26 TXD -4
28 RXD -4
30 RXD -5
32 TXD -5
33 (SPARE)
34 TXD -6
35 GND
39 RXD -0
41 TXD -0
42 (SPARE)
43 (SPARE)
A1A1W2


BULKHEAD CONNECTOR
J2
GMR (A1A1A1)
P25
P26
(SPARE) 26
(SPARE) 27
TXD -1 28
RXD -1 29
(SPARE) 37
(SPARE) 38
GND 39
TXD -2 40
RXD -2 41
(SPARE) 59
(SPARE) 49
(SPARE) 50
TXD -3 51
RXD -3 52
(SPARE) 61
GND 62
(SPARE) 63
(SPARE) 64
(SPARE) 65
GND 116
RTS -4 71
GND 72
CTS -5 73
RTN -5 74
CTS -4 94
RTN -4 95
CTS -6 75
RTN -6 76
RTS -5 82
GND 83
RTS -6 84
GND 85
RTS -7 86
GND 87
44 (SPARE)
45 (SPARE)
46 TXD -1
47 RXD -1
49 (SPARE)
50 (SPARE)
51 GND
52 TXD -2
53 RXD -2
55 (SPARE)
56 (SPARE)
37 (SPARE)
58 TXD -3
59 RXD -3
61 (SPARE)
1 GND
27 (SPARE)
36 (SPARE)
57 (SPARE)
66 GND
31 RXDH-5
29 RXDH-4
2 RTS -4
3 GND
4 CTS -5
5 RTN -5
14 CTS -4
15 RTN -4
6 CTS -6
7 RTN -6
19 RXDH -6
8 RTS -5
9 GND
10 RTS -6
11 GND
12 RTS -7
13 GND
A1A1W2

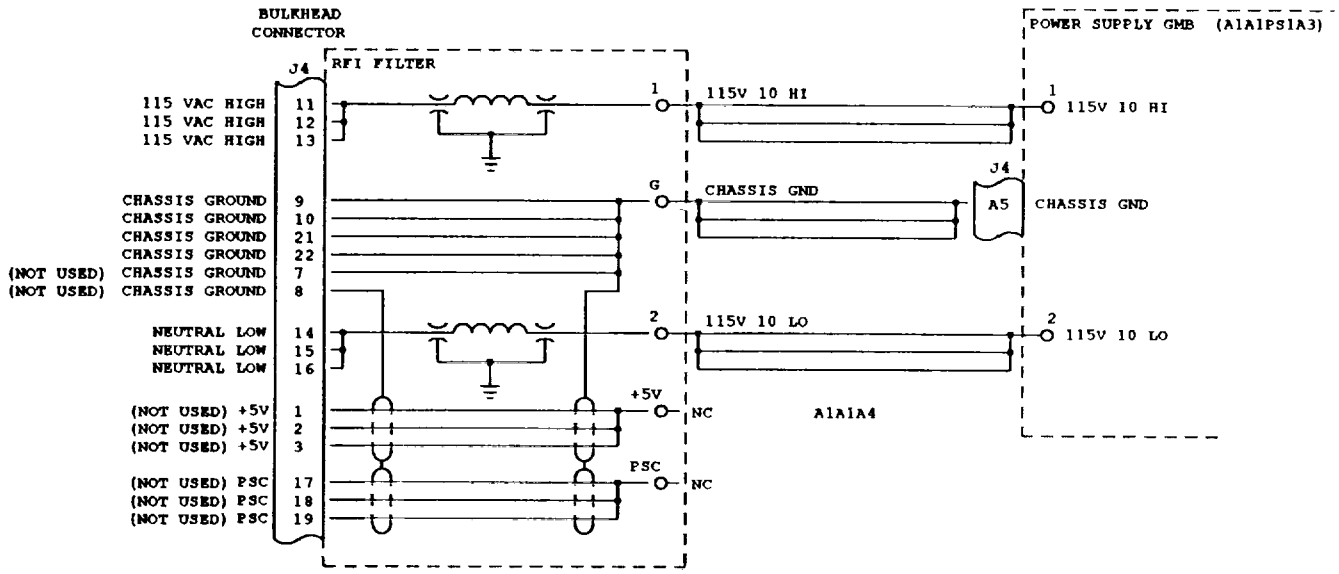

BULKHEAD CONNECTOR
J2
GMB (A1A1A1)
P26
CTS -7 96 — 16 CTS -7
RTN -7 97 — 17 RTN -7
25 RXDH -7
RXD -6 98 — 18 RXD -6
(SPARE) 105 — 20 (SPARE)
(SPARE) 106 — 21 (SPARE)
TXD -7 108 — 23 TXD -7
RXD -7 109 — 24 RXD -7
(SPARE) 115 — 26 (SPARE)
GND 117 — 1 GND
(SPARE) 118 — 22 (SPARE)
DISCOUT 3 122 — 30 DISCOUT 3
(SPARE) 123 — 31 (SPARE)
GND 124 — 64 GND
GND 125 — 66 GND
DISCIN -0 66 — 34 DISCIN -0
DISCIN -1 67 — 35 DISCIN -1
DISCIN -2 68 — 36 DISCIN -2
DISCIN -3 69 — 37 DISCIN -3
(SPARE) 70 — 38 (SPARE)
(SPARE) 81 — 39 (SPARE)
(SPARE) 77 — 40 (SPARE)
GND 78 — 41 GND
(SPARE) 79 — 42 (SPARE)
(SPARE) 80 — 43 (SPARE)
(SPARE) 88 — 44 (SPARE)
(SPARE) 89 — 45 (SPARE)
GND 90 — 46 GND
(SPARE) 91 — 47 (SPARE)
(SPARE) 92 — 48 (SPARE)
(SPARE) 93 — 49 (SPARE)
(SPARE) 100 — 50 (SPARE)
GND 101 — 51 GND
(SPARE) 102 — 52 (SPARE)
(SPARE) 103 — 53 (SPARE)
(SPARE) 104 — 54 (SPARE)
(SPARE) 114 — 55 (SPARE)
(SPARE) 111 — 56 (SPARE)
GND 112 — 57 GND
A1A1W2
BULKHEAD CONNECTOR
J2
GMB (A1A1A1)
P26
(SPARE) 113 — 58 (SPARE)
DISCOUT 2 121 — 59 DISCOUT 2
DISCOUT 0 119 — 60 DISCOUT 0
+5 VDC 120 — 61 +5 VDC
-12 VDC 126 — 62 -12 VDC
+15 VDC 127 — 63 +15 VDC
A1A1W2

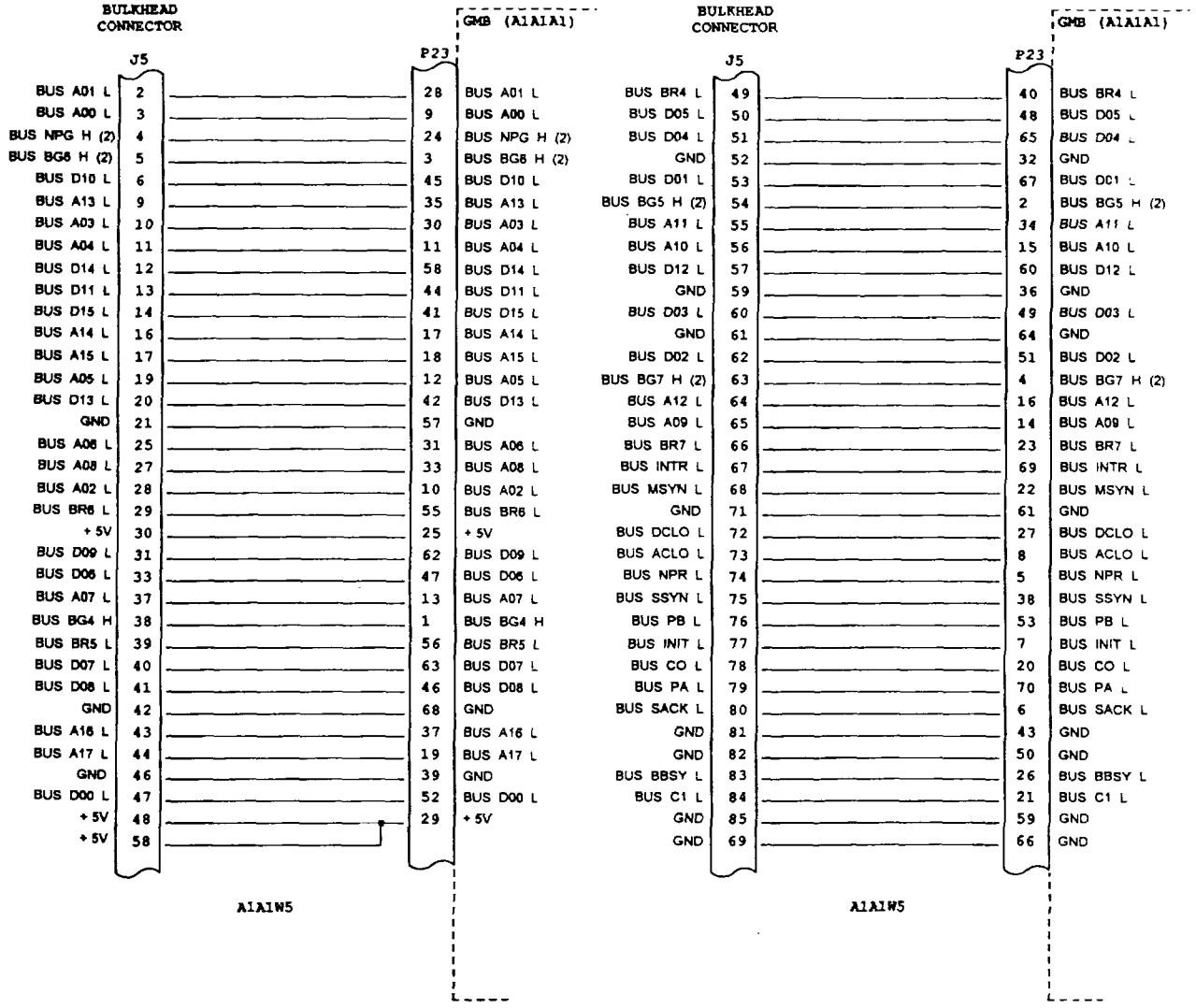

BULKHEAD CONNECTOR
J3
GMB (A1A1A1)
P27
(SPARE) 4 — 2 (SPARE)
(SPARE) 5 — 3 (SPARE)
CH0 CD H 6 — 4 CH0 CD H
CH0 RTN 7 — 5 CH0 RTN
(SPARE) 11 — 6 (SPARE)
(SPARE) 12 — 7 (SPARE)
CCA10 DISC 04 OUT 13 — 8 CCA10 DISC 04 OUT
(SPARE) 14 — 9 (SPARE)
CH0 TRXC H 19 — 10 CH0 TRXC H
CH0 TRXC L 20 — 11 CH0 TRXC L
SMA14 DISC IN 0 21 — 12 SMA14 DISC IN 0
CH0 RTN 22 — 13 CH0 RTN
CH0 RTXC H 23 — 14 CH0 RTXC H
CH0 RTXC L 24 — 15 CH0 RTXC L
(SPARE) 30 — 16 (SPARE)
(SPARE) 31 — 17 (SPARE)
CH1 CD H 33 — 19 CH1 CD H
CH1 RTN 32 — 18 CH1 RTN
CH1 RTXC H 34 — 20 CH1 RTXC H
CH1 RTXC L 35 — 21 CH1 RTXC L
SMA14 DISC IN 1 43 — 23 SMA14 DISC IN 1
CH1 RTN 42 — 22 CH1 RTN
CH1 TRXC H 44 — 24 CH1 TRXC H
CH1 TRXC L 45 — 25 CH1 TRXC L
CCA10 DISC 05 OUT 46 — 26 CCA10 DISC 05 OUT
(SPARE) 47 — 27 (SPARE)
(SPARE) 53 — 28 (SPARE)
(SPARE) 54 — 29 (SPARE)
(SPARE) 55 — 30 (SPARE)
(SPARE) 56 — 31 (SPARE)
(SPARE) 57 — 32 (SPARE)
(SPARE) 58 — 33 (SPARE)
(SPARE) 2 — 34 (SPARE)
(SPARE) 3 — 35 (SPARE)
CH0 RTS H 9 — 36 CH0 RTS H
GND 10 — 37 GND
CH0 RXD L 16 — 39 CH0 RXD L
CH0 RXD H 8 — 38 CH0 RXD H
CH0 CTS H 18 — 41 CH0 CTS H
CH0 RTN 17 — 40 CH0 RTN
A1A1W3

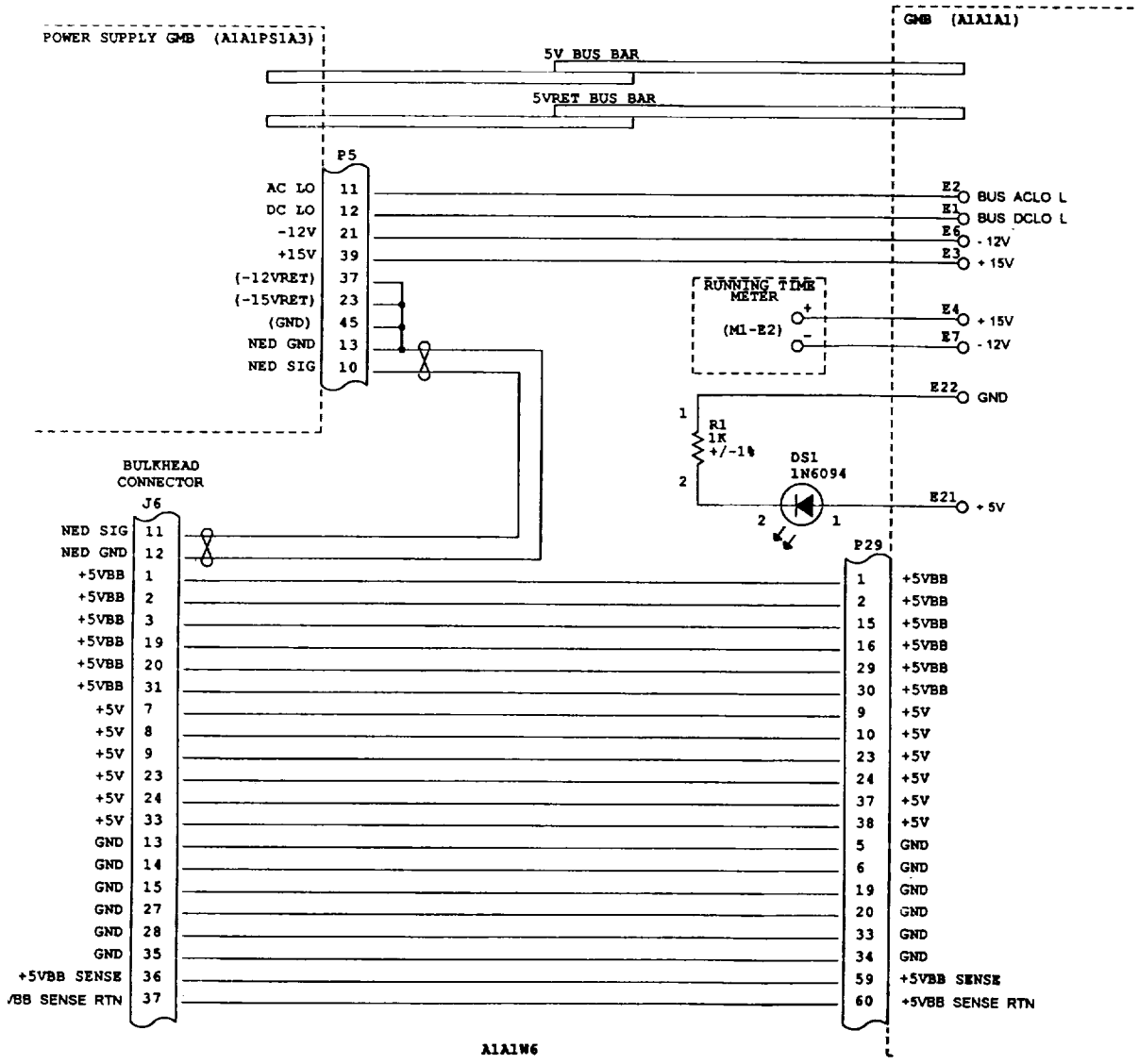

BULKHEAD CONNECTOR
J3
GMB (A1A1A1)
P27
CH0 TXD H 15 — 42 CH0 TXD H
GND 25 — 43 GND
CH1 RTS H 26 — 44 CH1 RTS H
GND 27 — 45 GND
(SPARE) 28 — 46 (SPARE)
(SPARE) 29 — 47 (SPARE)
CH1 TXD H 37 — 49 CH1 TXD H
GND 36 — 48 GND
CH1 RXD L 38 — 50 CH1 RXD L
CH1 RXD H 39 — 51 CH1 RXD H
CH1 CTS H 40 — 52 CH1 CTS H
CH1 RTN 41 — 53 CH1 RTN
(SPARE) 48 — 54 (SPARE)
(SPARE) 59 — 55 (SPARE)
(SPARE) 49 — 56 (SPARE)
(SPARE) 50 — 57 (SPARE)
(SPARE) 51 — 58 (SPARE)
(SPARE) 52 — 59 (SPARE)
(SPARE) 60 — 60 (SPARE)
(SPARE) 61 — 61 (SPARE)
GND 62 — 62 GND
GND 63 — 63 GND
GND 64 — 64 GND
GND 65 — 65 GND
NC 66 GND
NC 1 GND
P28
(SPARE) 71 — 2 (SPARE)
(SPARE) 72 — 3 (SPARE)
(SPARE) 73 — 4 (SPARE)
(SPARE) 74 — 5 (SPARE)
CH2 RTS H 75 — 6 CH2 RTS H
GND 76 — 7 GND
CH2 TXD H 83 — 9 CH2 TXD H
GND 82 — 8 GND
CH2 RXD L 84 — 10 CH2 RXD L
CH2 RXD H 85 — 11 CH2 RXD H
CH2 CTS H 86 — 12 CH2 CTS H
CH2 RTN 87 — 13 CH2 RTN
A1A1W3


BULKHEAD CONNECTOR
J3
GMB (A1A1A1)
P28
(SPARE) 94 — 14 (SPARE)
(SPARE) 95 — 15 (SPARE)
(SPARE) 96 — 16 (SPARE)
GND 97 — 17 GND
(SPARE) 98 — 18 (SPARE)
(SPARE) 99 — 19 (SPARE)
CH3 TXD H 105 — 20 CH3 TXD H
GND 106 — 21 GND
CH3 RTS H 107 — 22 CH3 RTS H
GND 108 — 23 GND
CH3 TRXC H 110 — 25 CH3 TRXC H
(SPARE) 109 — 24 (SPARE)
CH3 CD 115 — 26 CH3 CD
CH3 RTN 116 — 27 CH3 RTN
(SPARE) 117 — 28 (SPARE)
(SPARE) 118 — 29 (SPARE)
(SPARE) 122 — 30 (SPARE)
(SPARE) 123 — 31 (SPARE)
GND 124 — 32 GND
GND 125 — 33 GND
CH3 CTS H 66 — 34 CH3 CTS H
CH3 RTN 67 — 35 CH3 RTN
(SPARE) 68 — 36 (SPARE)
(SPARE) 69 — 37 (SPARE)
(SPARE) 70 — 38 (SPARE)
(SPARE) 81 — 39 (SPARE)
CH2 CD 77 — 40 CH2 CD
CH2 RTN 78 — 41 CH2 RTN
CH2 RTXC H 79 — 42 CH2 RTXC H
CH2 RTXC L 80 — 43 CH2 RTXC L
SMA14 DISC IN 2 89 — 45 SMA14 DISC IN 2
CH2 RTN 88 — 44 CH2 RTN
CH2 TRXC H 90 — 46 CH2 TRXC H
CH2 TRXC L 91 — 47 CH2 TRXC L
CCA10 DISC 06 OUT 92 — 48 CCA10 DISC 06 OUT
(SPARE) 93 — 49 (SPARE)
(SPARE) 100 — 50 (SPARE)
(SPARE) 101 — 51 (SPARE)
CH3 RXD L 103 — 53 CH3 RXD L
CH3 RXD H 102 — 52 CH3 RXD H
BULKHEAD CONNECTOR
J3
GMB (A1A1A1)
P28
CCA10 DISC 07 OUT 114 — 55 CCA10 DISC 07 OUT
CH3 TRXC L 104 — 54 CH3 TRXC L
SMA14 DISC IN 3 111 — 56 SMA14 DISC IN 3
CH3 RTN 112 — 57 CH3 RTN
CH3 RTXC H 113 — 58 CH3 RTXC H
CH3 RTXC L 121 — 59 CH3 RTXC L
(SPARE) 119 — 60 (SPARE)
+ 5V 120 — 61 + 5V
- 12V 126 — 62 - 12V
+ 15V 127 — 63 + 15V
GND 128 — 64 GND
NC 65 (SPARE)
NC 66 GND
NC 1 GND
A1A1W3

A1A1W3


BULKHEAD CONNECTOR
J4
RFI FILTER
POWER SUPPLY GMB (A1A1PS1A3)
115 VAC HIGH 11
115 VAC HIGH 12
115 VAC HIGH 13
1
115V 10 HI
1
115V 10 HI
CHASSIS GROUND 9
CHASSIS GROUND 10
CHASSIS GROUND 21
CHASSIS GROUND 22
(NOT USED) CHASSIS GROUND 7
(NOT USED) CHASSIS GROUND 8
G
CHASSIS GND
J4
A5
CHASSIS GND
NEUTRAL LOW 14
NEUTRAL LOW 15
NEUTRAL LOW 16
2
115V 10 LO
2
115V 10 LO
(NOT USED) +5V 1
(NOT USED) +5V 2
(NOT USED) +5V 3
+5V
NC
A1A1A4
(NOT USED) PSC 17
(NOT USED) PSC 18
(NOT USED) PSC 19
PSC
NC


BULKHEAD CONNECTOR
J5
P23
GMB (A1A1A1)
BUS A01 L 2 28 BUS A01 L
BUS A00 L 3 9 BUS A00 L
BUS NPG H (2) 4 24 BUS NPG H (2)
BUS BG6 H (2) 5 3 BUS BG6 H (2)
BUS D10 L 6 45 BUS D10 L
BUS A13 L 9 35 BUS A13 L
BUS A03 L 10 30 BUS A03 L
BUS A04 L 11 11 BUS A04 L
BUS D14 L 12 58 BUS D14 L
BUS D11 L 13 44 BUS D11 L
BUS D15 L 14 41 BUS D15 L
BUS A14 L 16 17 BUS A14 L
BUS A15 L 17 18 BUS A15 L
BUS A05 L 19 12 BUS A05 L
BUS D13 L 20 42 BUS D13 L
GND 21 57 GND
BUS A06 L 25 31 BUS A06 L
BUS A08 L 27 33 BUS A08 L
BUS A02 L 28 10 BUS A02 L
BUS BR6 L 29 55 BUS BR6 L
+ 5V 30 25 + 5V
BUS D09 L 31 62 BUS D09 L
BUS D06 L 33 47 BUS D06 L
BUS A07 L 37 13 BUS A07 L
BUS BG4 H 38 1 BUS BG4 H
BUS BR5 L 39 56 BUS BR5 L
BUS D07 L 40 63 BUS D07 L
BUS D08 L 41 46 BUS D08 L
GND 42 68 GND
BUS A16 L 43 37 BUS A16 L
BUS A17 L 44 19 BUS A17 L
GND 46 39 GND
BUS D00 L 47 52 BUS D00 L
+ 5V 48 29 + 5V
+ 5V 58
A1A1W5
BULKHEAD CONNECTOR
J5
P23
GMB (A1A1A1)
BUS BR4 L 49 40 BUS BR4 L
BUS D05 L 50 48 BUS D05 L
BUS D04 L 51 65 BUS D04 L
GND 52 32 GND
BUS D01 L 53 67 BUS D01 L
BUS BG5 H (2) 54 2 BUS BG5 H (2)
BUS A11 L 55 34 BUS A11 L
BUS A10 L 56 15 BUS A10 L
BUS D12 L 57 60 BUS D12 L
GND 59 36 GND
BUS D03 L 60 49 BUS D03 L
GND 61 64 GND
BUS D02 L 62 51 BUS D02 L
BUS BG7 H (2) 63 4 BUS BG7 H (2)
BUS A12 L 64 16 BUS A12 L
BUS A09 L 65 14 BUS A09 L
BUS BR7 L 66 23 BUS BR7 L
BUS INTR L 67 69 BUS INTR L
BUS MSYN L 68 22 BUS MSYN L
GND 71 61 GND
BUS DCLO L 72 27 BUS DCLO L
BUS ACLO L 73 8 BUS ACLO L
BUS NPR L 74 5 BUS NPR L
BUS SSYN L 75 38 BUS SSYN L
BUS PB L 76 53 BUS PB L
BUS INIT L 77 7 BUS INIT L
BUS CO L 78 20 BUS CO L
BUS PA L 79 70 BUS PA L
BUS SACK L 80 6 BUS SACK L
GND 81 43 GND
GND 82 50 GND
BUS BBSY L 83 26 BUS BBSY L
BUS C1 L 84 21 BUS C1 L
GND 85 59 GND
GND 69 66 GND
A1A1W5

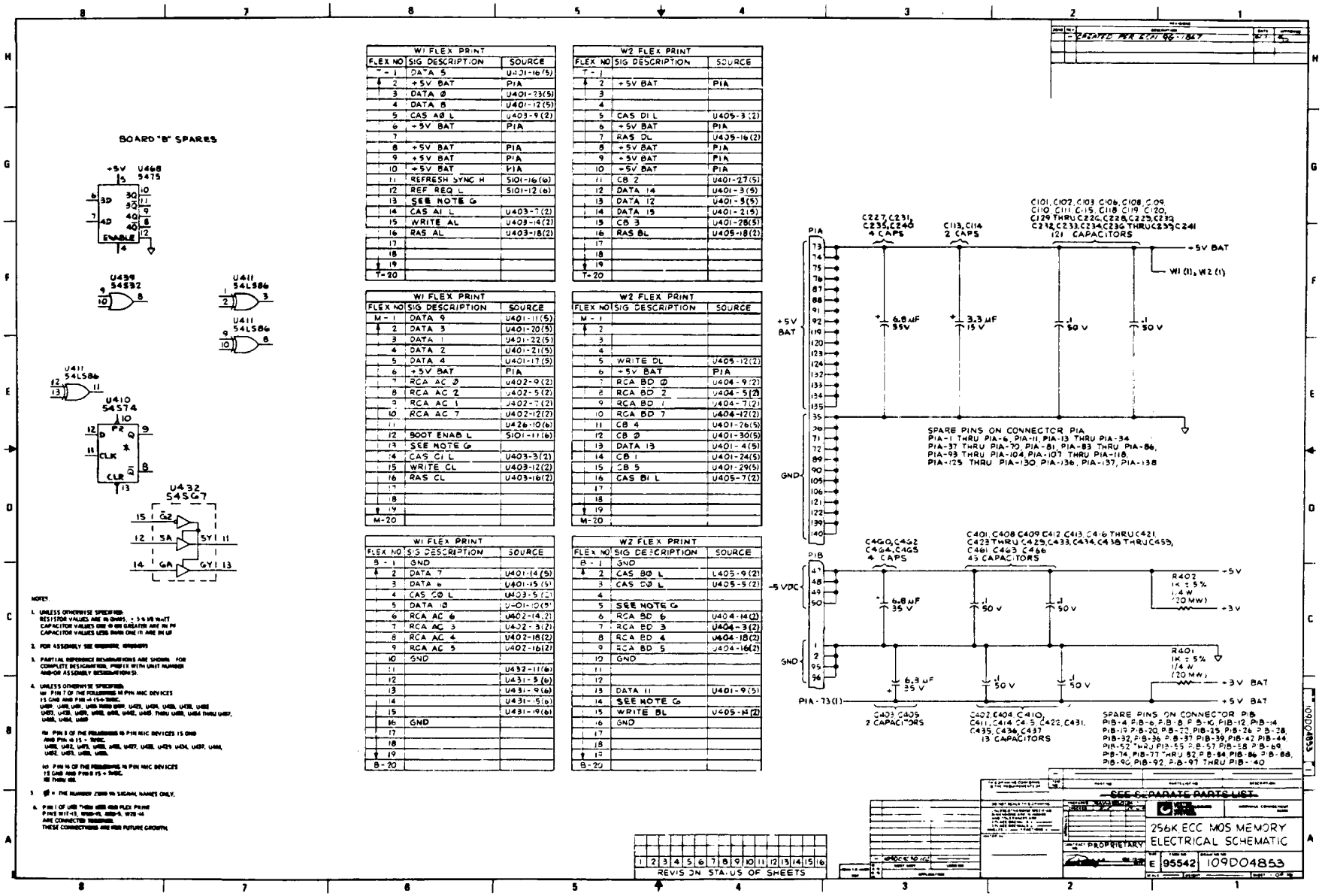

POWER SUPPLY GMB (A1A1PS1A3)
GMB (A1A1A1)
5V BUS BAR
5VRET BUS BAR
P5
AC LO 11
DC LO 12
-12V 21
+15V 39
(-12VRET) 37
(-15VRET) 23
(GND) 45
NED GND 13
NED SIG 10
E2 BUS ACLO L
E1 BUS DCLO L
E6 -12V
E3 +15V
RUNNING TIME METER
(M1-E2)
E4 +15V
E7 -12V
E22 GND
R1 1K +/-1%
DS1 1N6094
E21 +5V
BULKHEAD CONNECTOR
J6
NED SIG 11
NED GND 12
+5VBB 1
+5VBB 2
+5VBB 3
+5VBB 19
+5VBB 20
+5VBB 31
+5V 7
+5V 8
+5V 9
+5V 23
+5V 24
+5V 33
GND 13
GND 14
GND 15
GND 27
GND 28
GND 35
+5VBB SENSE 36
/BB SENSE RTN 37
P29
1 +5VBB
2 +5VBB
15 +5VBB
16 +5VBB
29 +5VBB
30 +5VBB
9 +5V
10 +5V
23 +5V
24 +5V
37 +5V
38 +5V
5 GND
6 GND
19 GND
20 GND
33 GND
34 GND
59 +5VBB SENSE
60 +5VBB SENSE RTN
A1A1W6

APPENDIX I

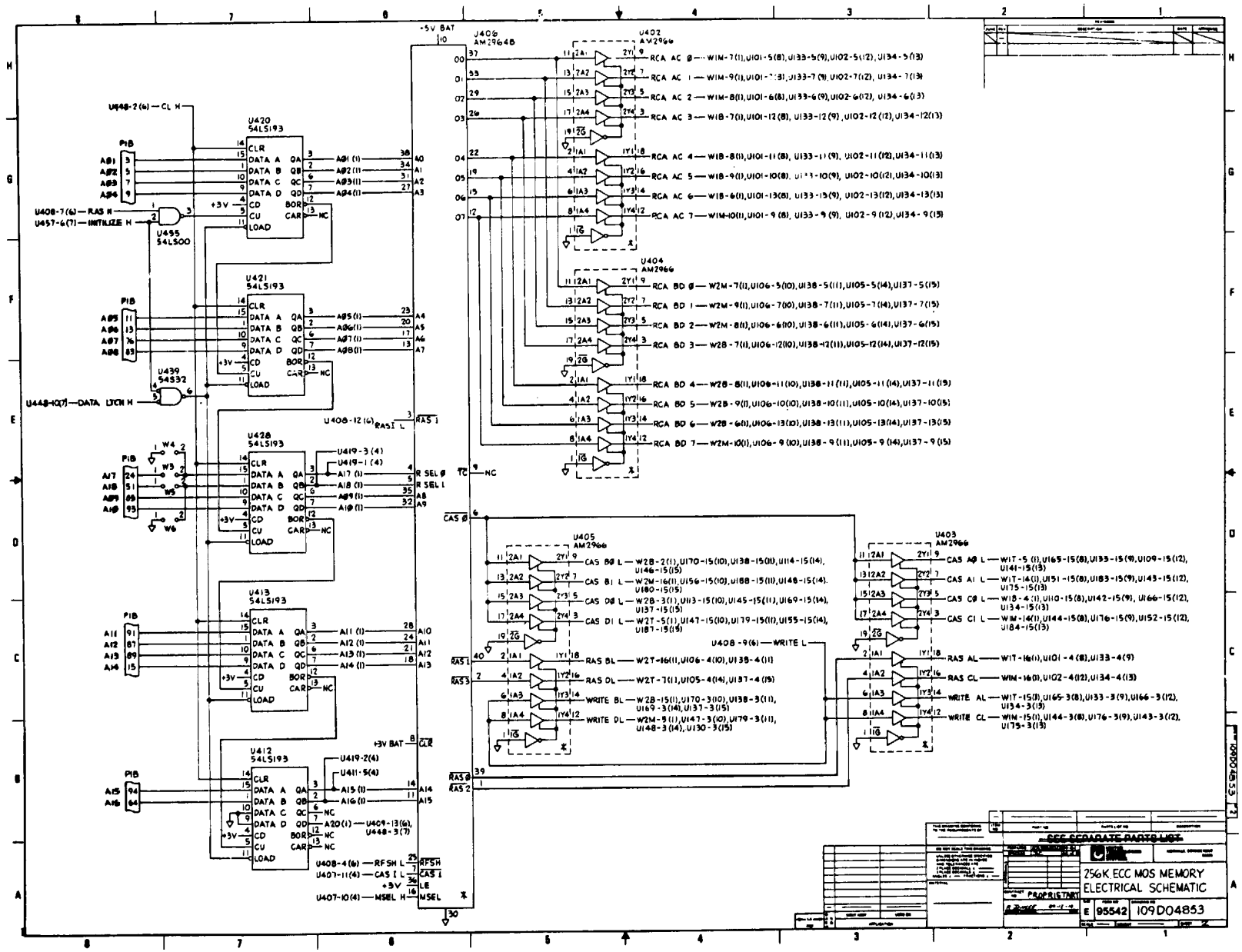
MODULE SCHEMATICS

NOTE

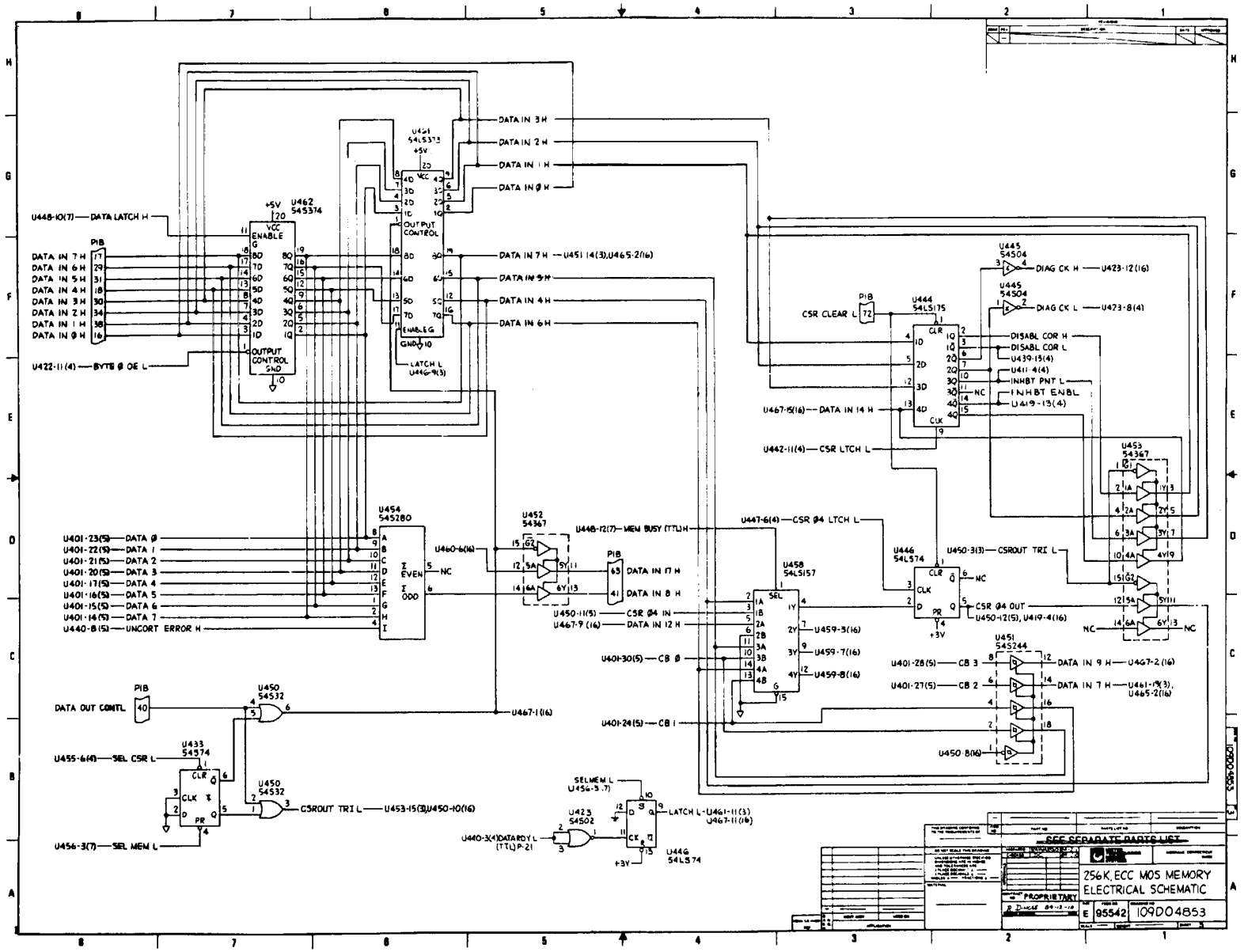
The 109D drawings provided in this Appendix are for repair and maintenance purposes only. The technical information contained in these drawings are proprietary to Norden Systems



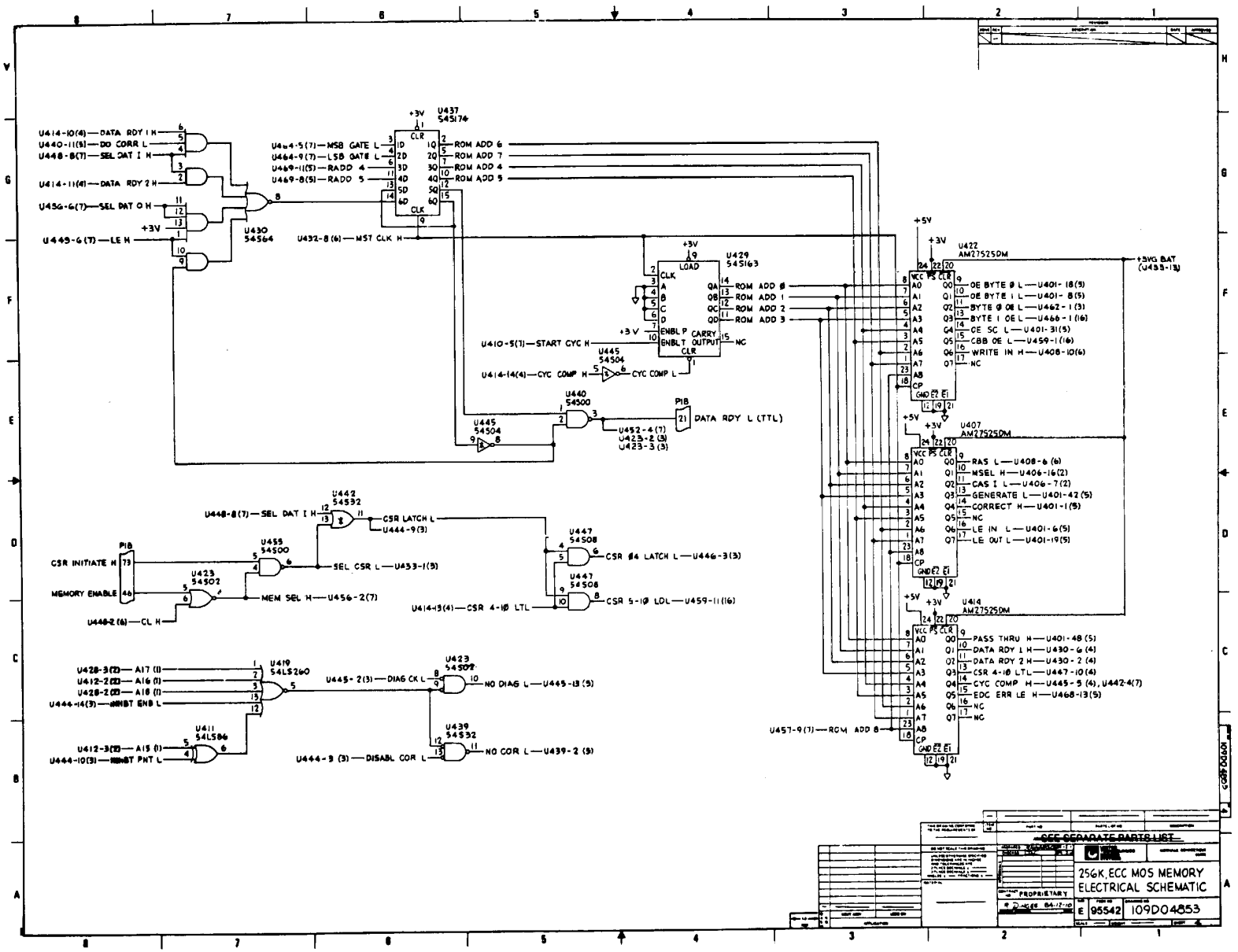
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 1 of 16)



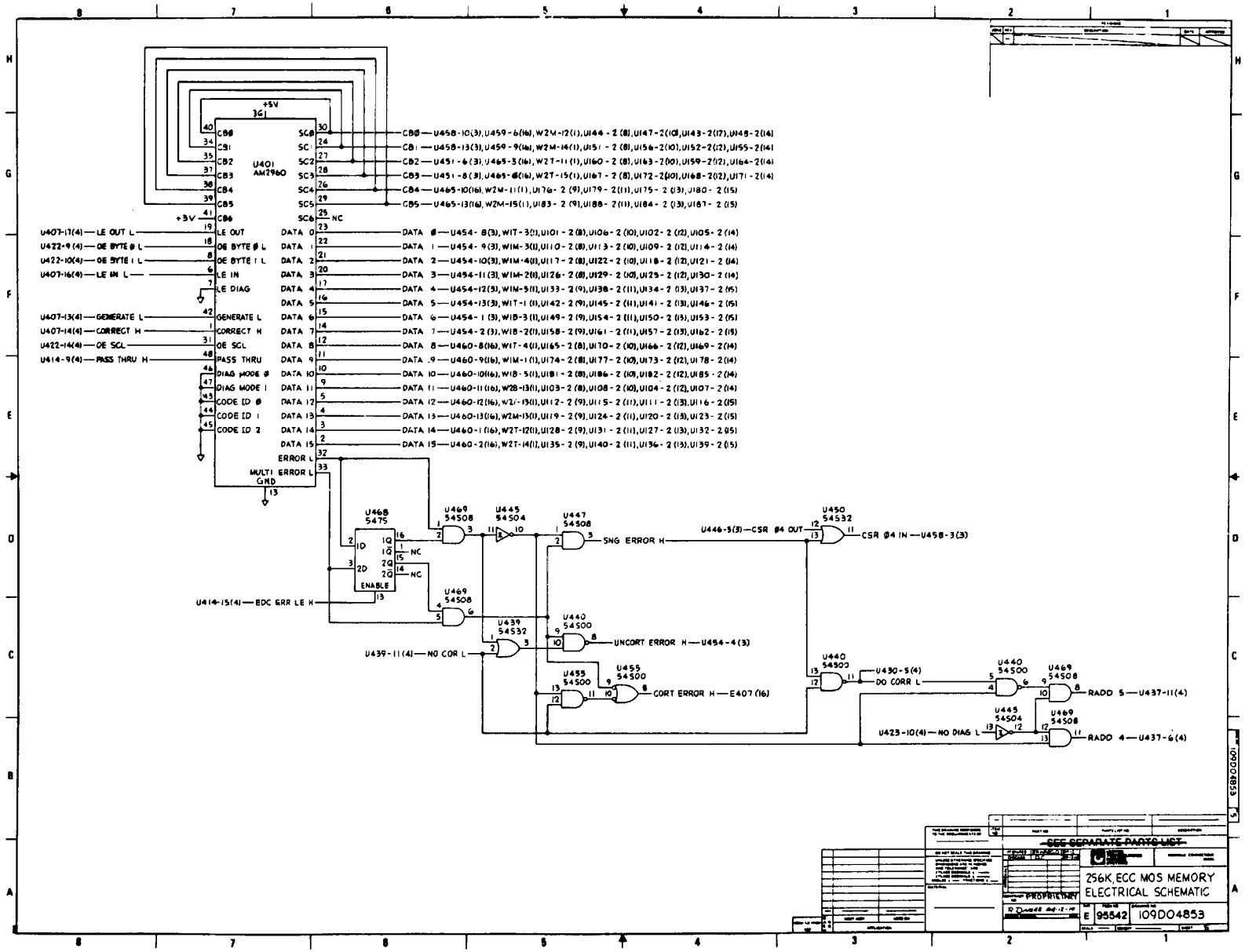
256K (WORD) ECC MS MEMORY
SCHEMATIC (Sheet 2 of 16)



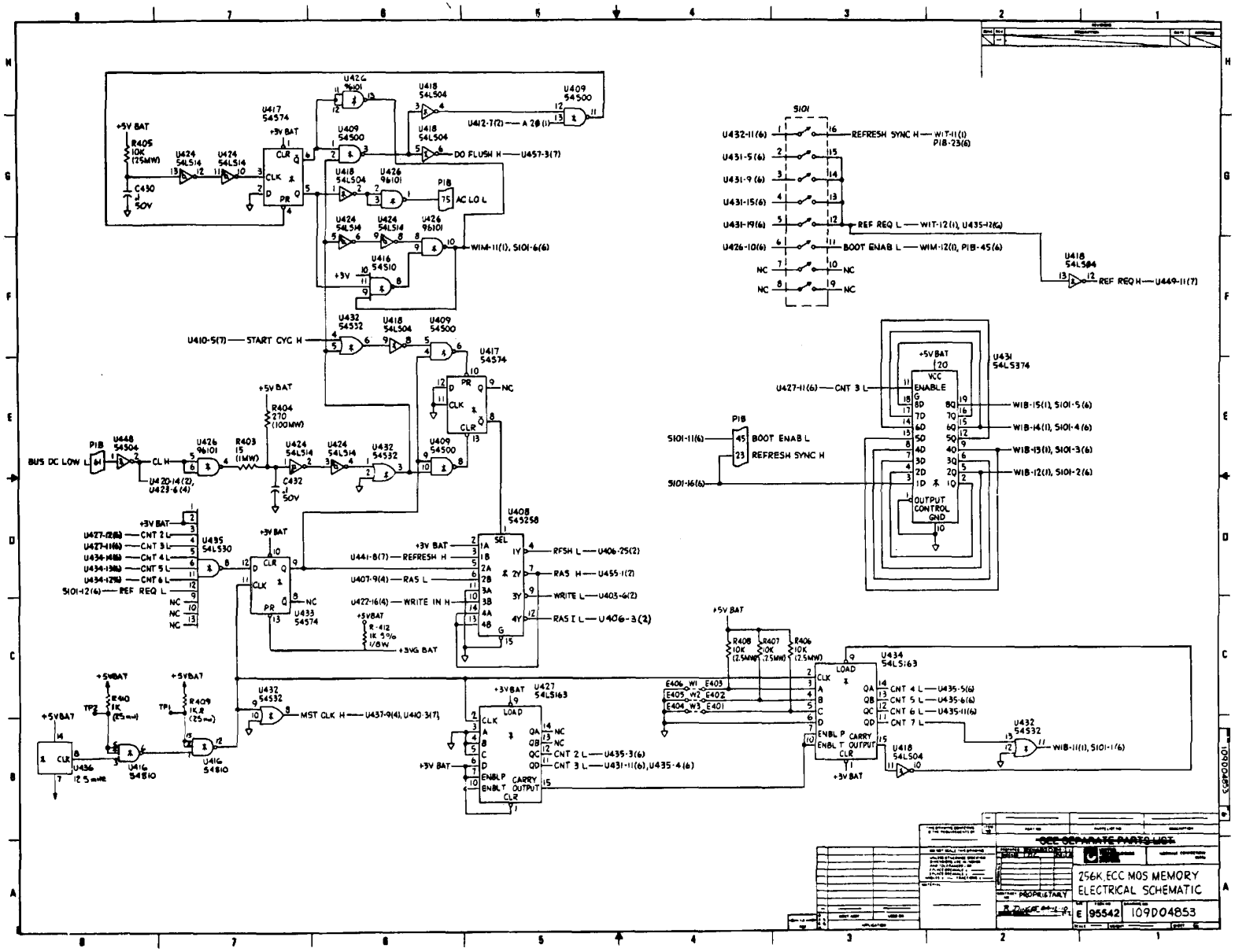
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 3 of 16)



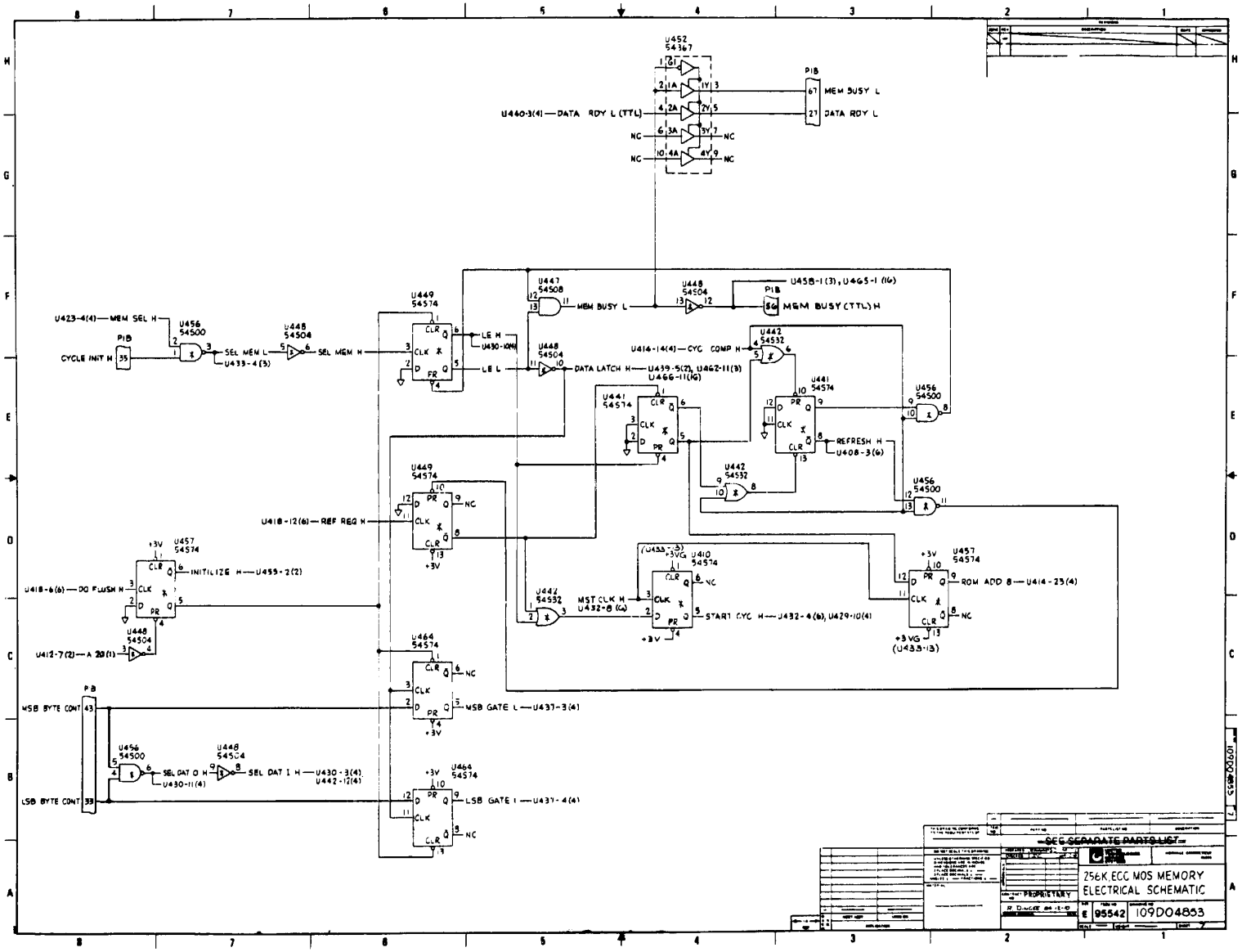
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 4 of 16)



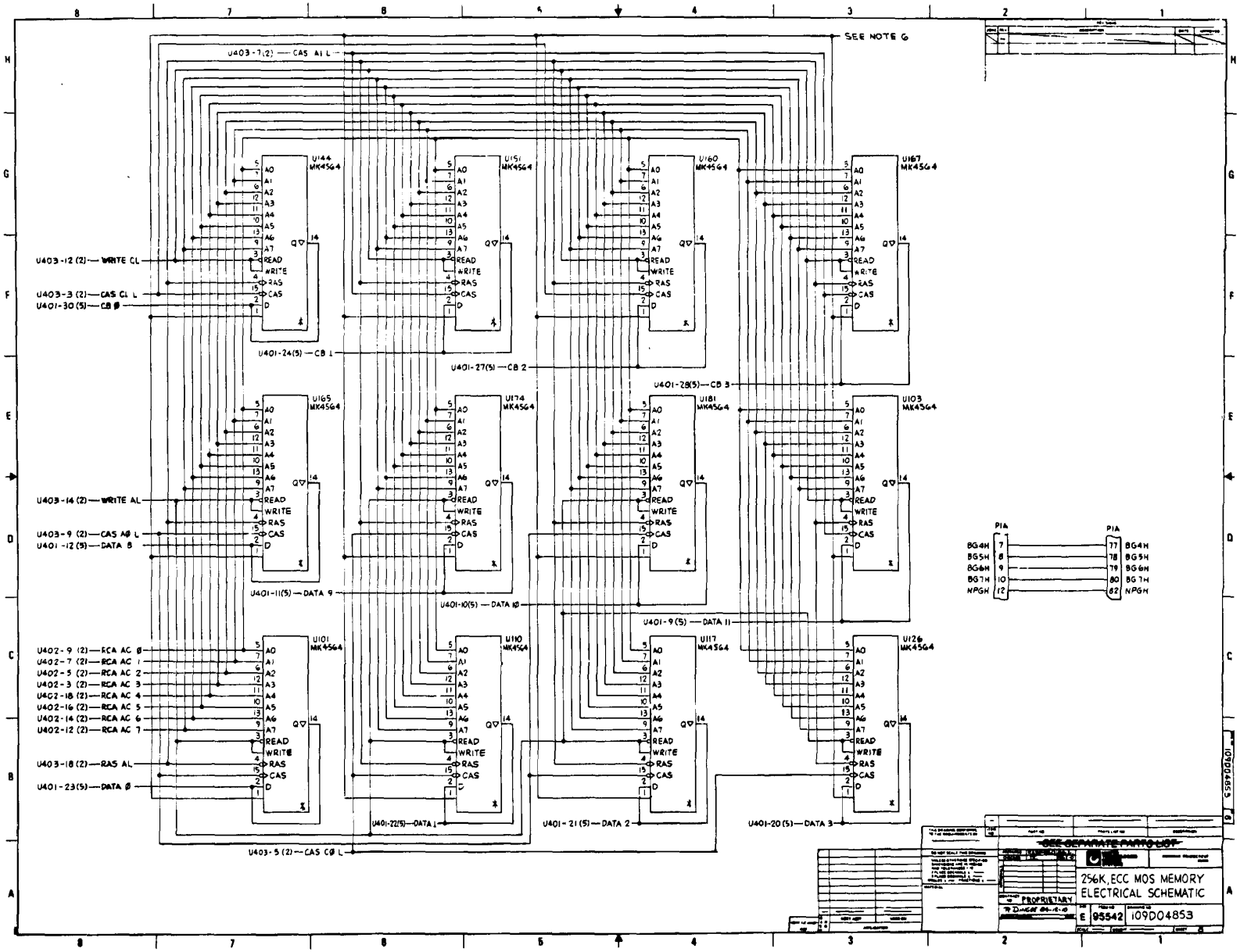
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 5 of 16)



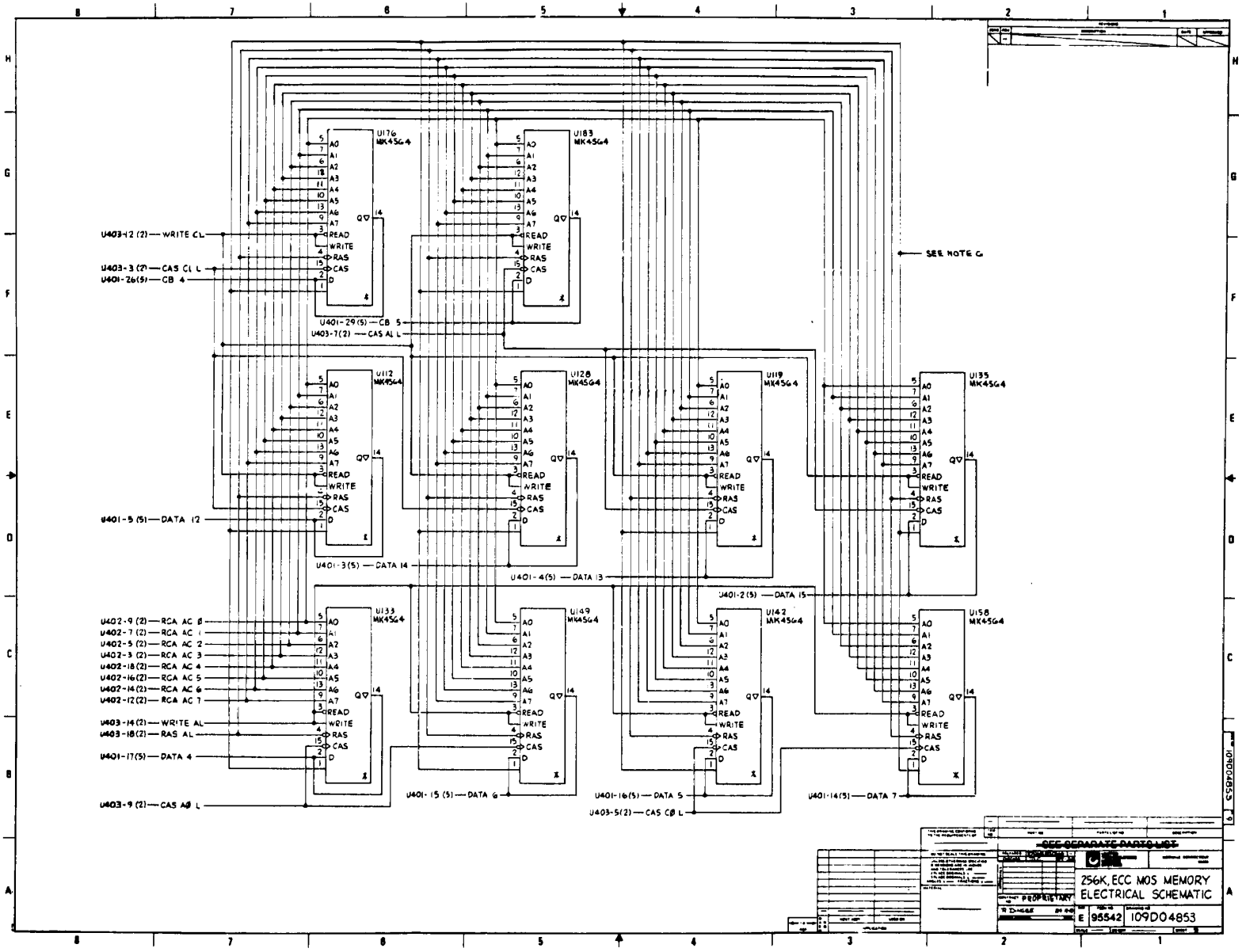
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 6 of 16)



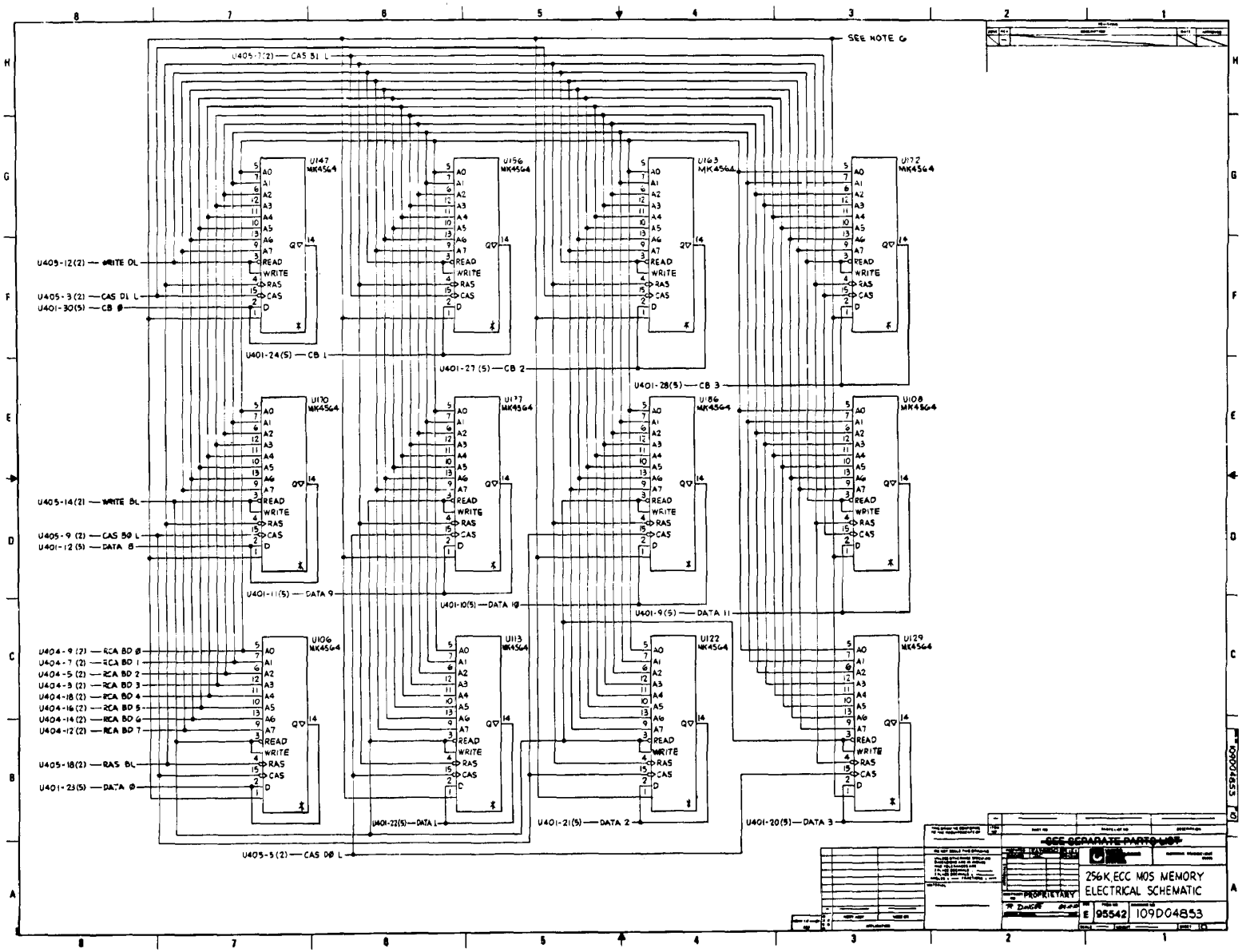
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 7 of 16)



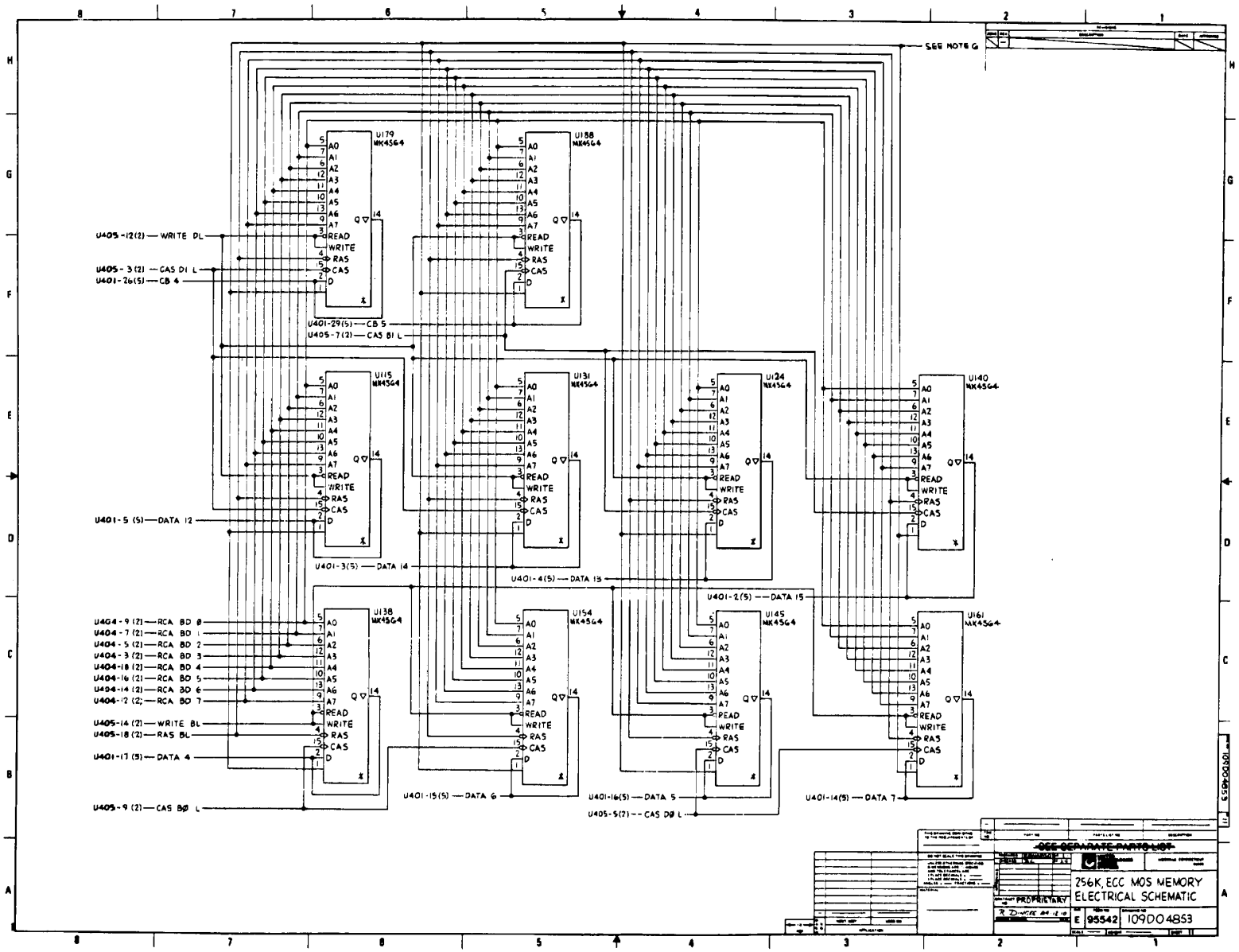
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 8 of 16)



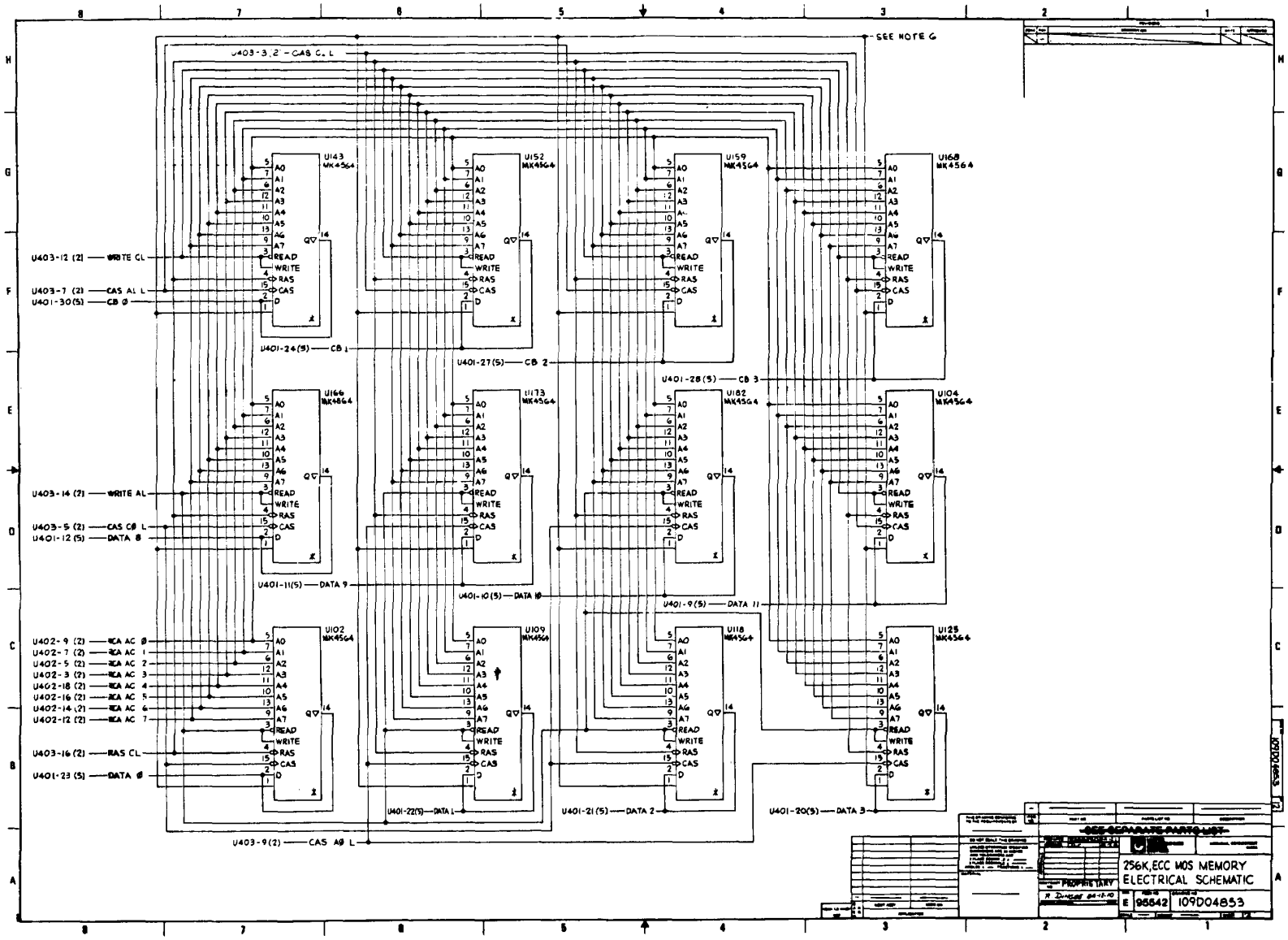
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 9 of 16)



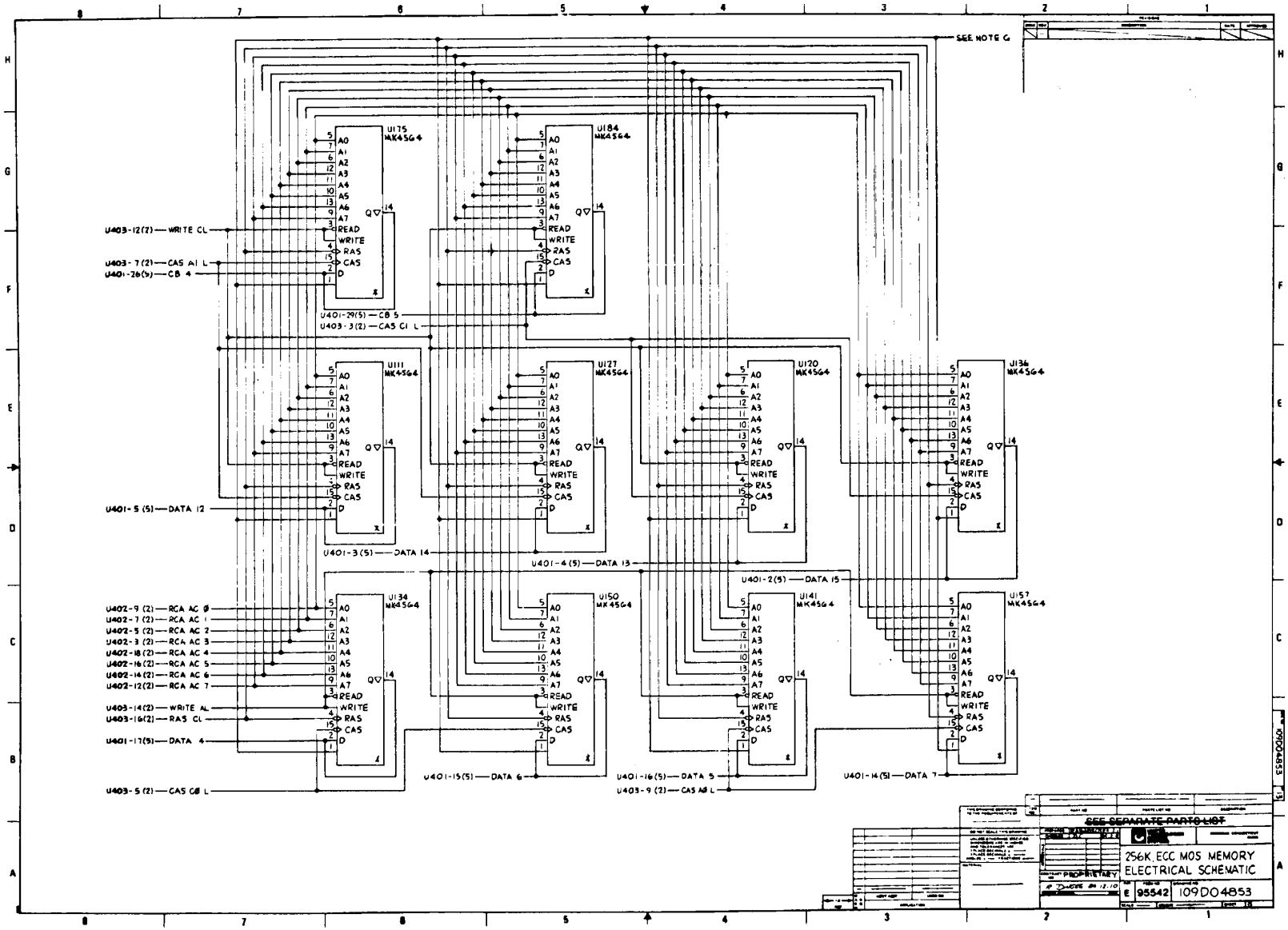
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 10 of 16)



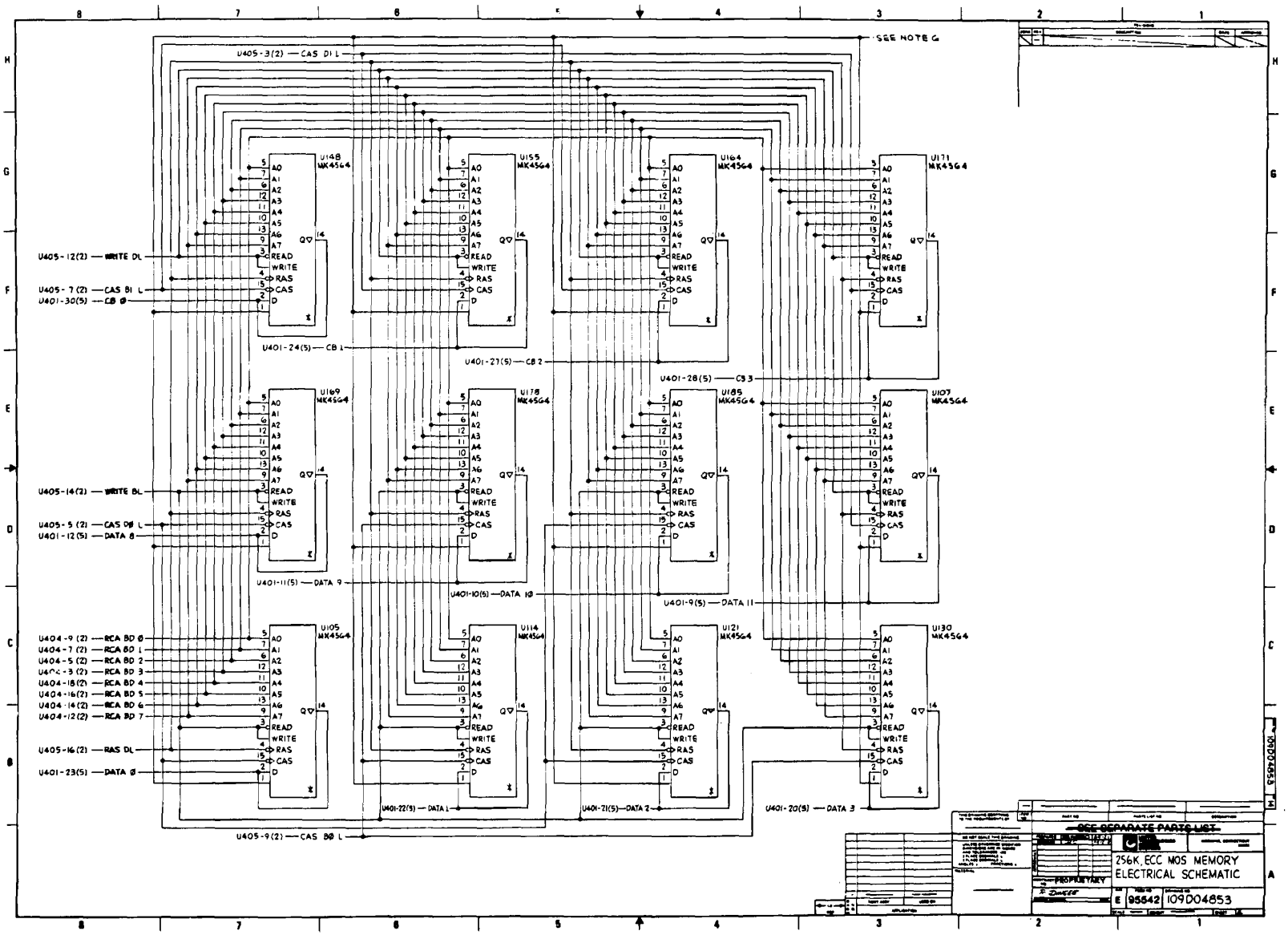
256K (WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 11 of 16)



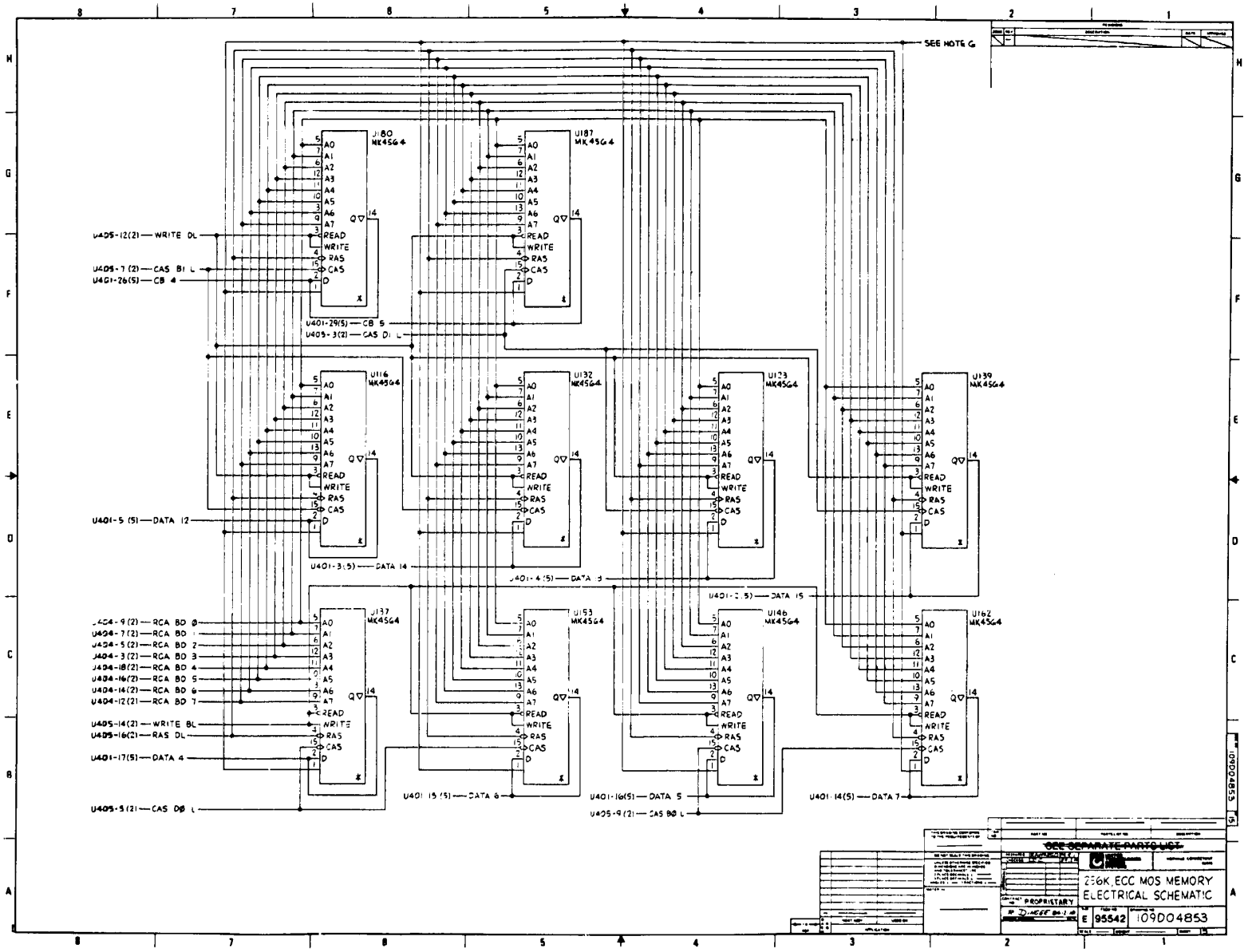
256K(WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 12 of 16)



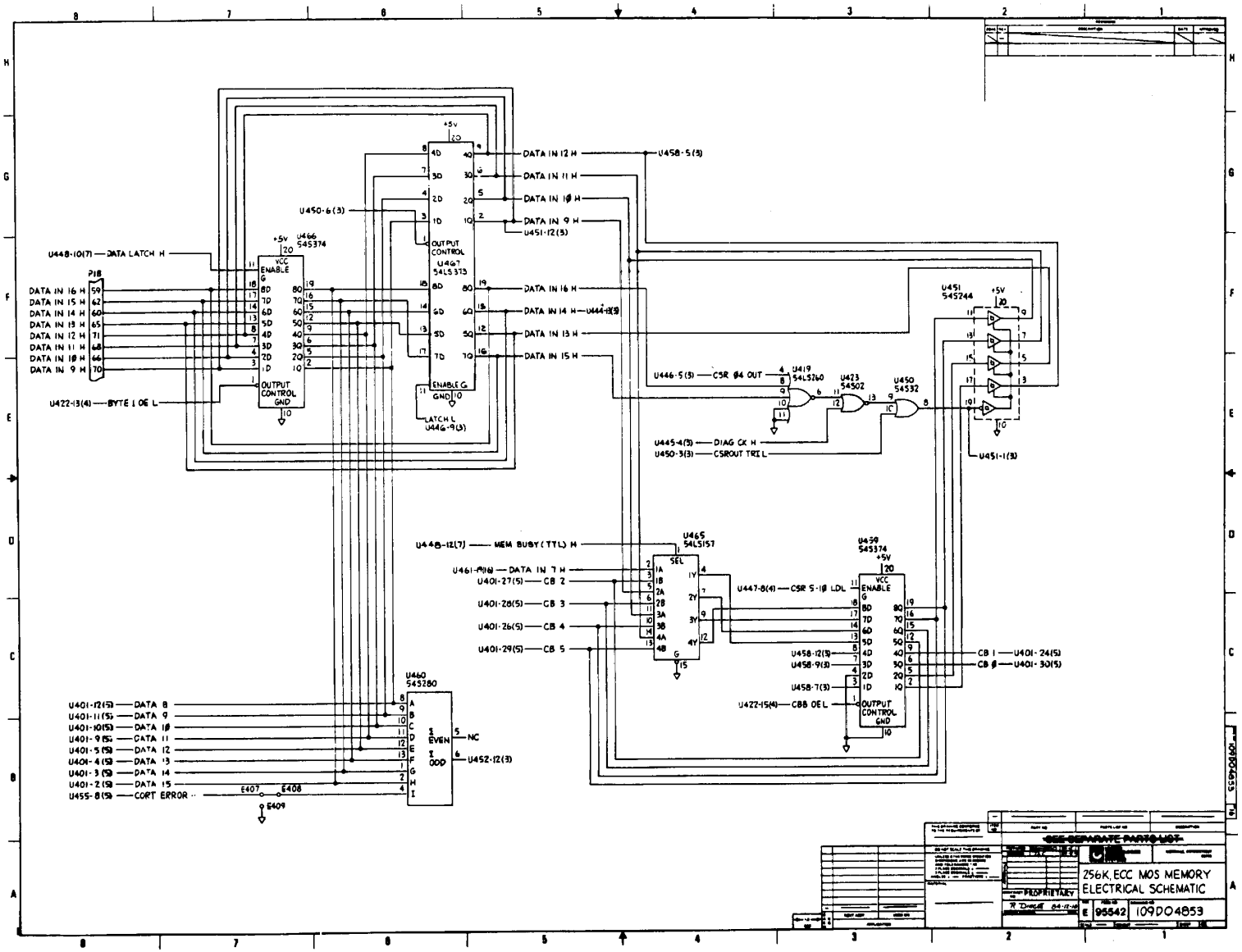
256K(WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 13 of 16)



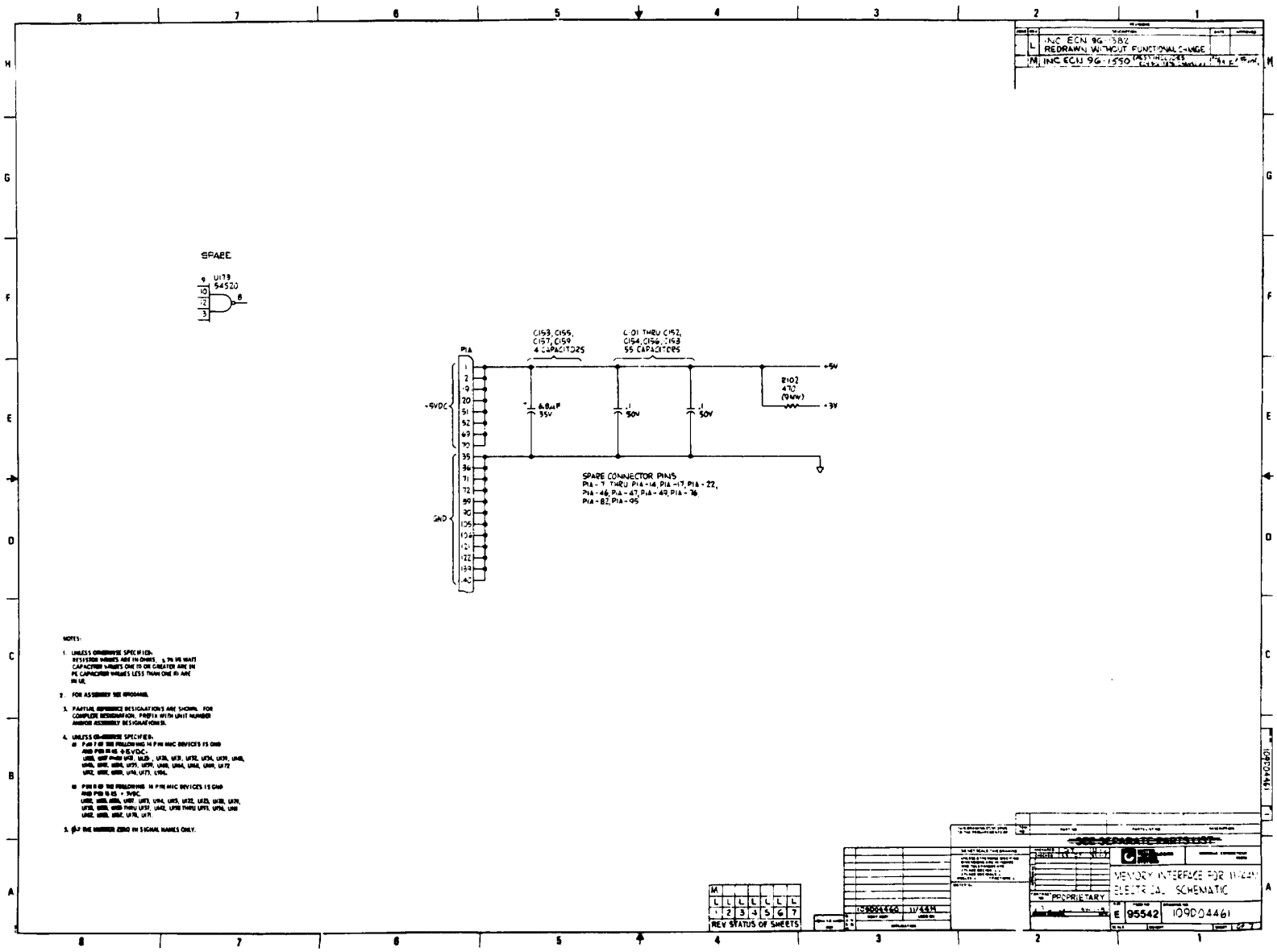
256K(WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 14 of 16)



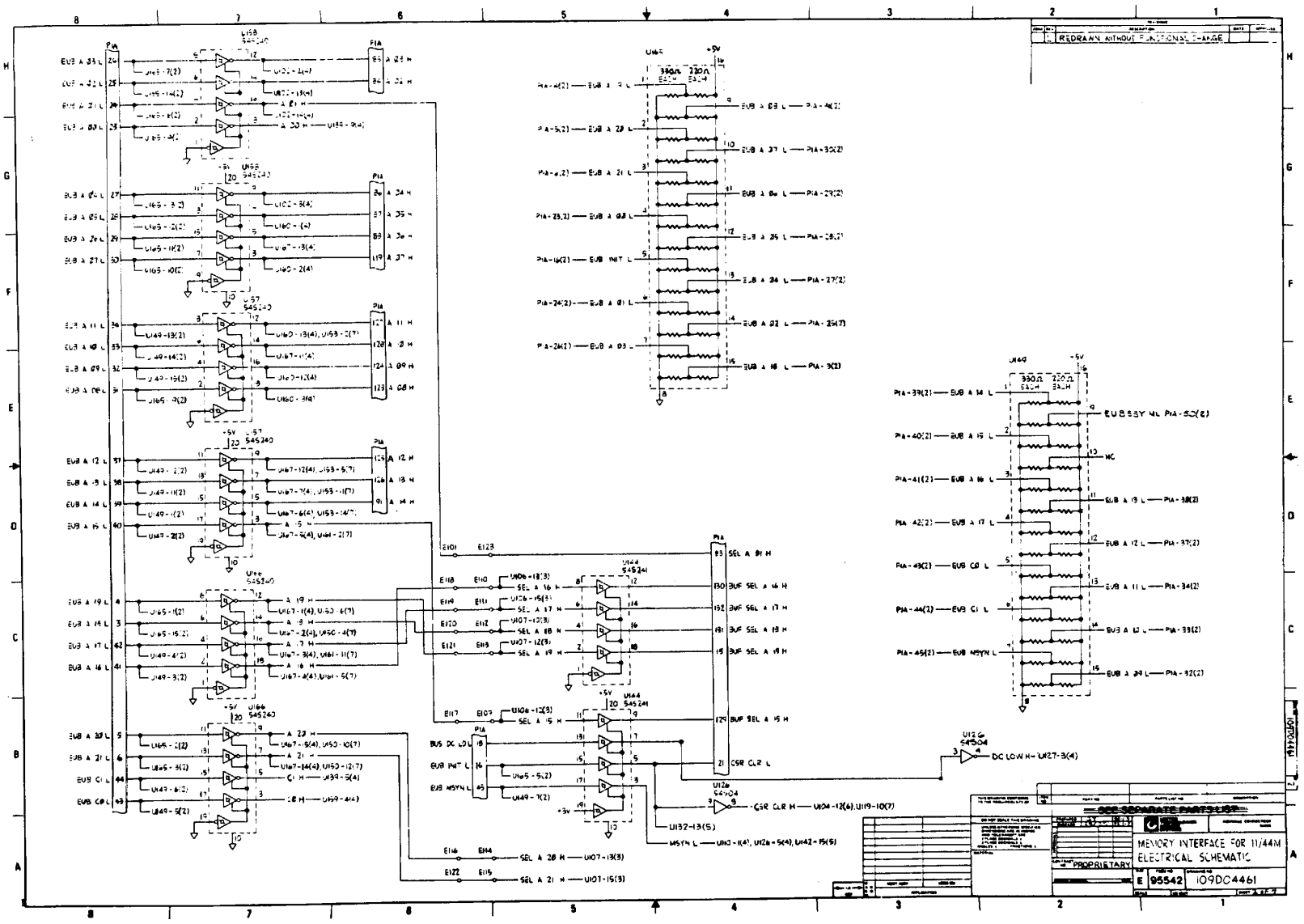
256K(WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 15 of 16)



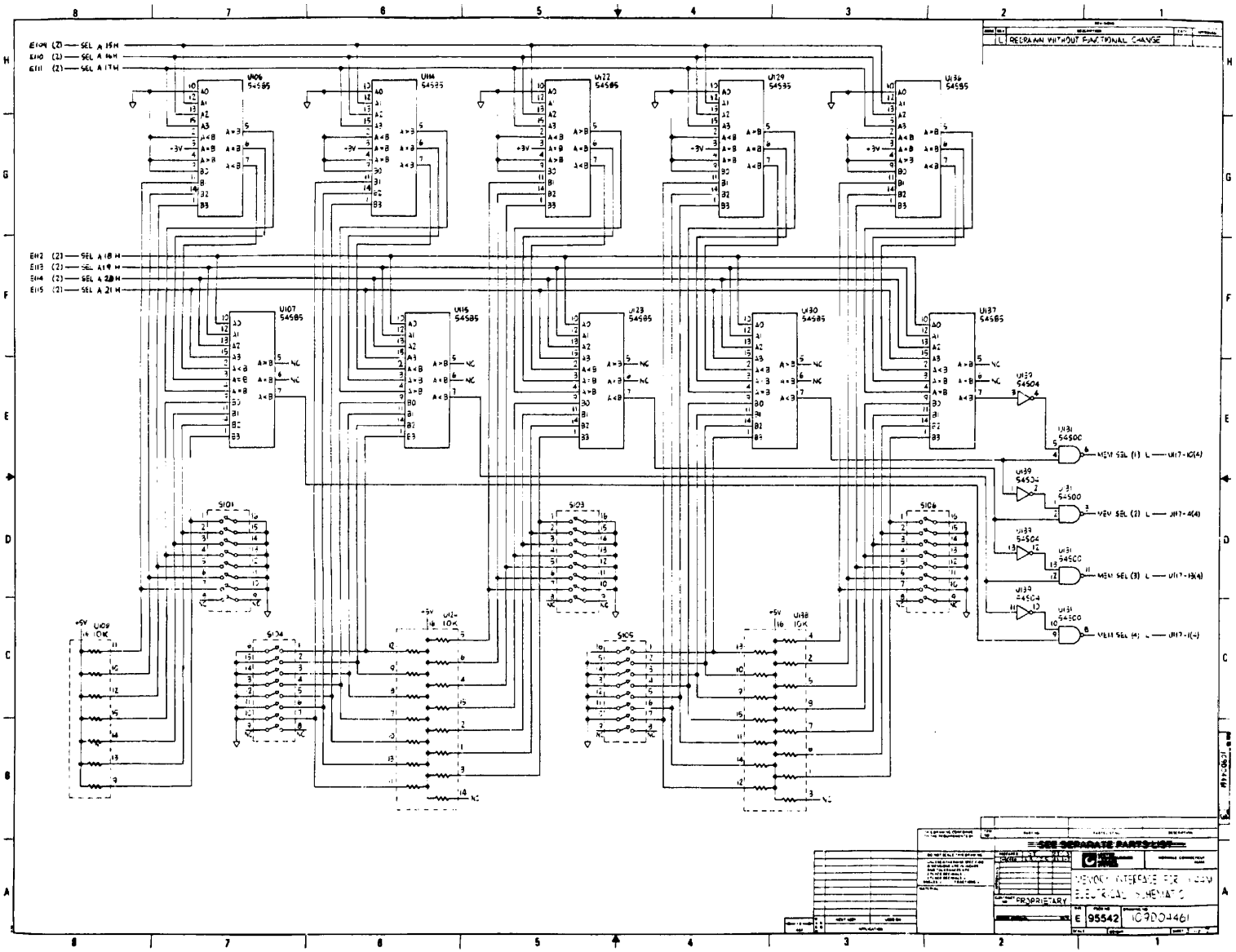
256K(WORD) ECC MOS MEMORY
SCHEMATIC (Sheet 16 of 16)



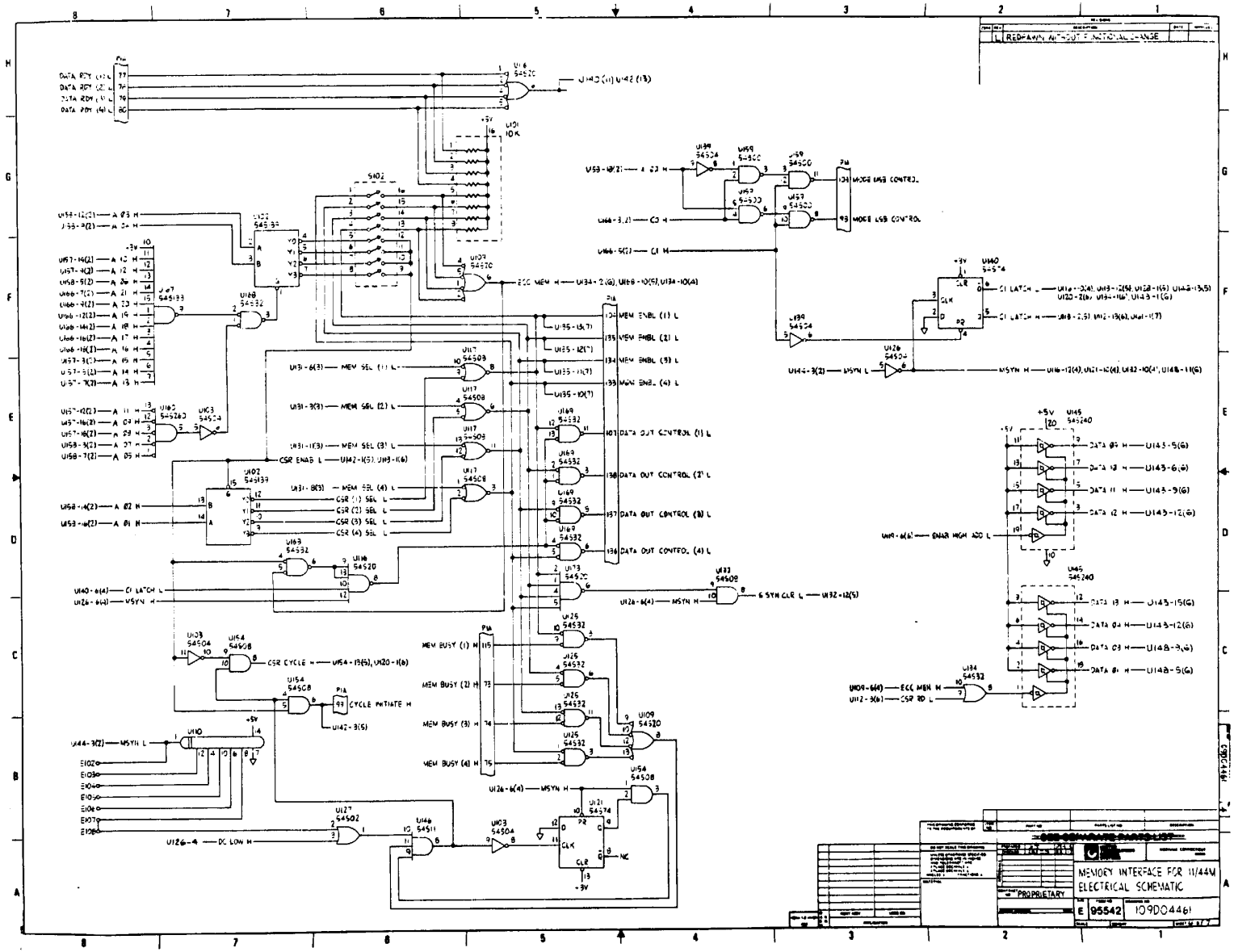
MEMORY I/F SCHEMATIC
I-I (Sheet 1 of 7)



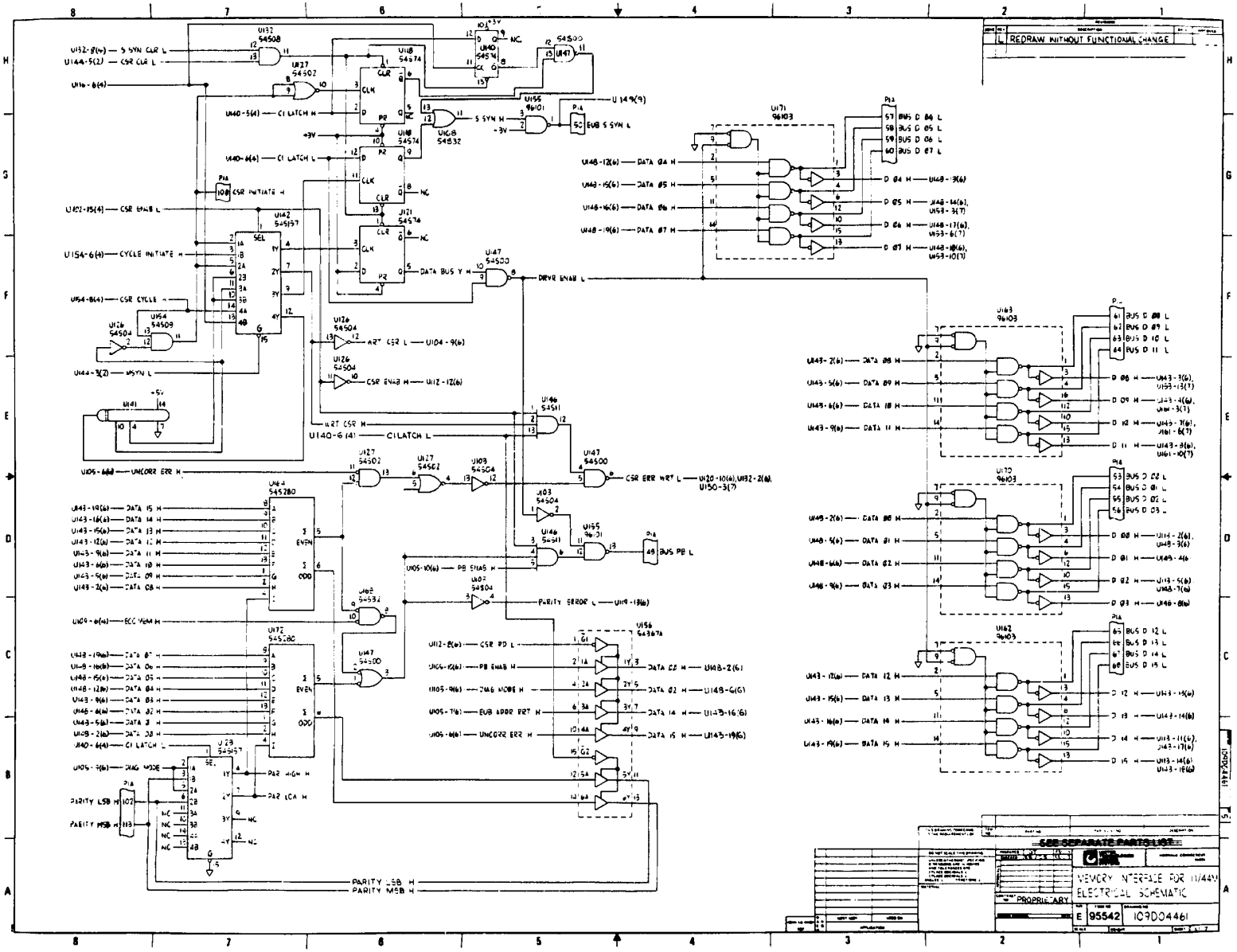
MEMORY I/F SCHEMATIC
(Sheet 2 of 7)



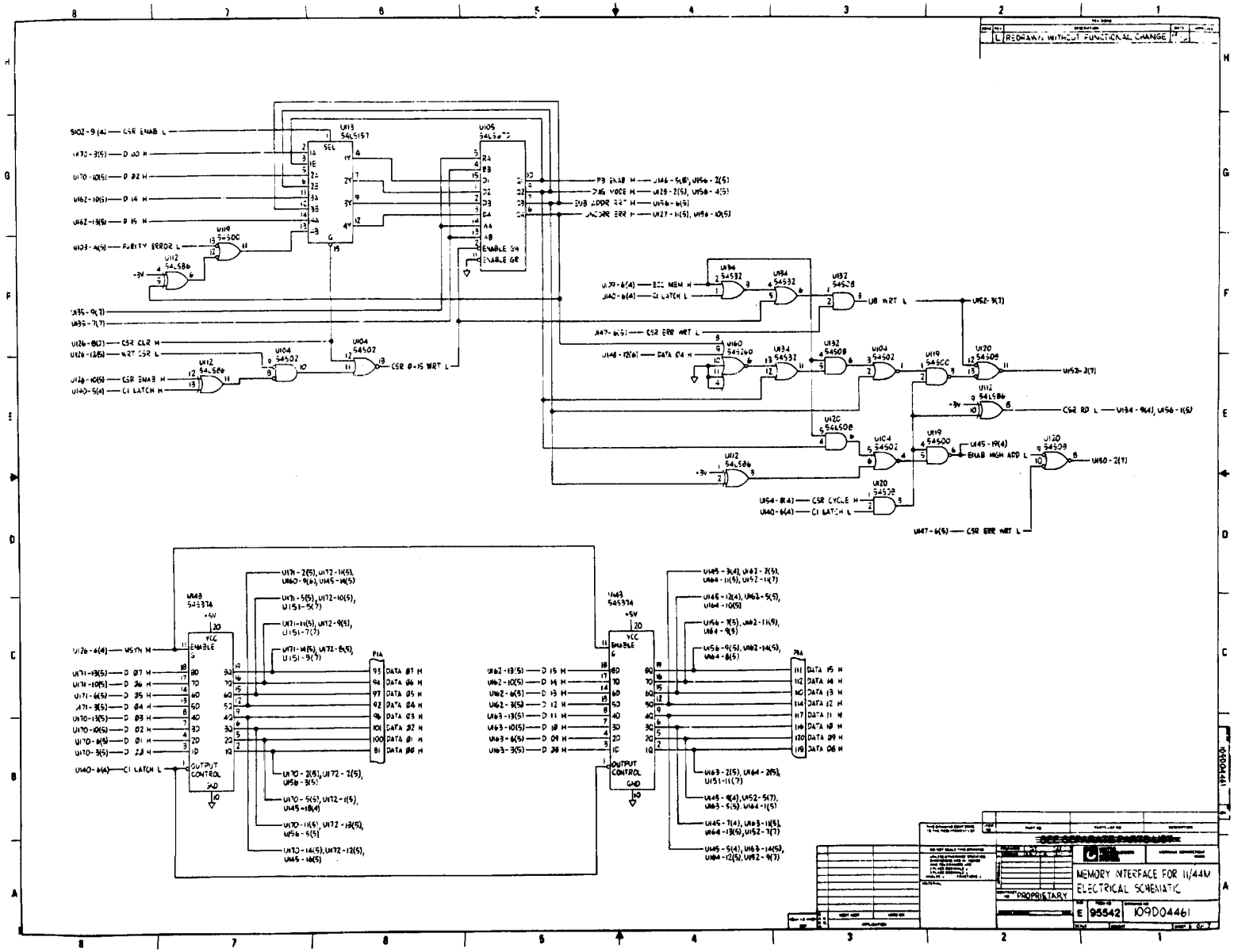
MEMORY I/F SCHEMATIC
(Sheet 3 of 7)



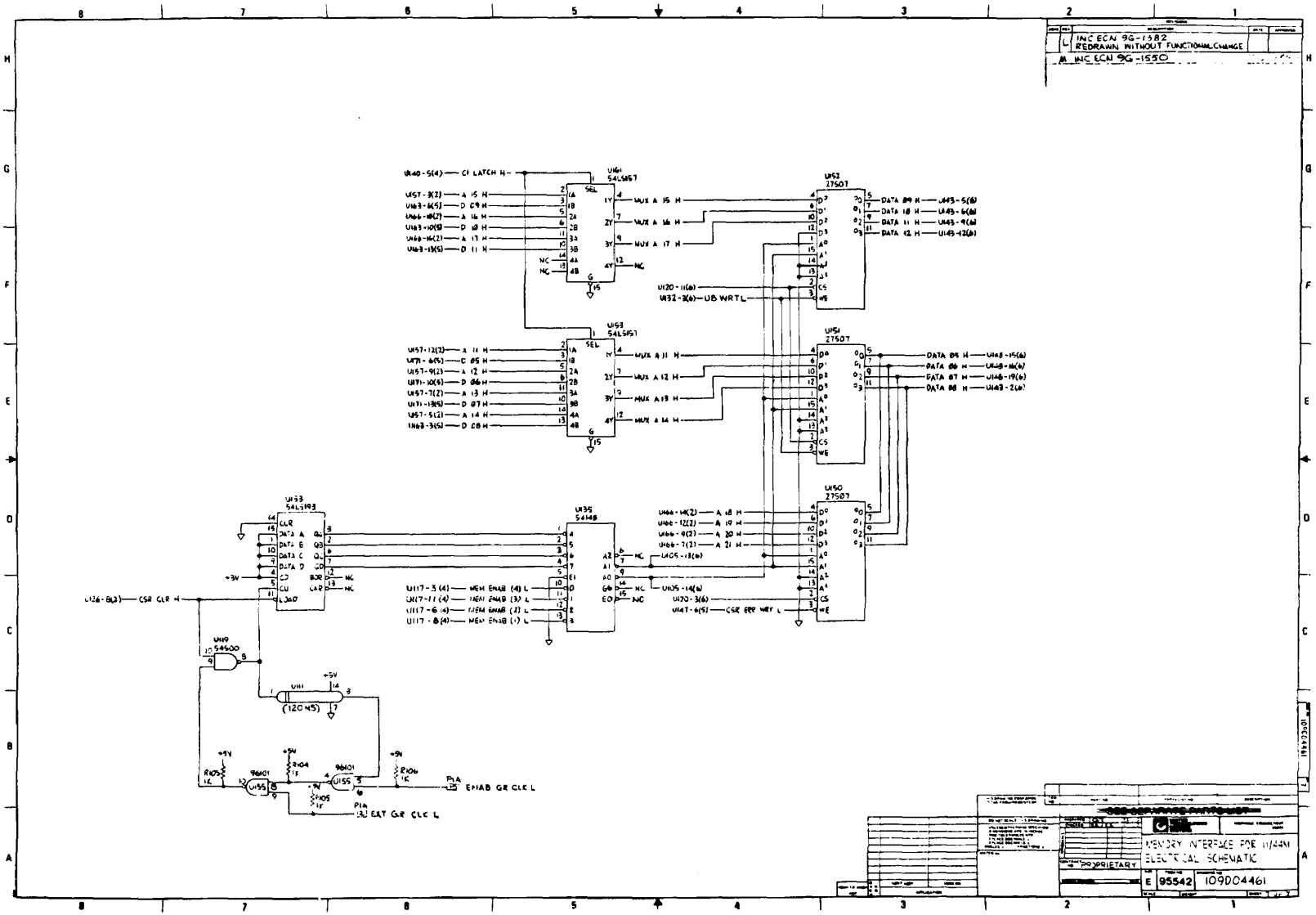
MEMORY I/F SCHEMATIC
(Sheet 4 of 7)



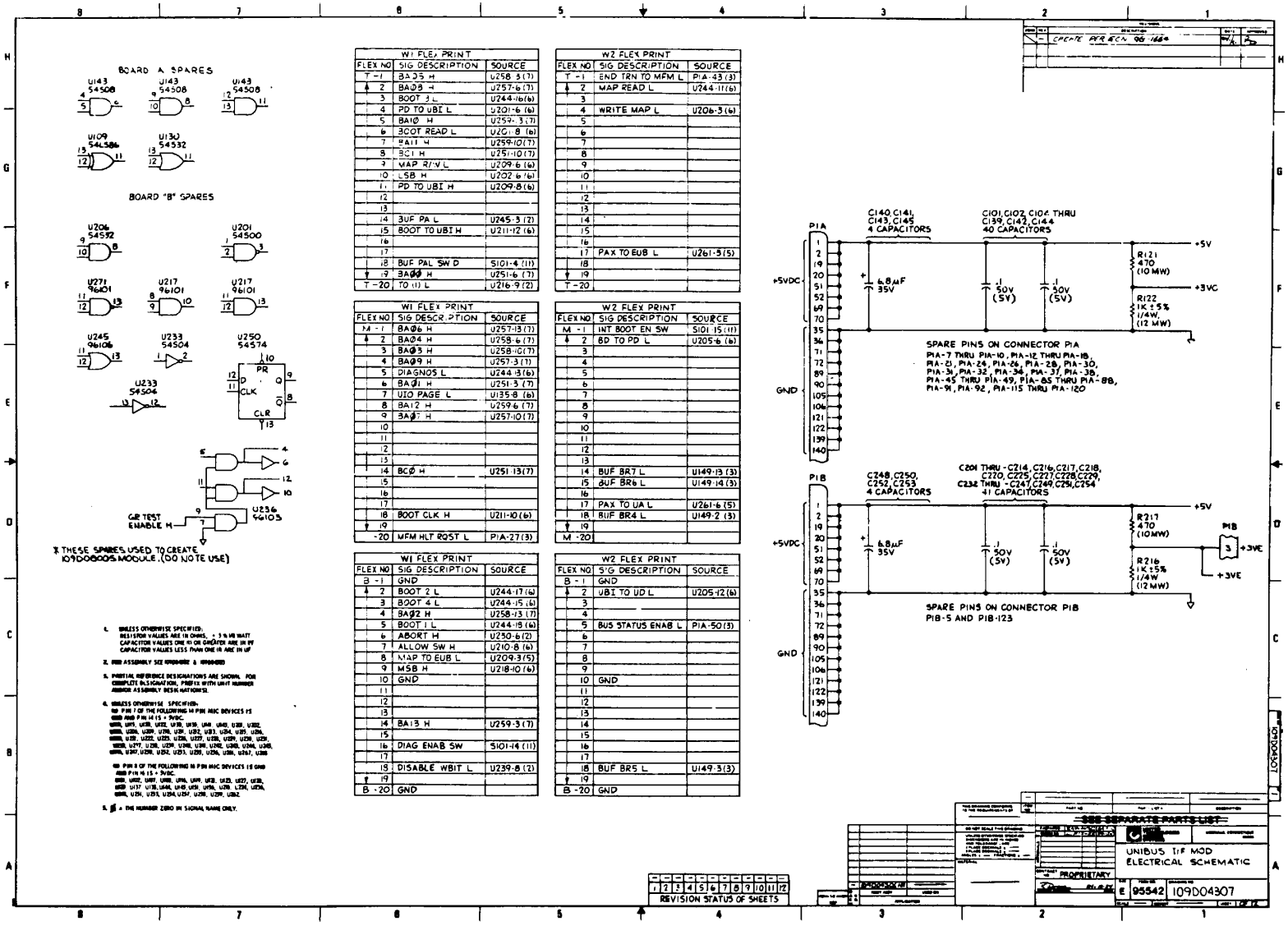
MEMORY I/F SCHEMATIC
(Sheet 5 of 7)



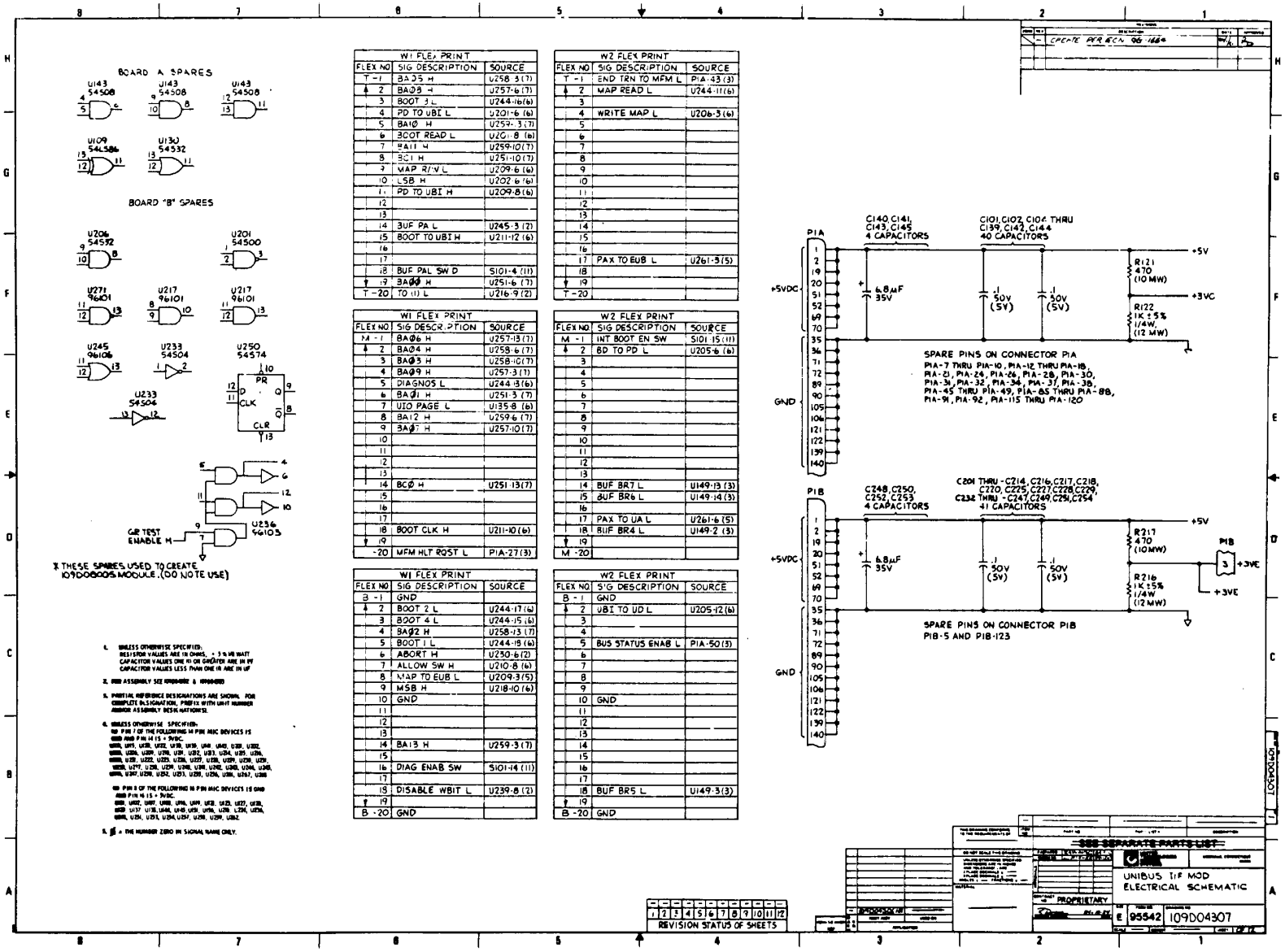
MEMORY I/F SCHEMATIC
(Sheet 6 of 7)



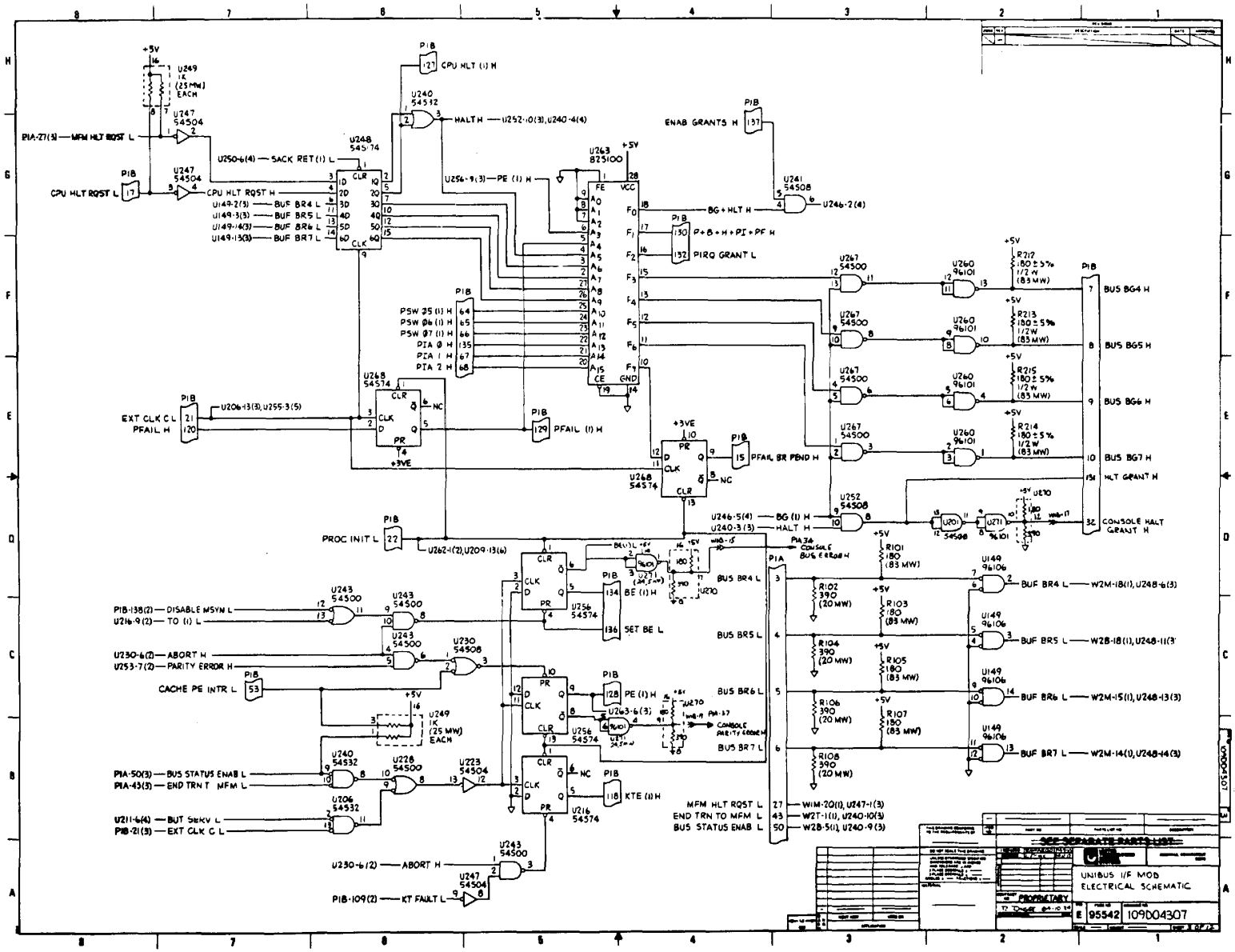
MEMORY I/F SCHEMATIC
(Sheet 7 of 7)



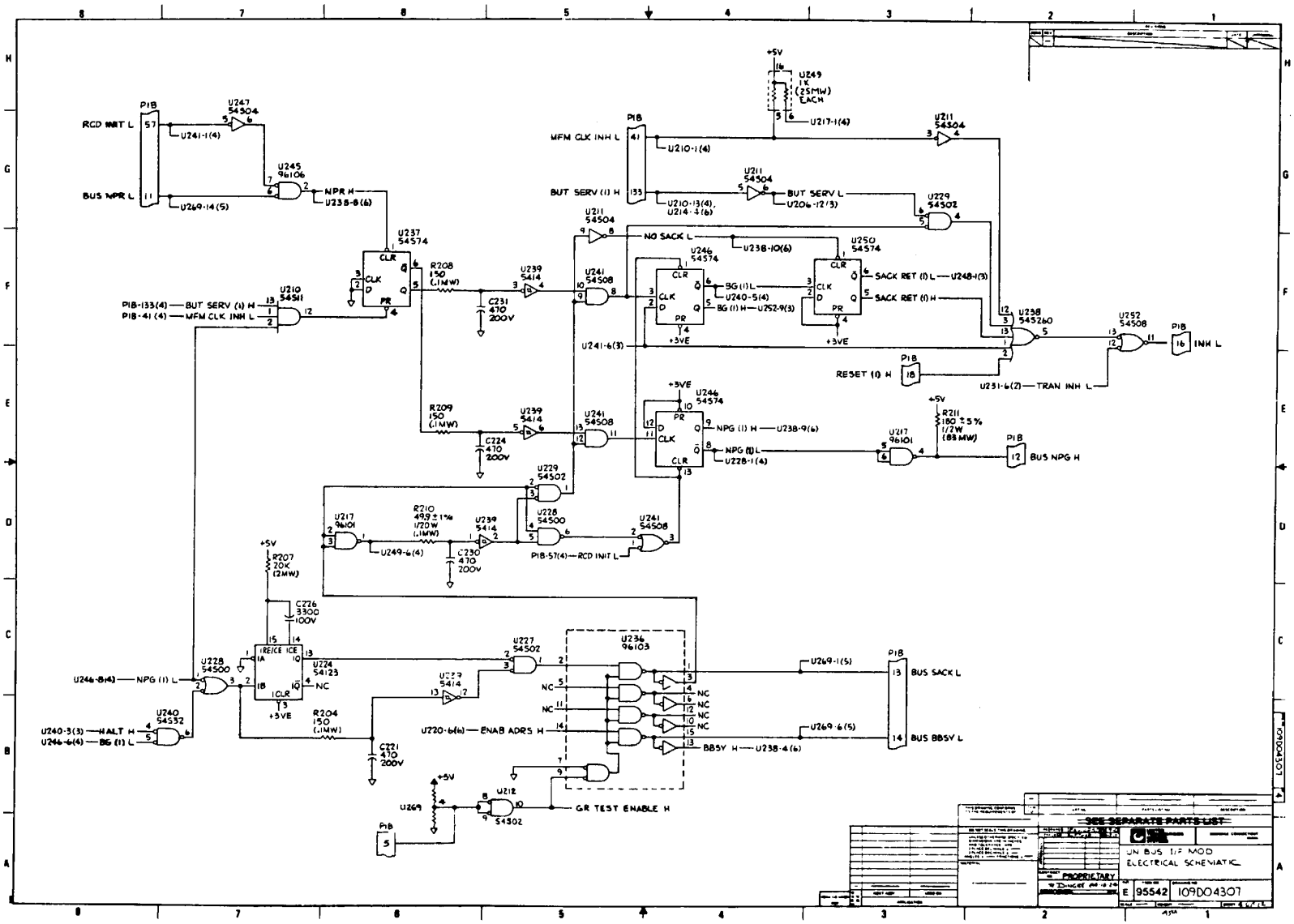
UNIBUS IF SCHEMATIC
(Sheet 1 of 12)



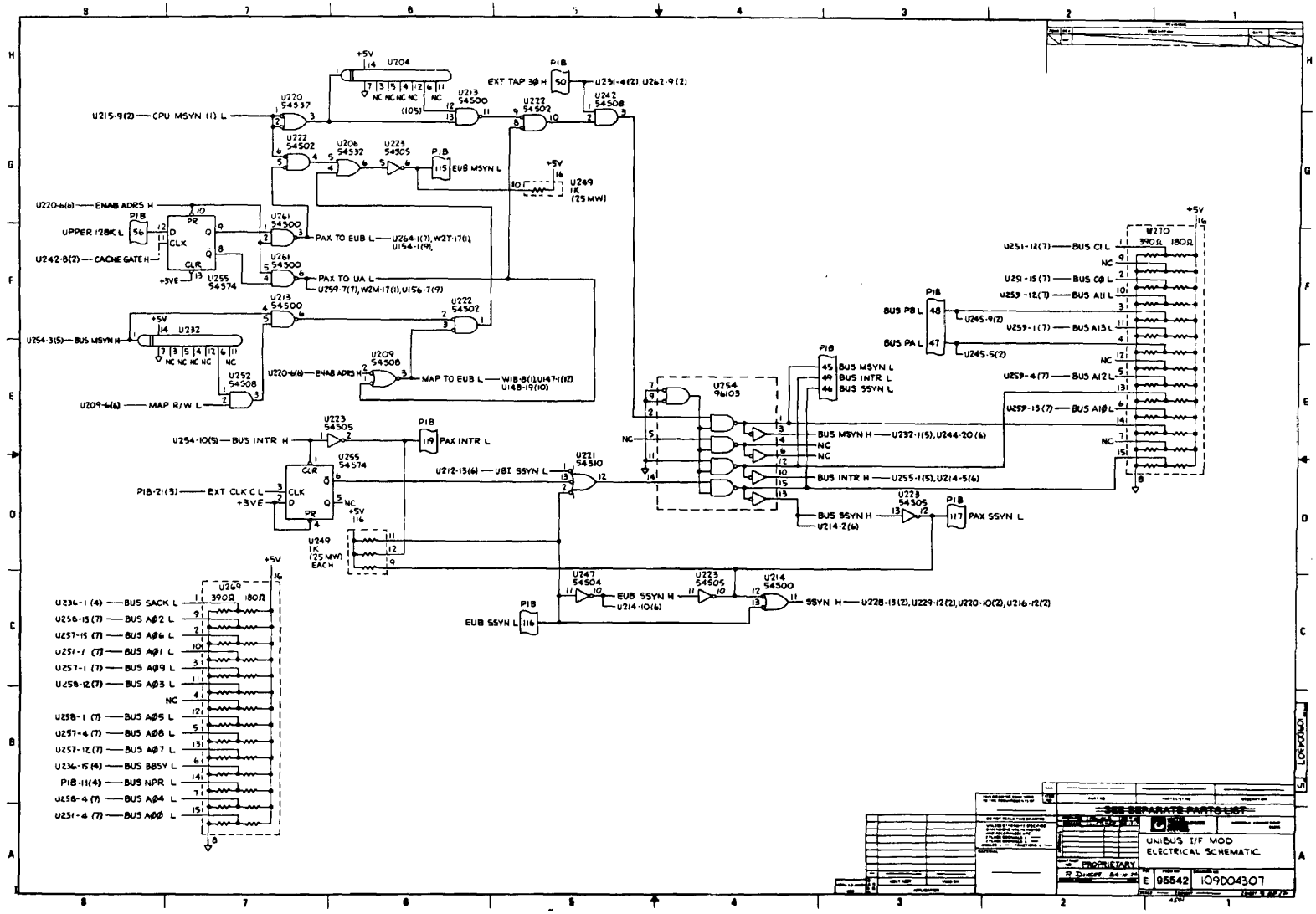
UNIBUS IF SCHEMATIC
(Sheet 2 of 12)



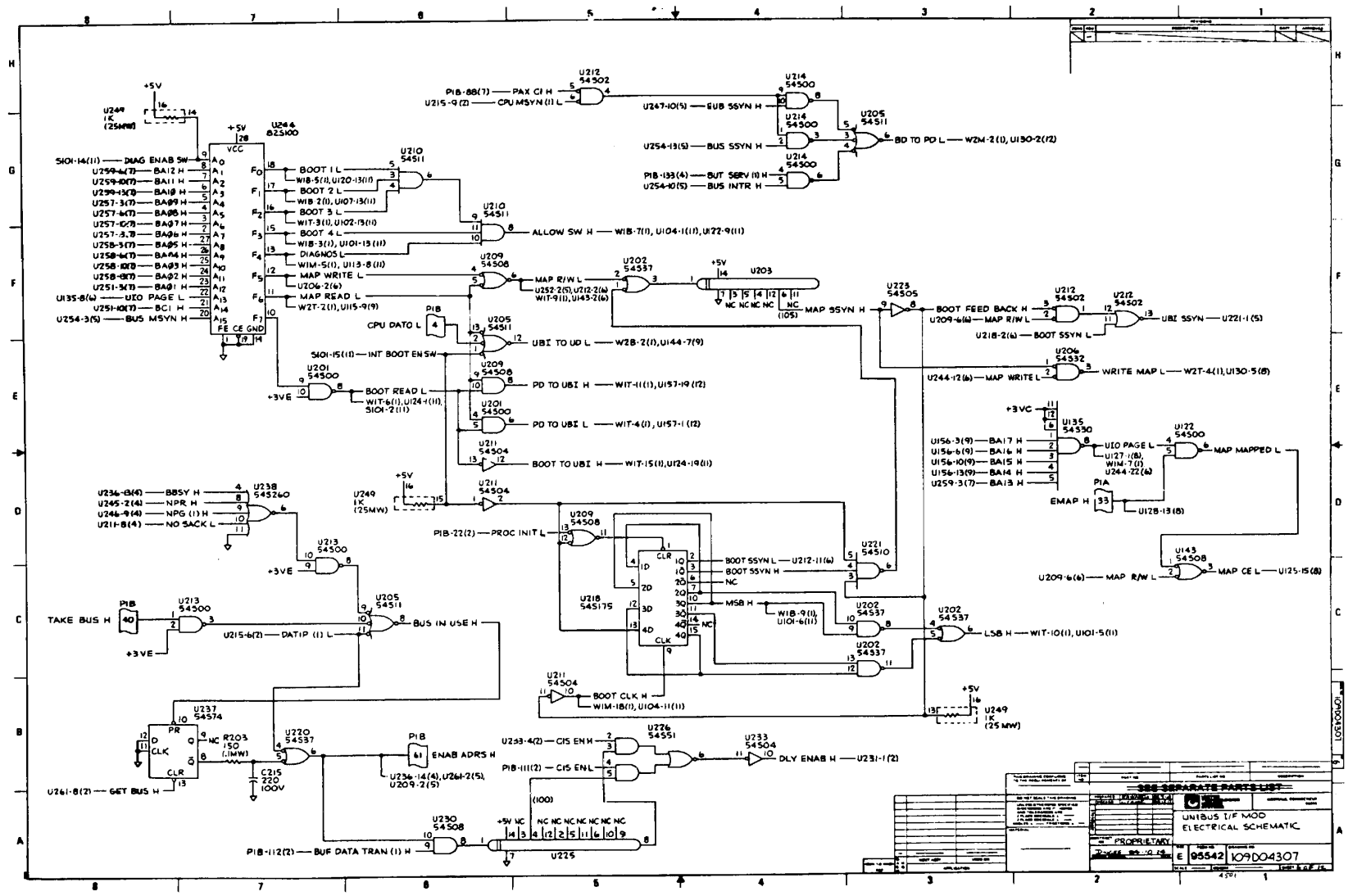
UNIBUS IF SCHEMATIC I-27
(Sheet 3 of 12)



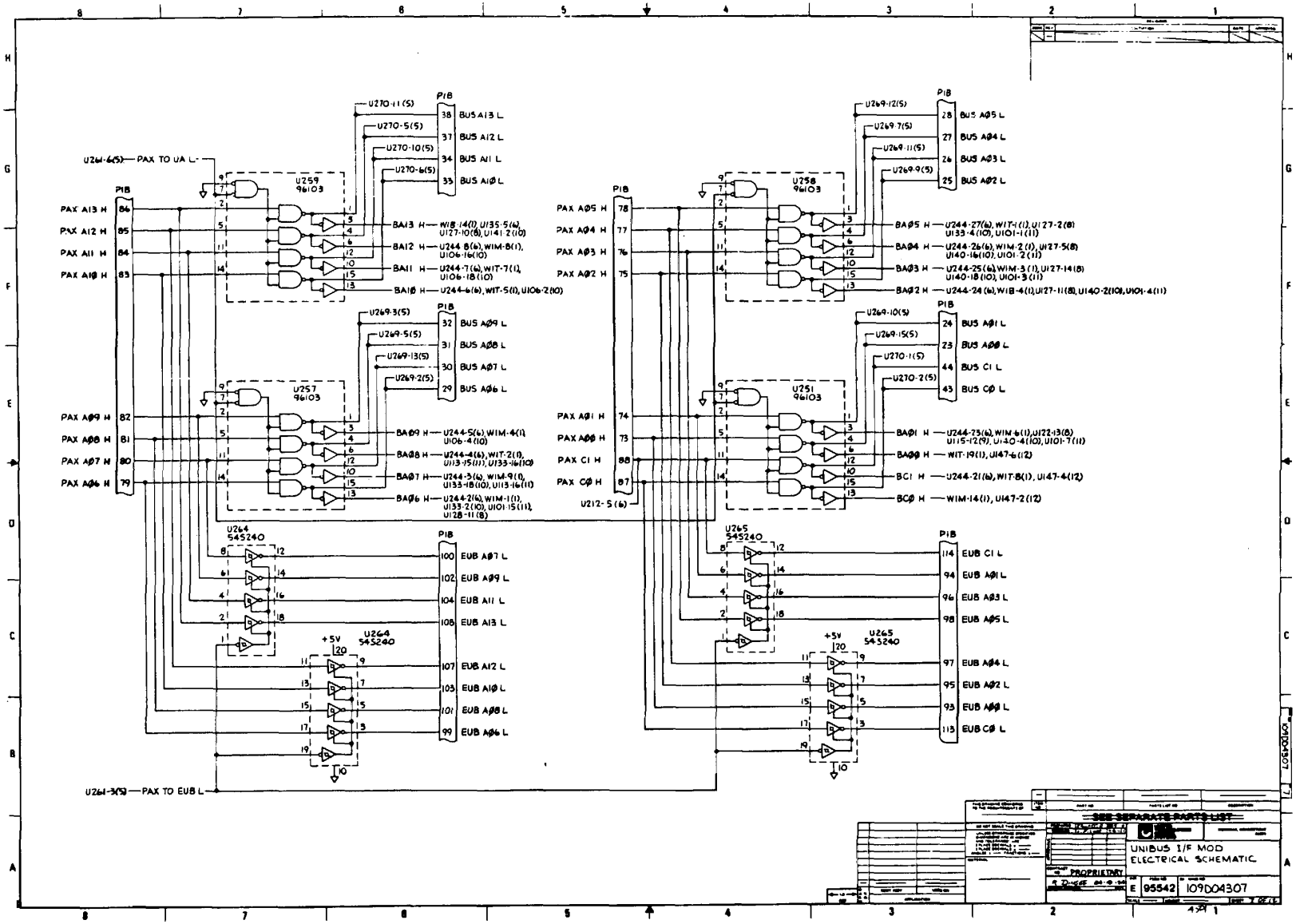
UNIBUS IF SCHEMATIC
(Sheet 4 of 12)



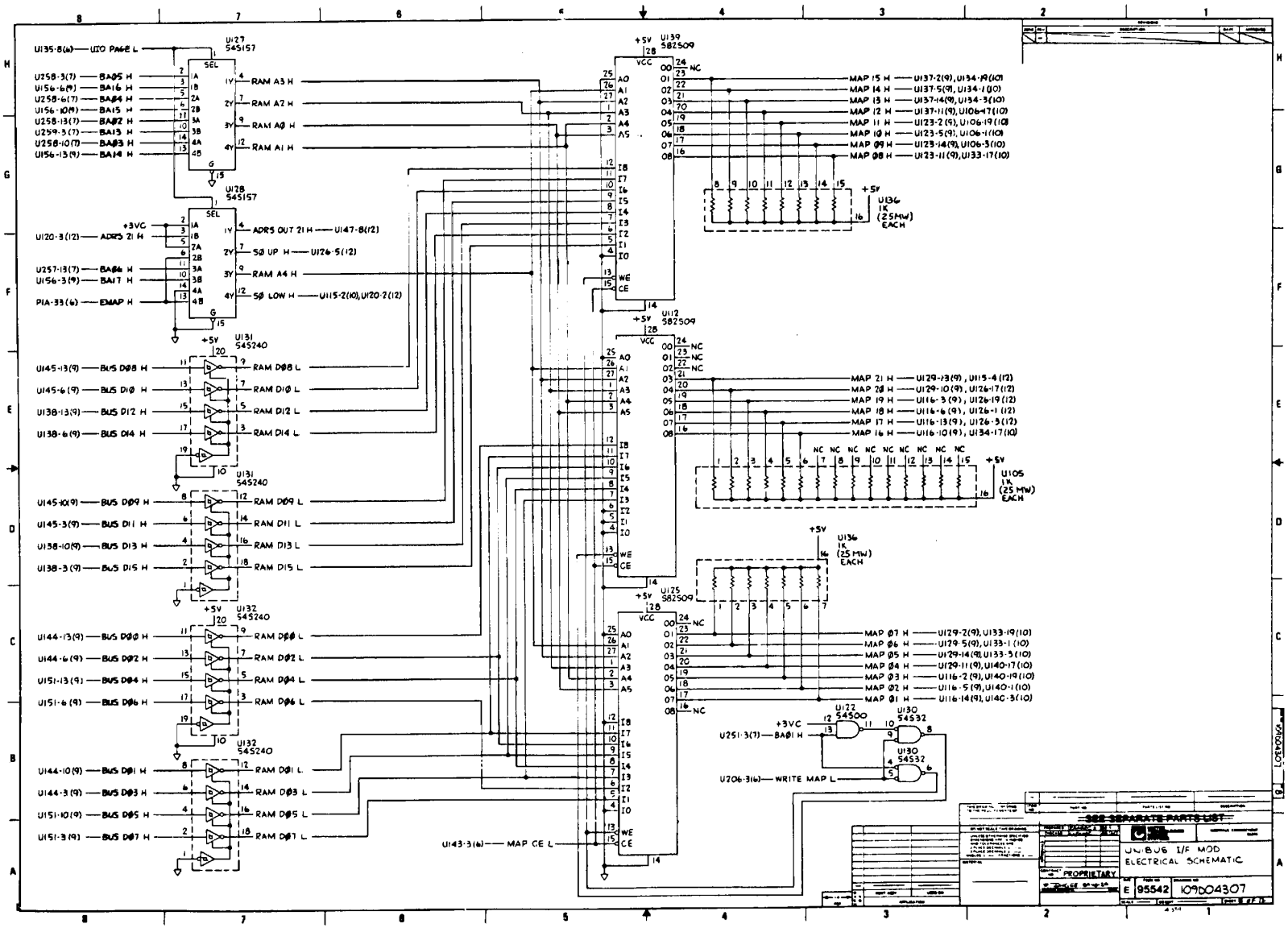
UNIBUS IF SCHEMATIC
(Sheet 5 of 12)



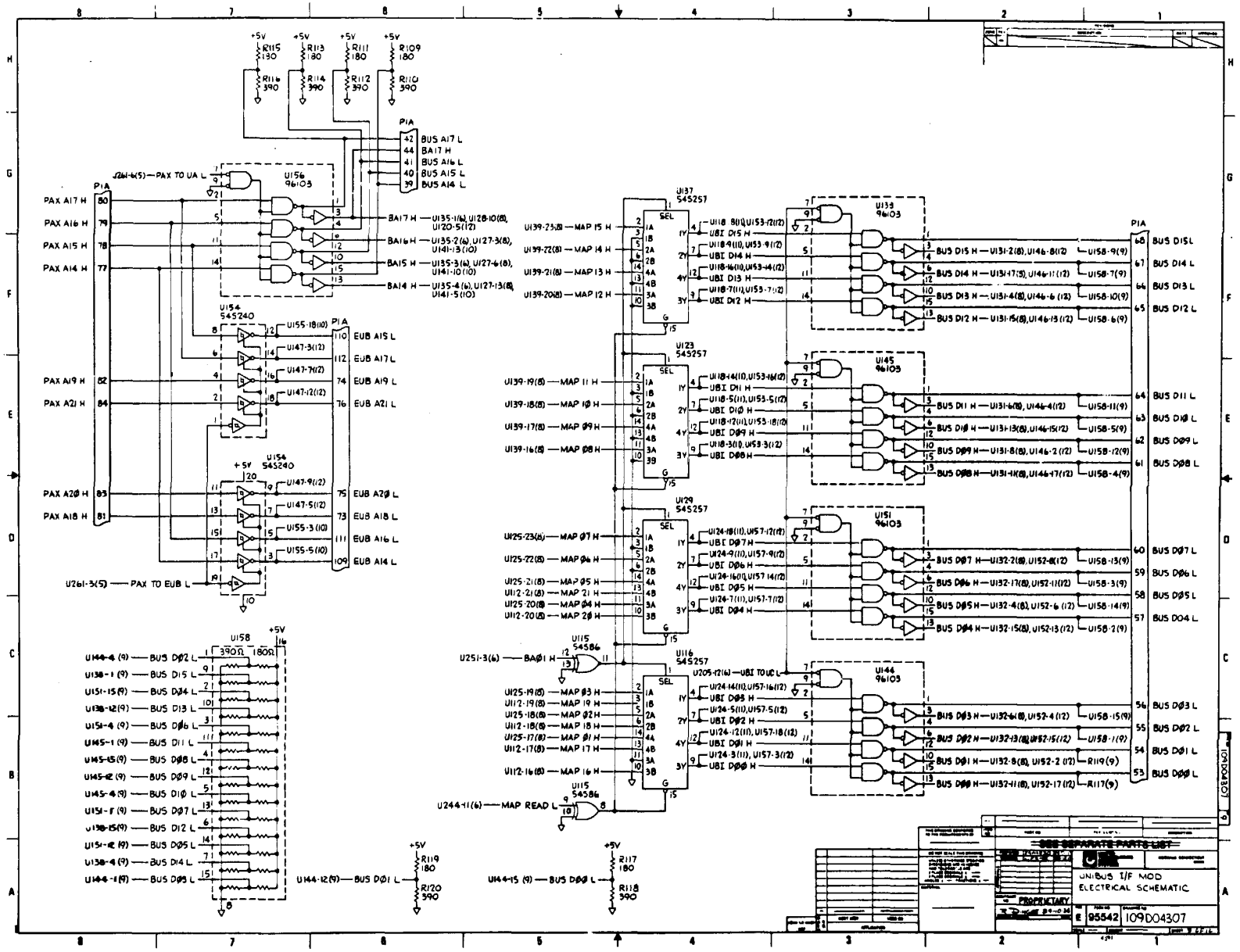
UNIBUS IF SCHEMATIC
(Sheet 6 of 12)



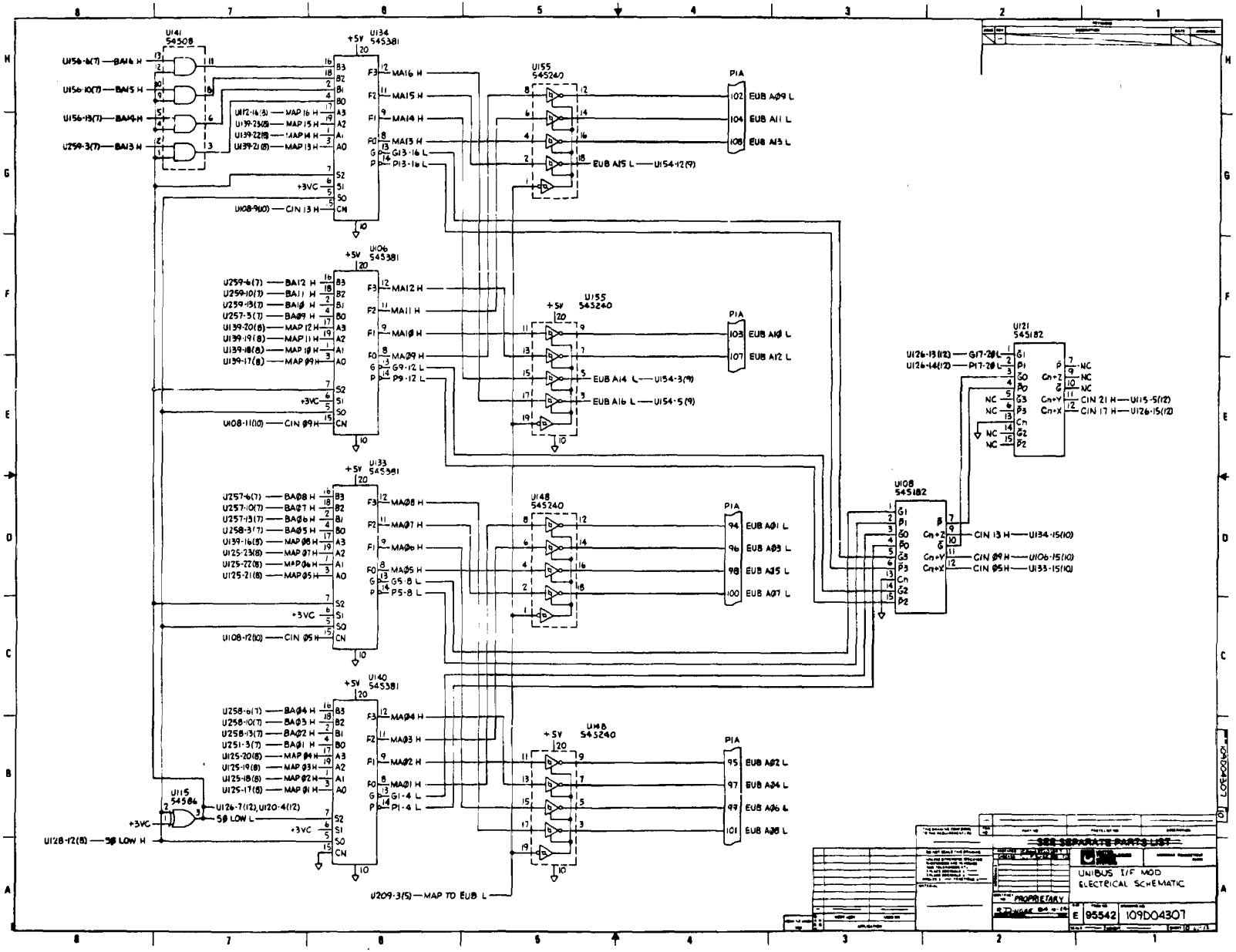
UNIBUS IF SCHEMATIC
(Sheet 7 of 12)



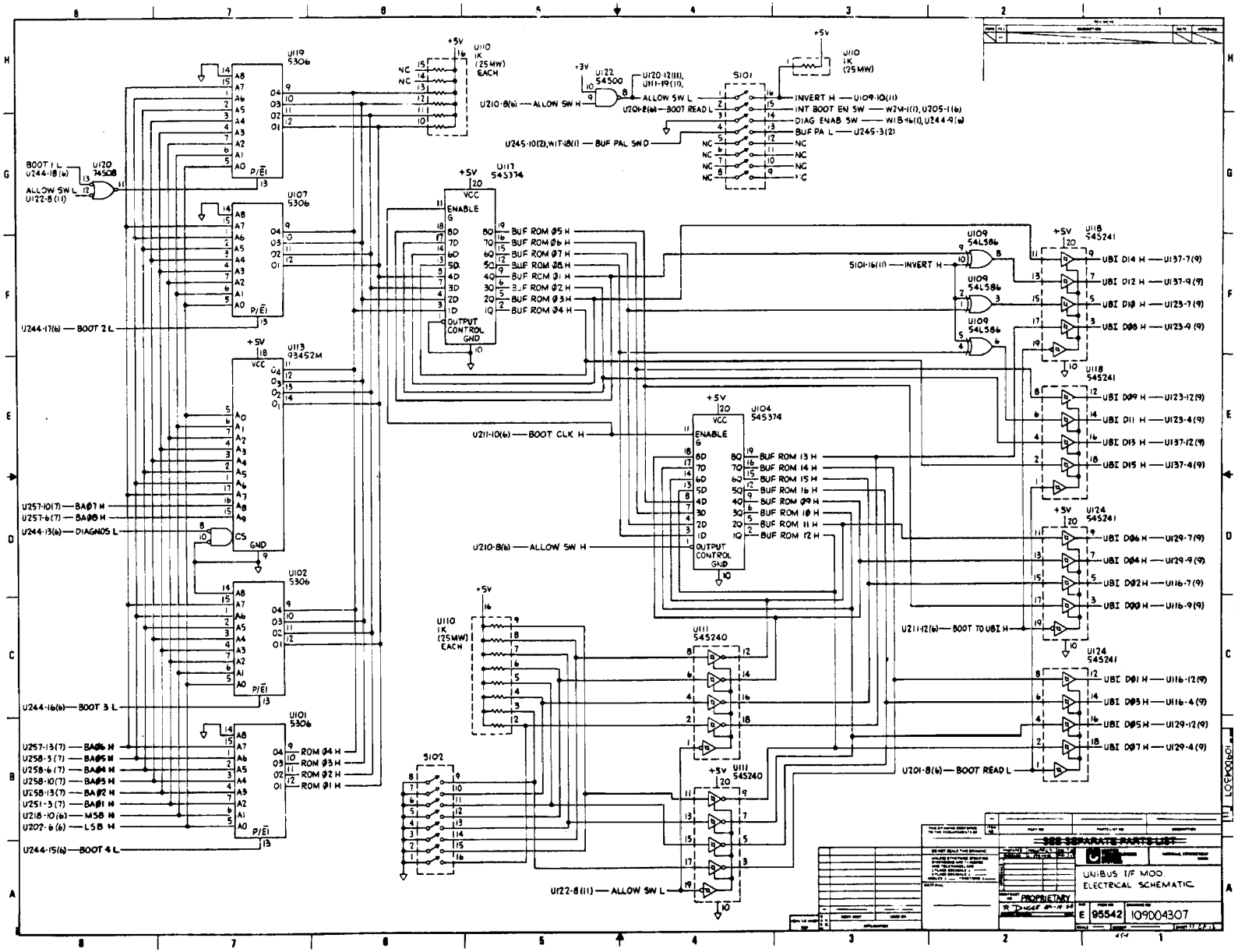
UNIBUS IF SCHEMATIC
(Sheet 8 of 12)



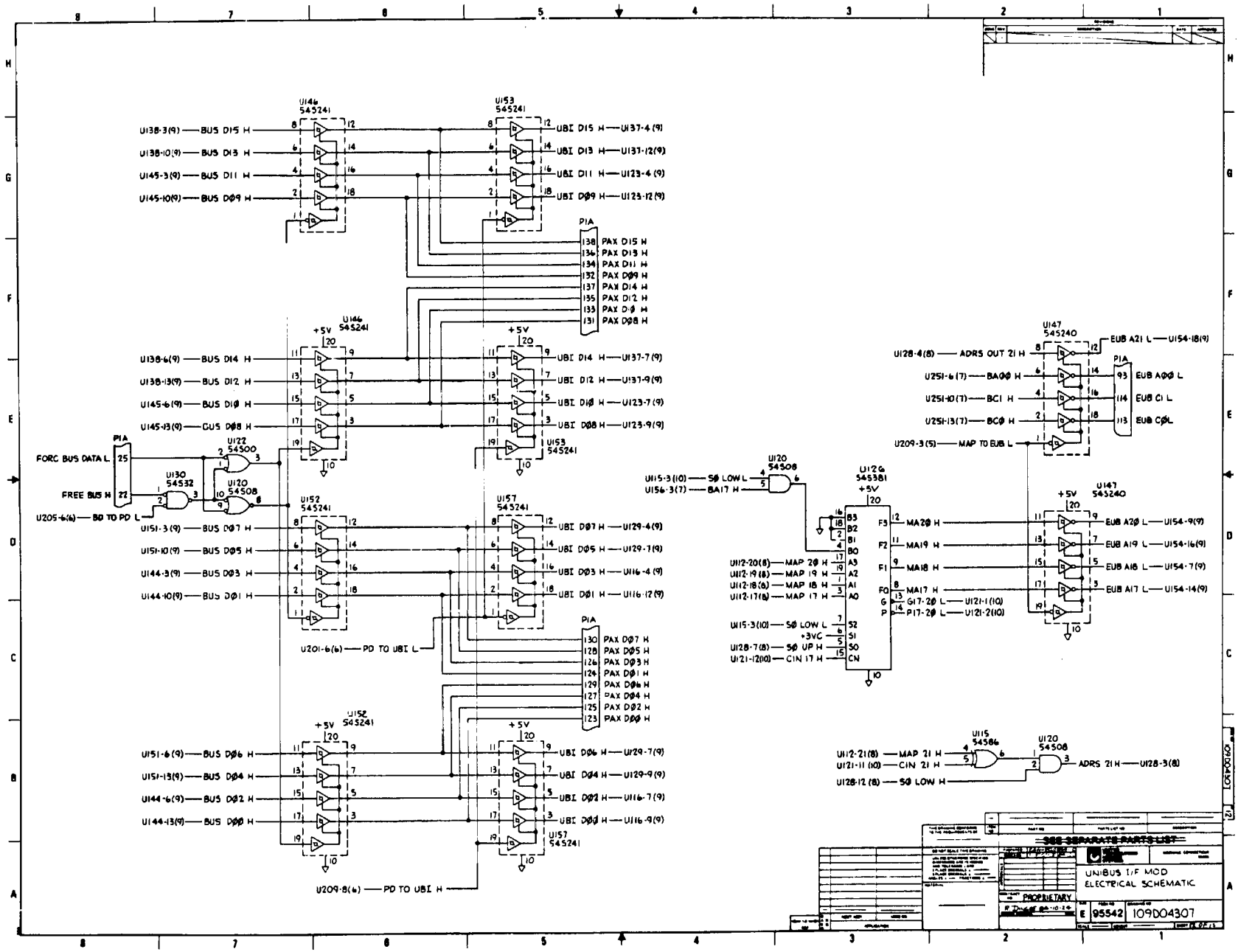
UNIBUS IF SCHEMATIC
(Sheet 9 of 12)



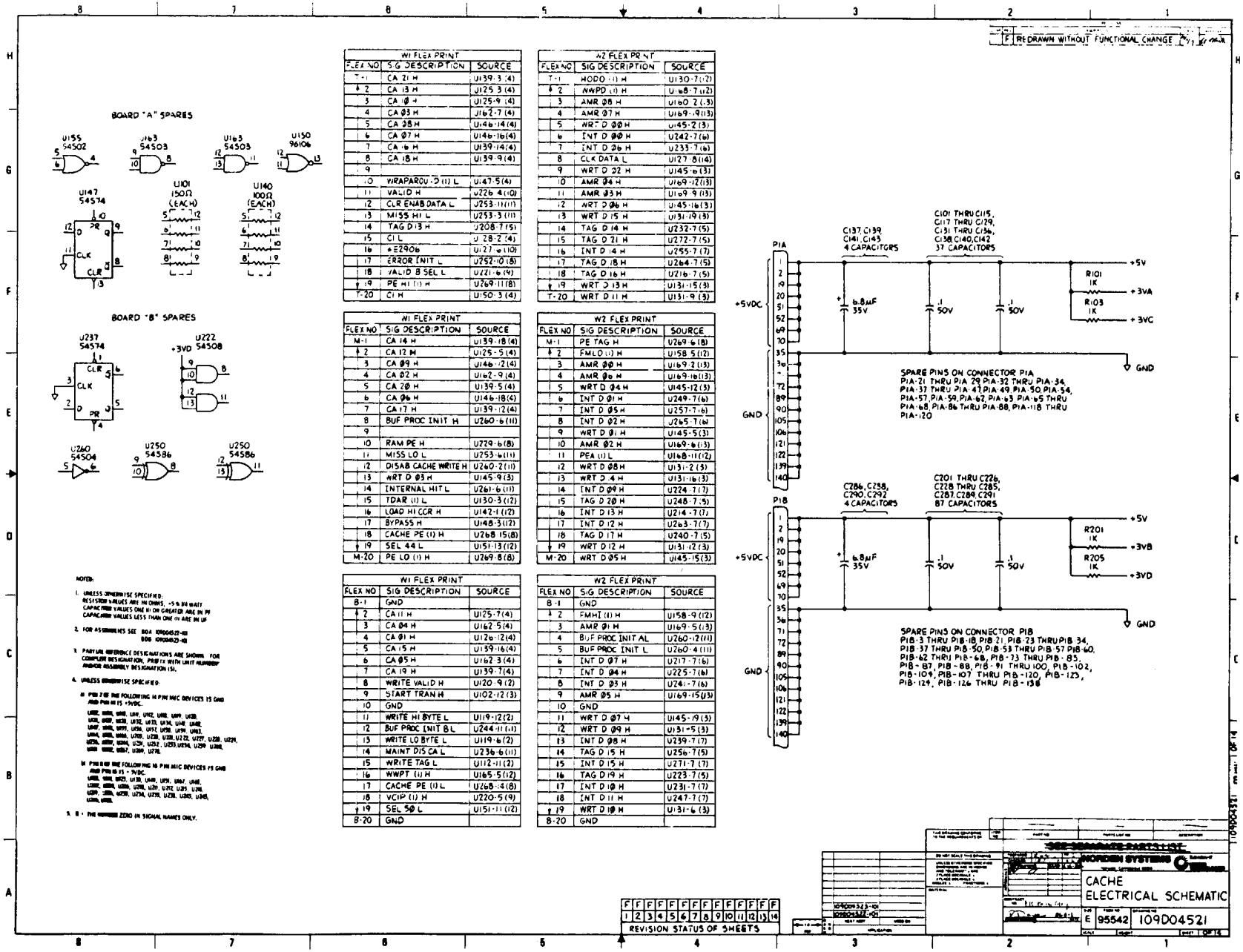
UNIBUS IF SCHEMATIC
(Sheet 10 of 12)



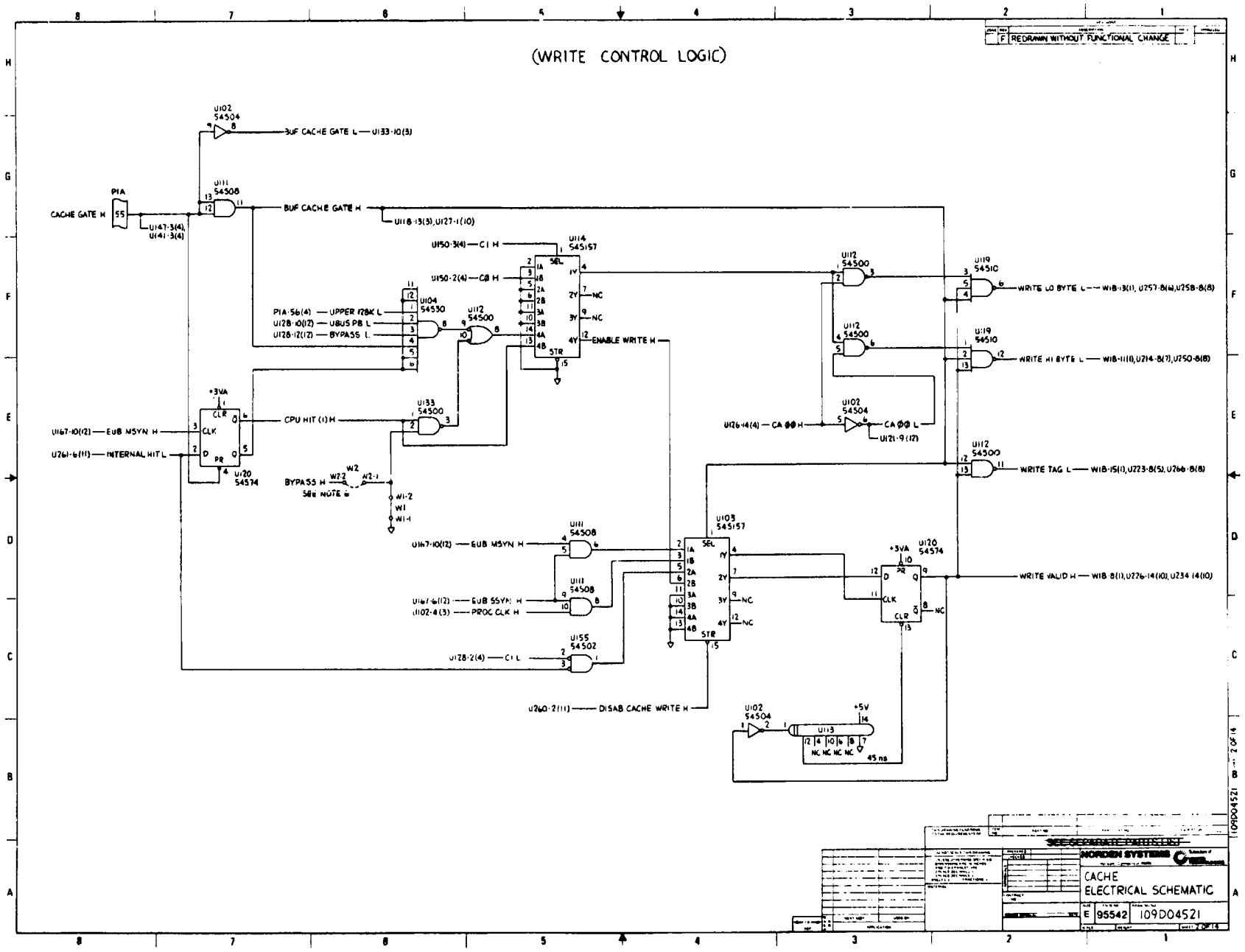
UNIBUS IF SCHEMATIC
(Sheet 11 of 12)



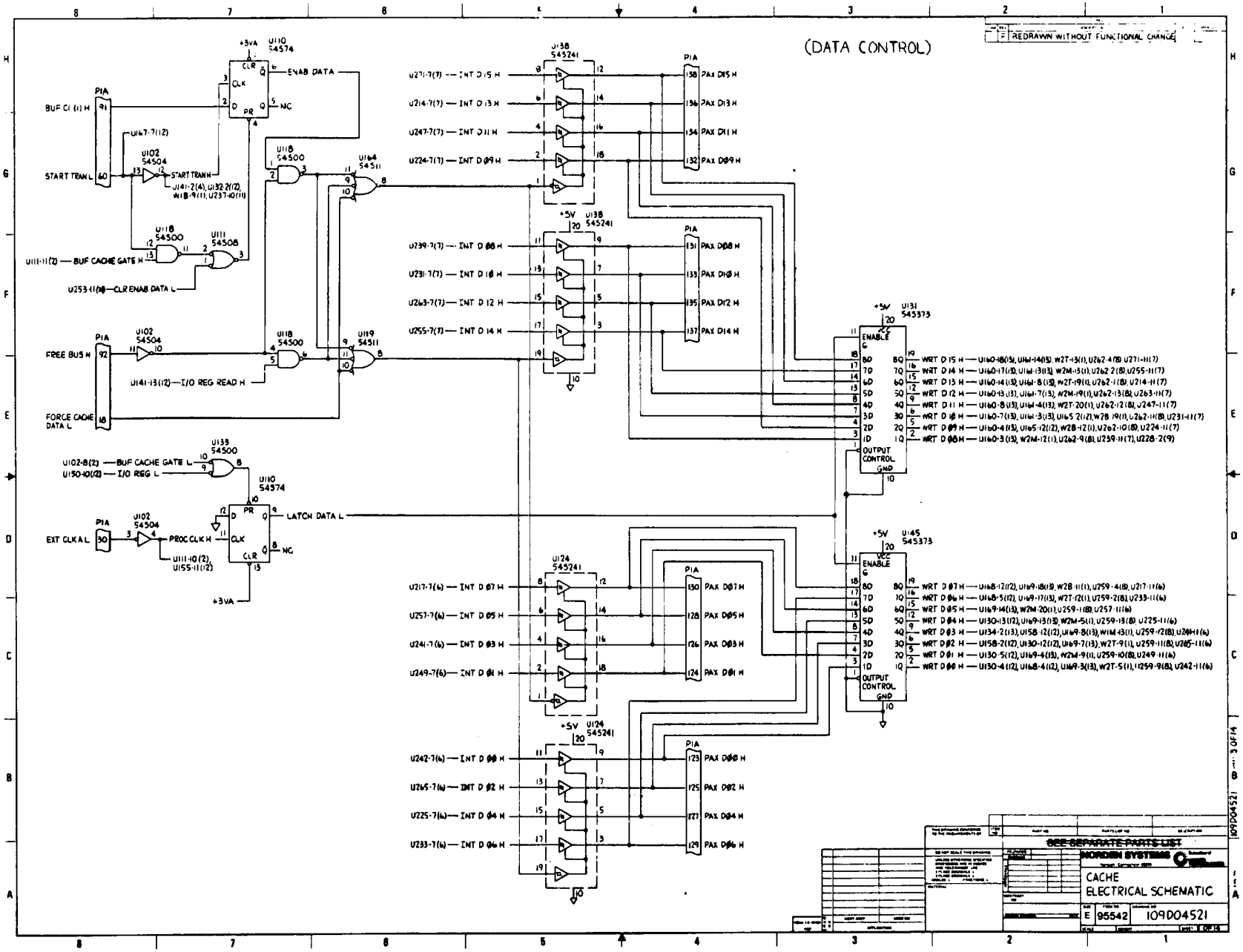
UNIBUS IF SCHEMATIC
(Sheet 12 of 12)



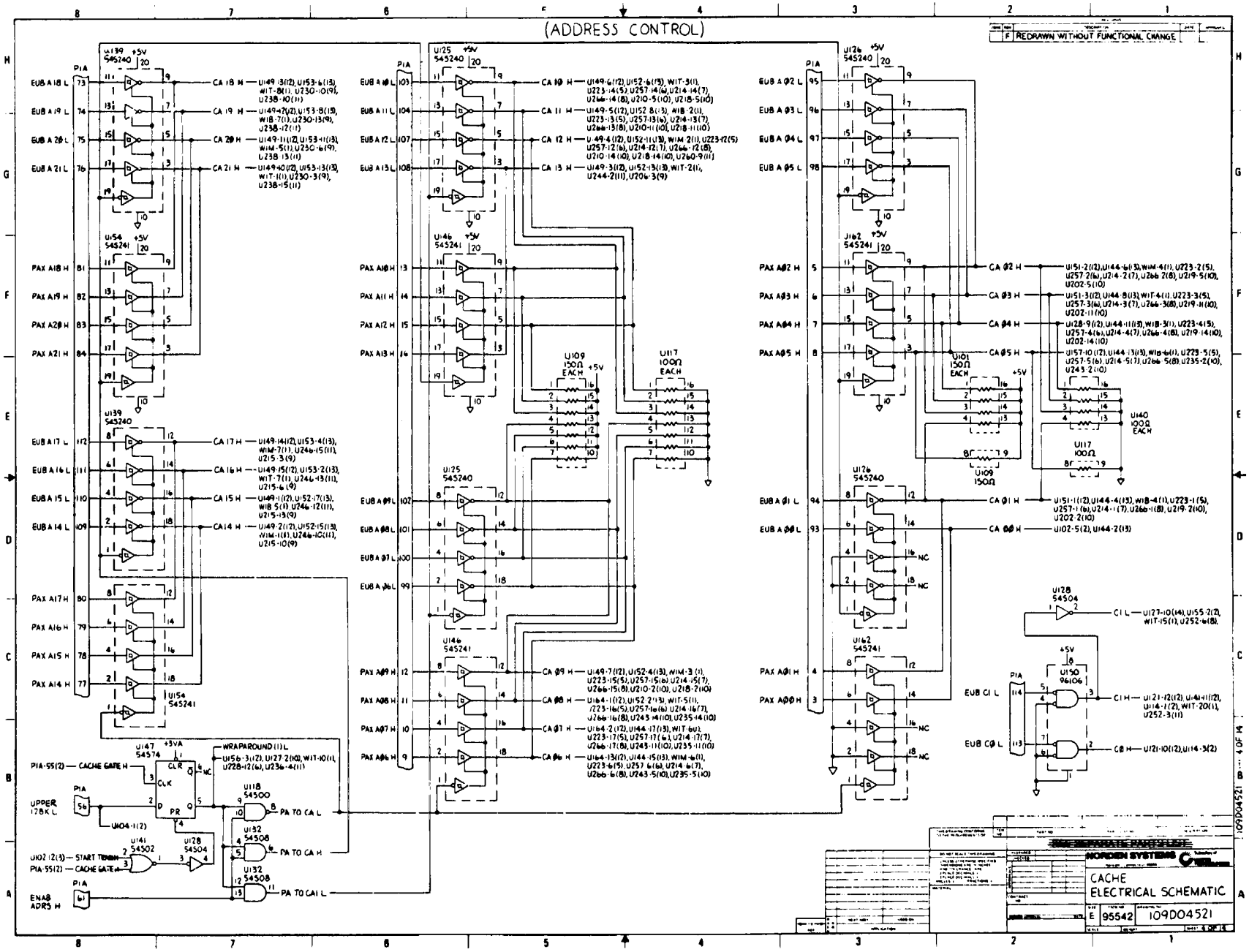
CACHE SCHEMATIC
(Sheet 1 of 14)



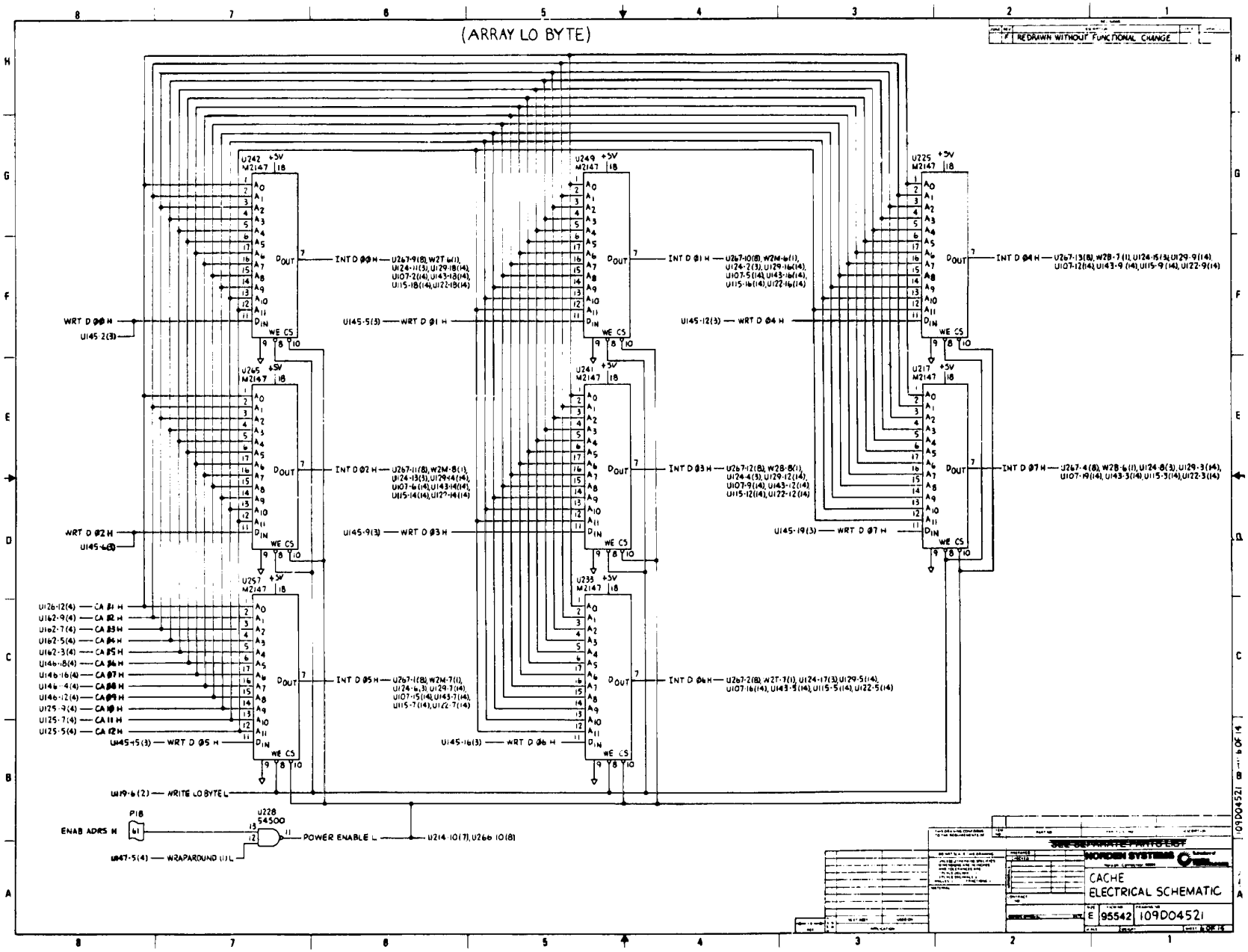
CACHE SCHEMATIC
(Sheet 2 of 14)



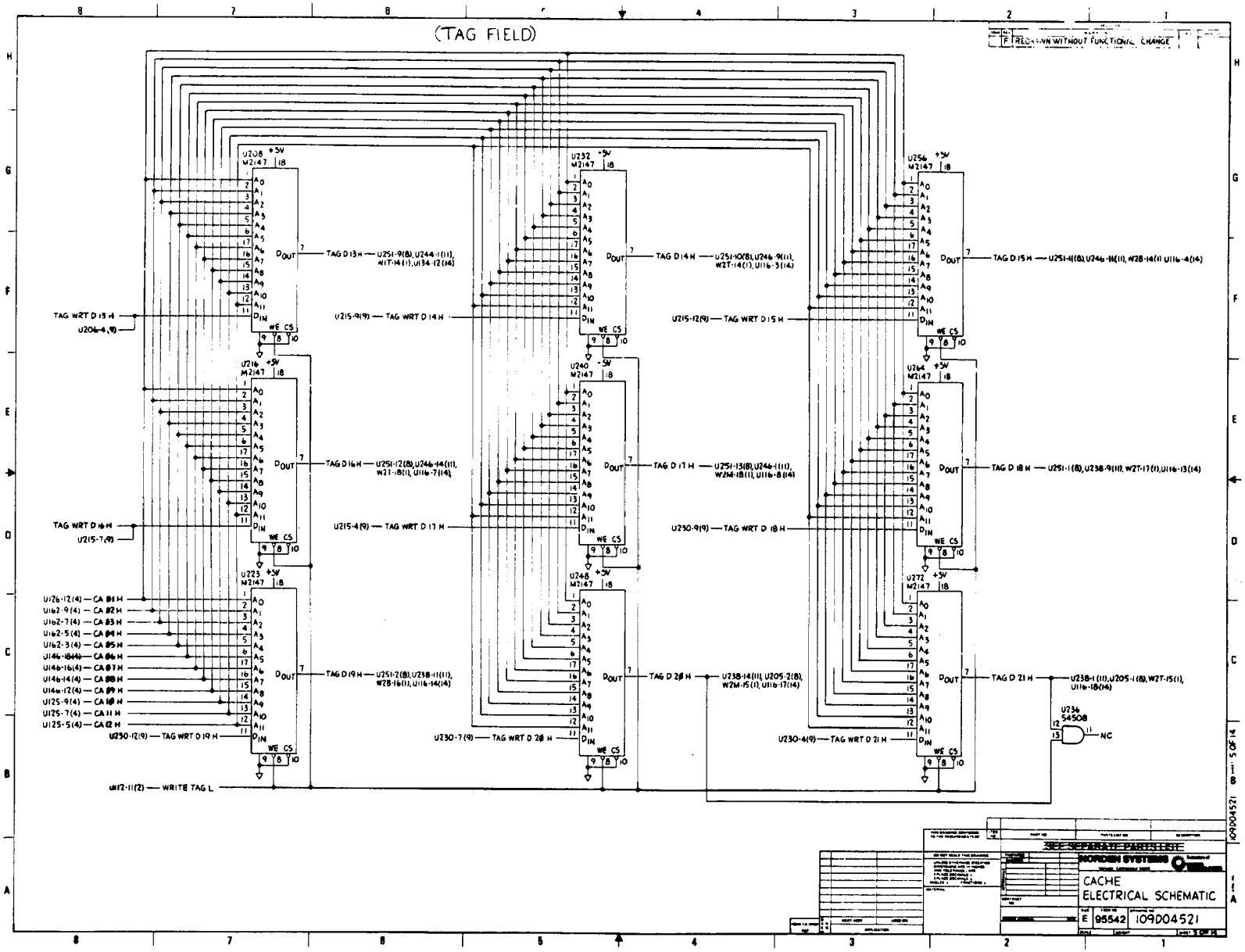
CACHE SCHEMATIC
(Sheet 3 of 14)



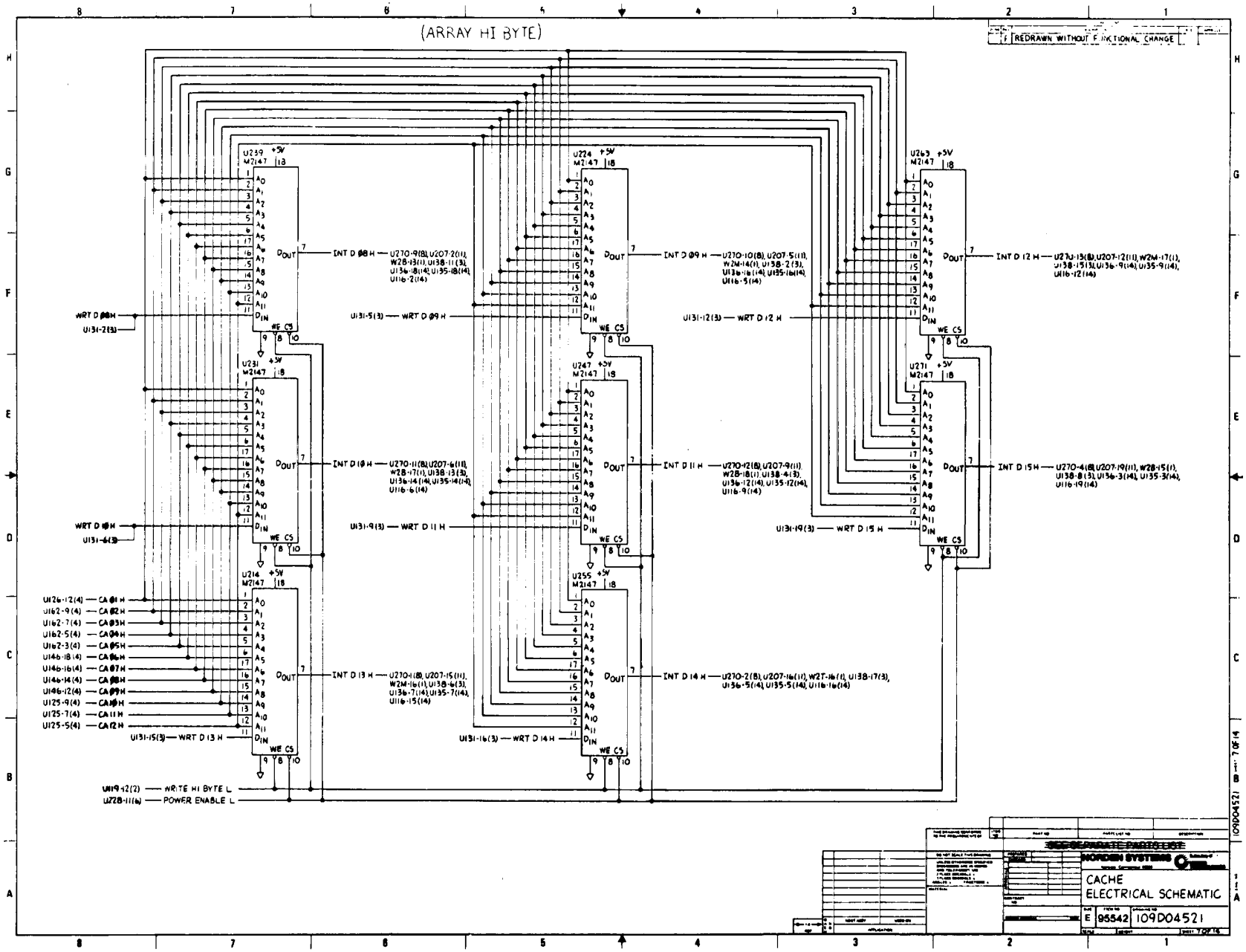
CACHE SCHEMATIC
(Sheet 4 of 14)



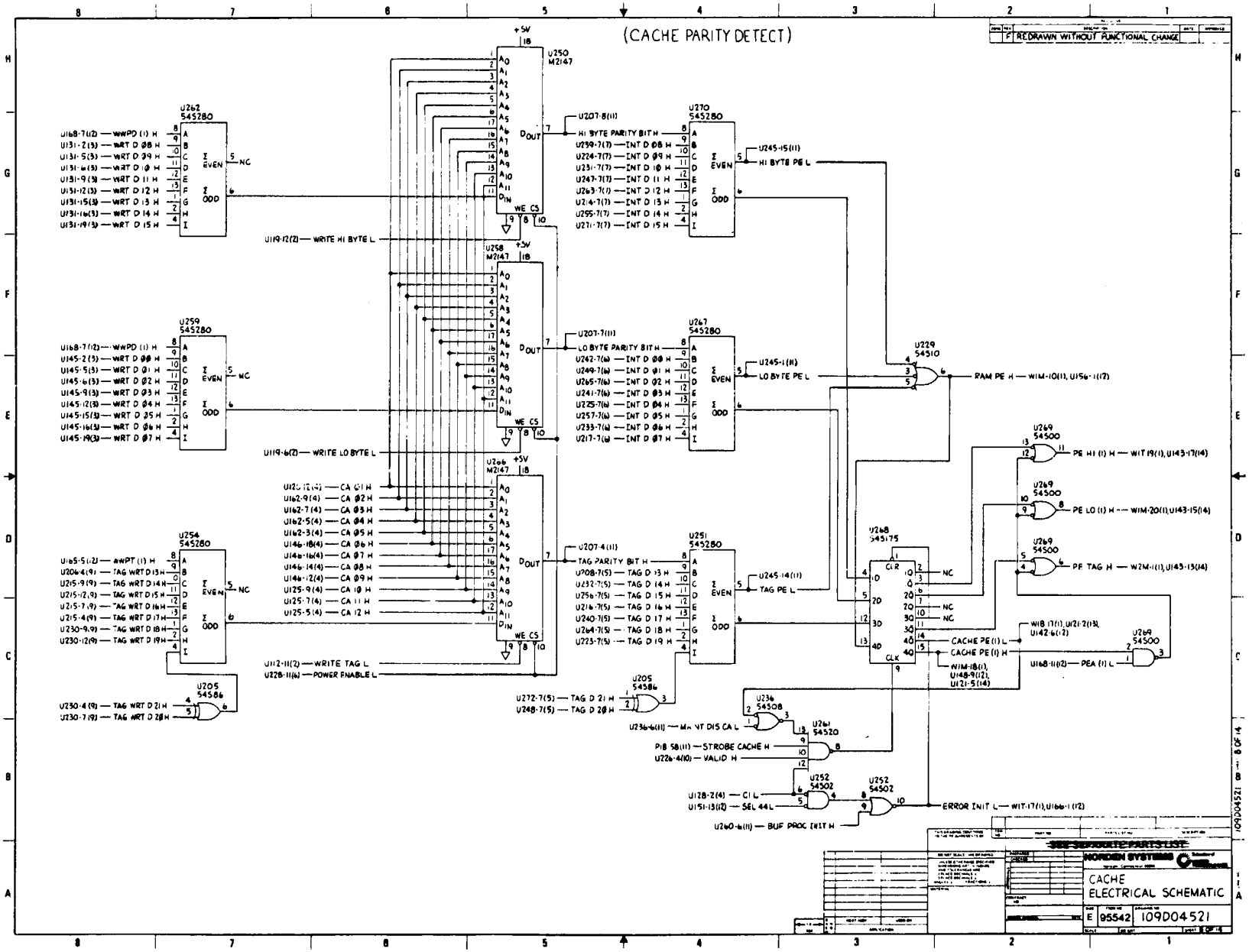
CACHE SCHEMATIC
(Sheet 5 of 14)



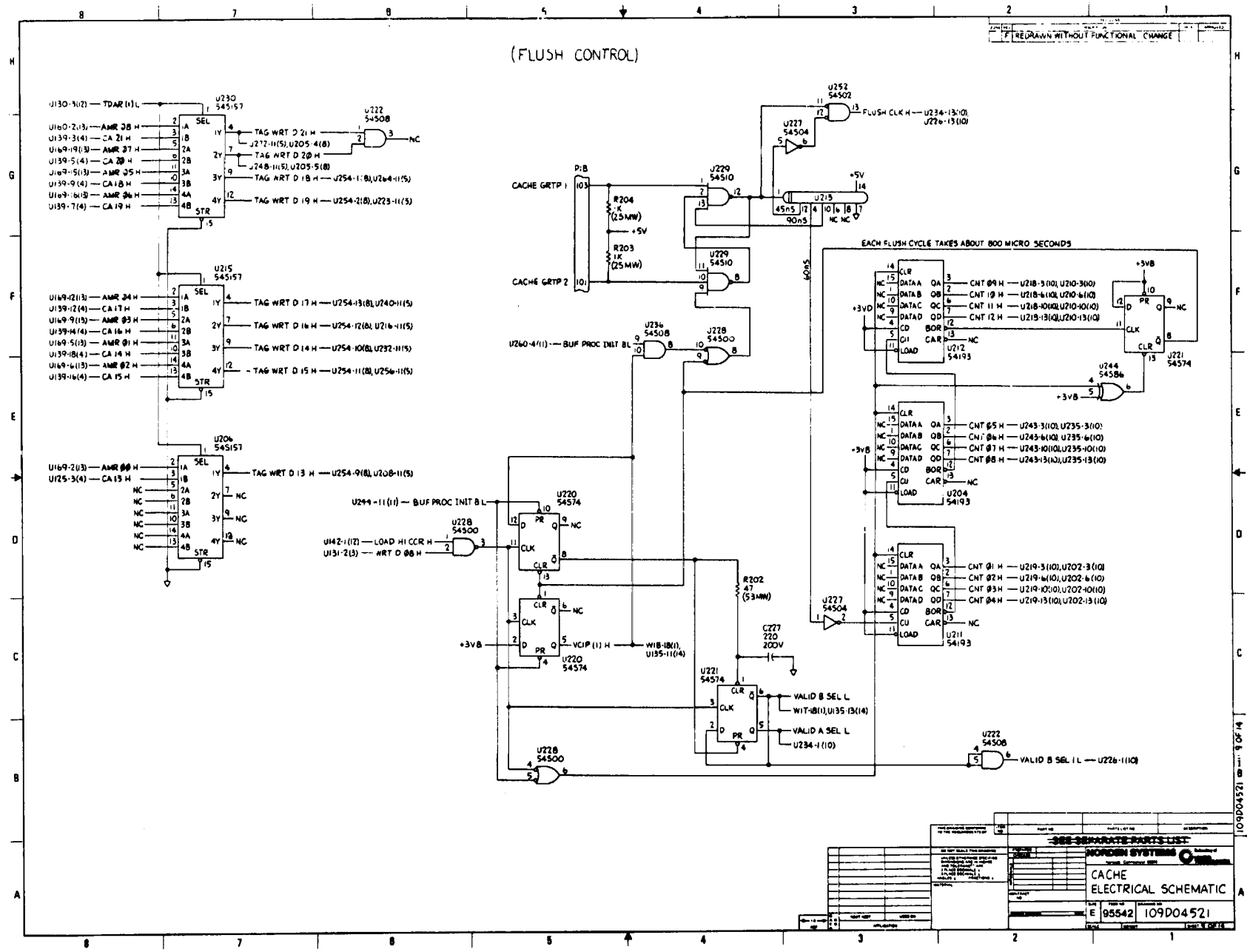
CACHE SCHEMATIC
(Sheet 6 of 14)



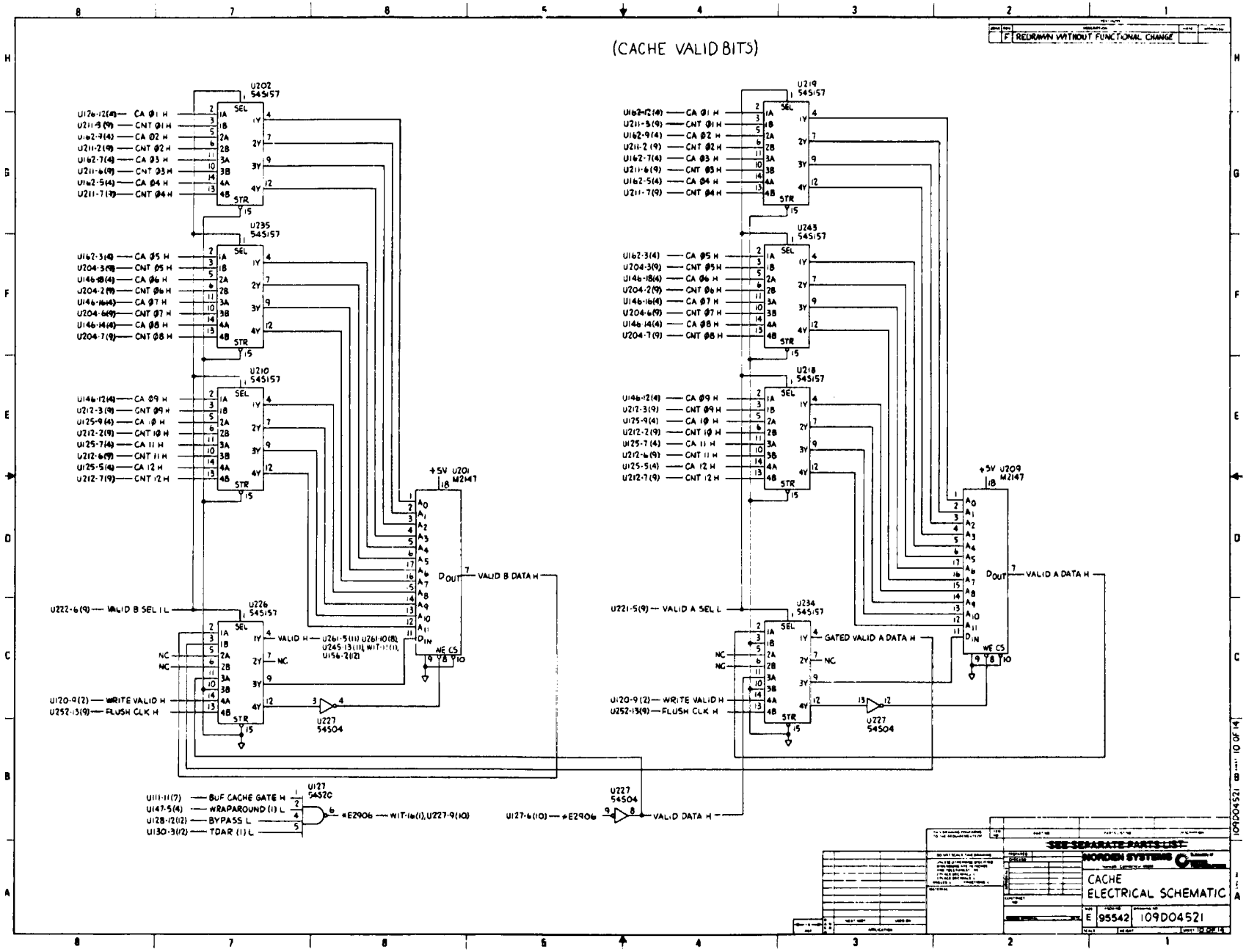
CACHE SCHEMATIC
(Sheet 7 of 14)



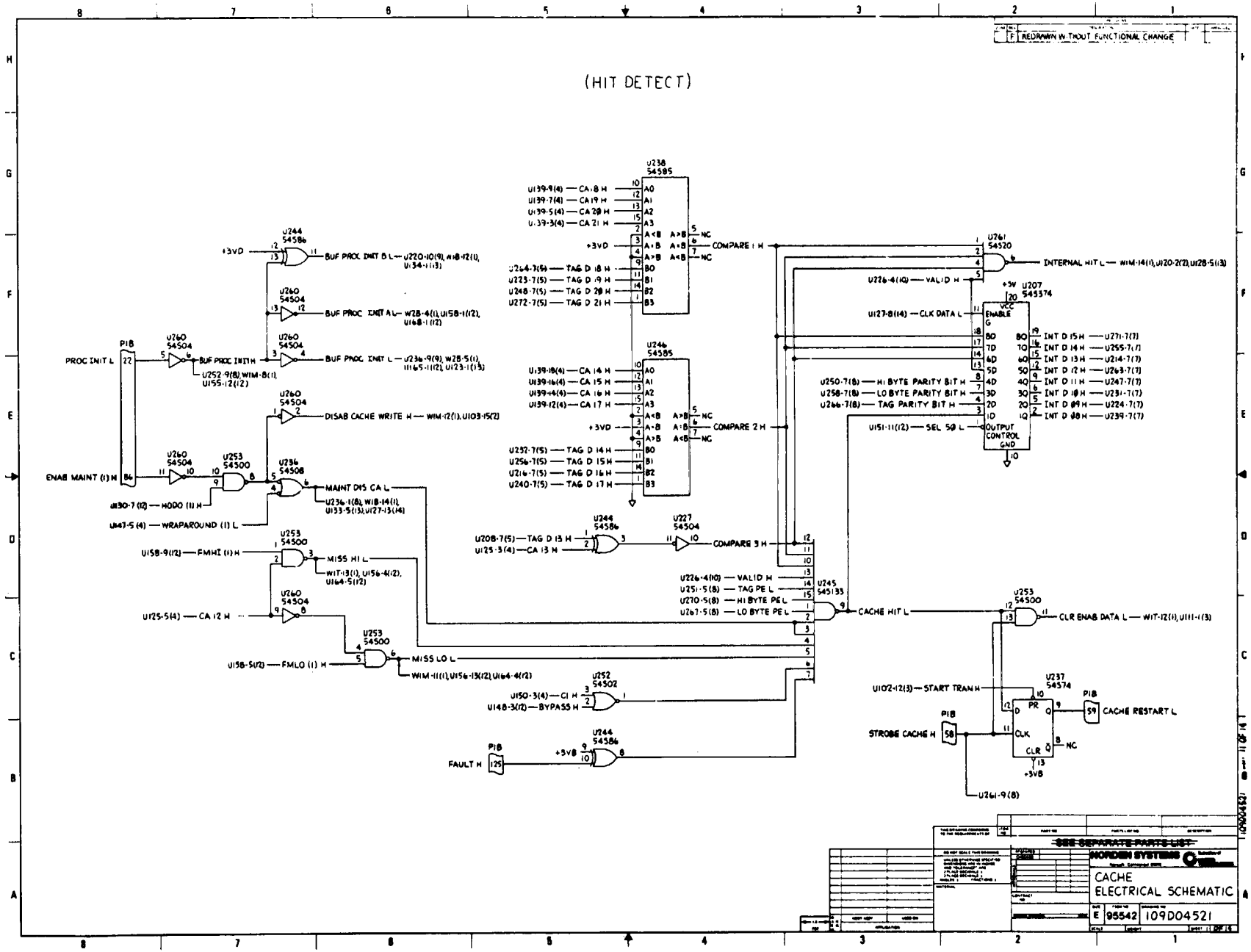
CACHE SCHEMATIC
(Sheet 8 of 14)



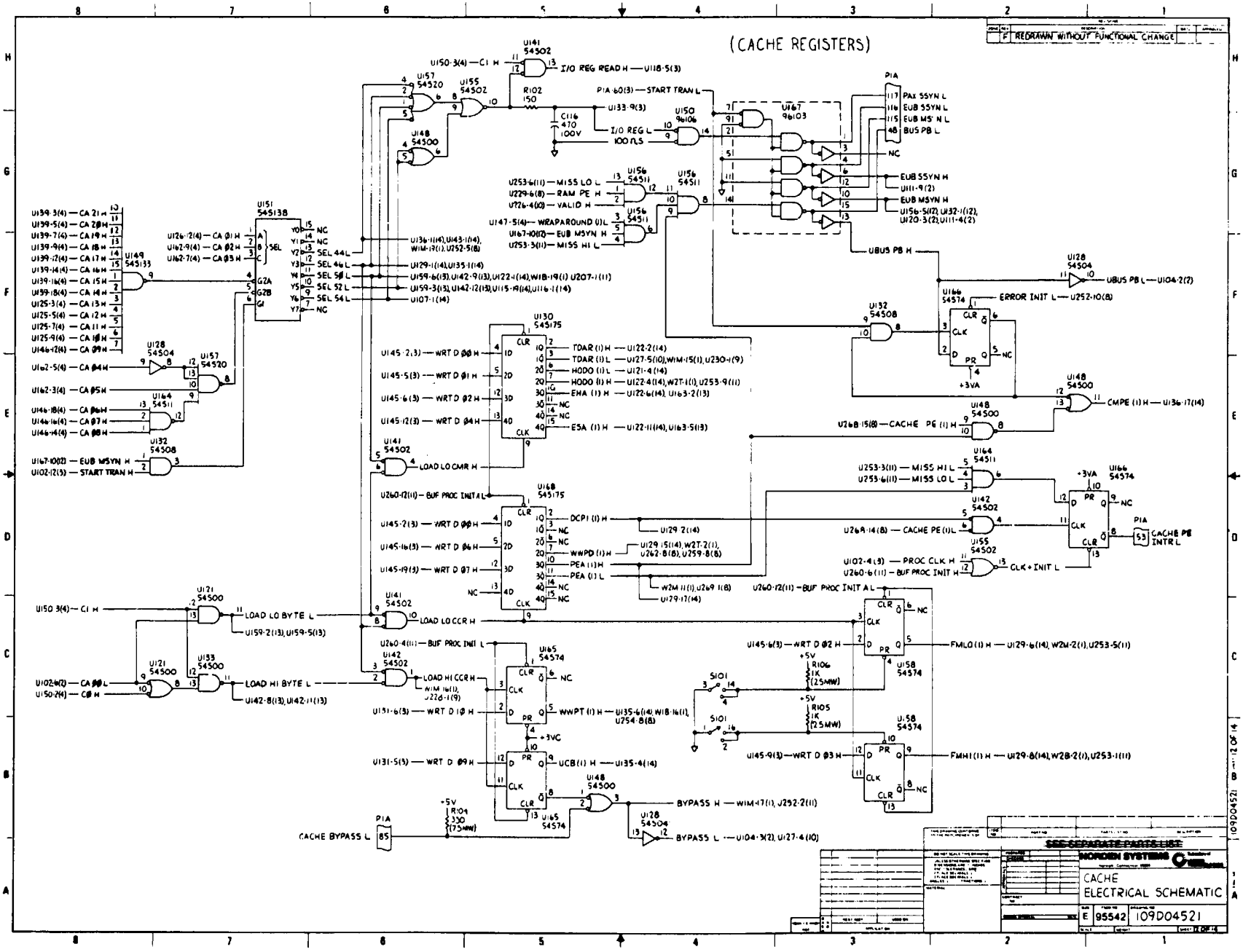
CACHE SCHEMATIC
(Sheet 9 of 14)



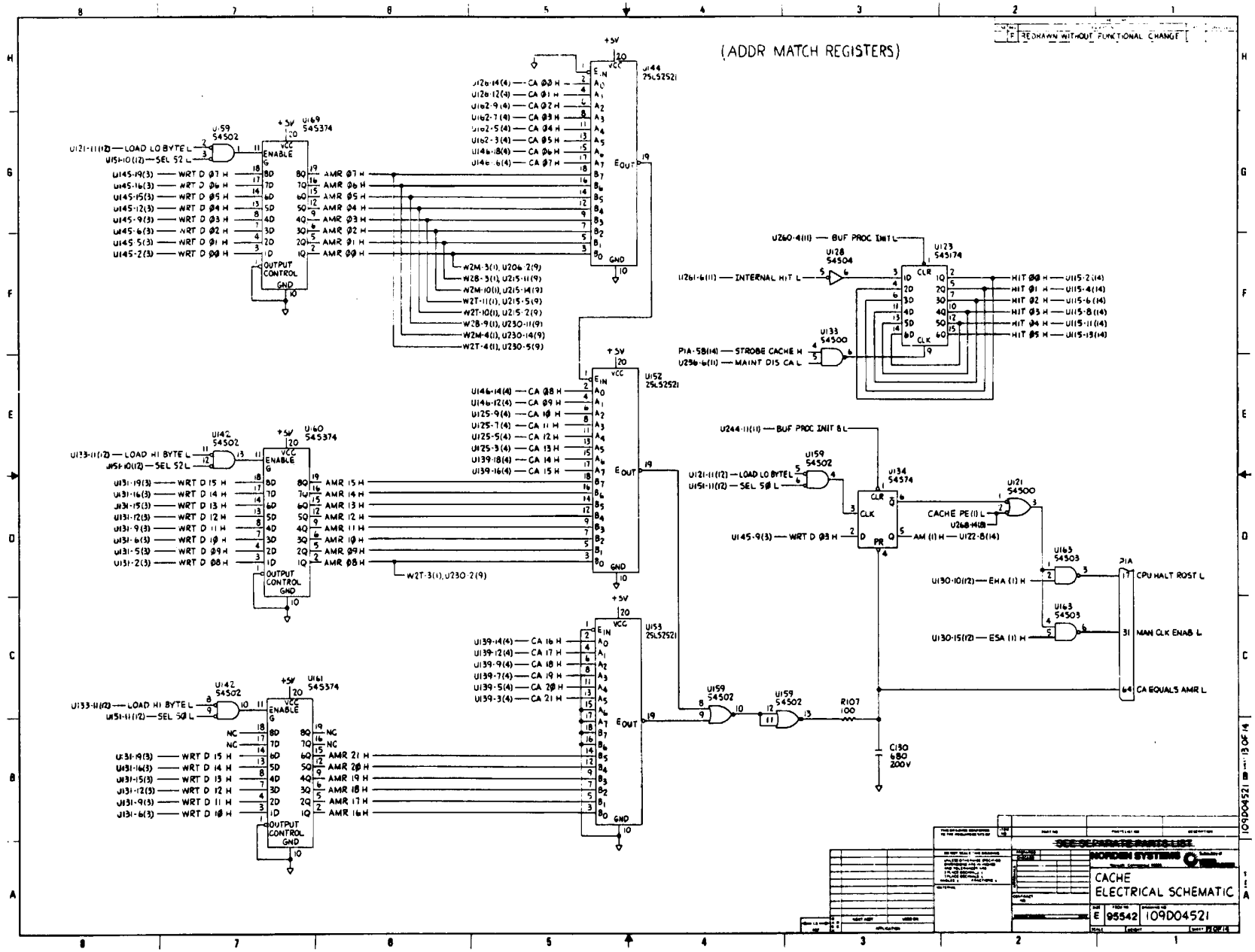
CACHE SCHEMATIC
(Sheet 10 of 14)



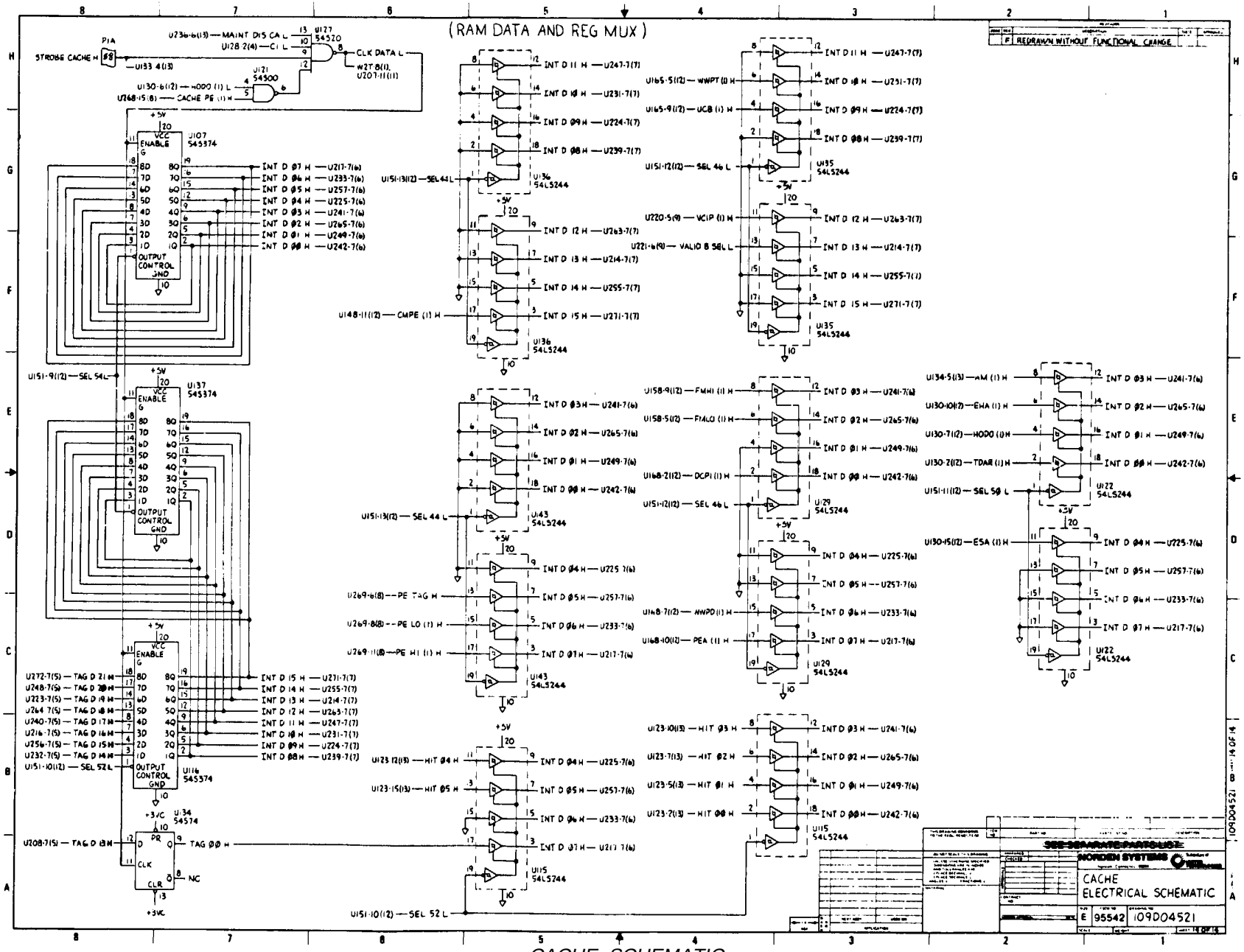
CACHE SCHEMATIC
(Sheet 11 of 14)



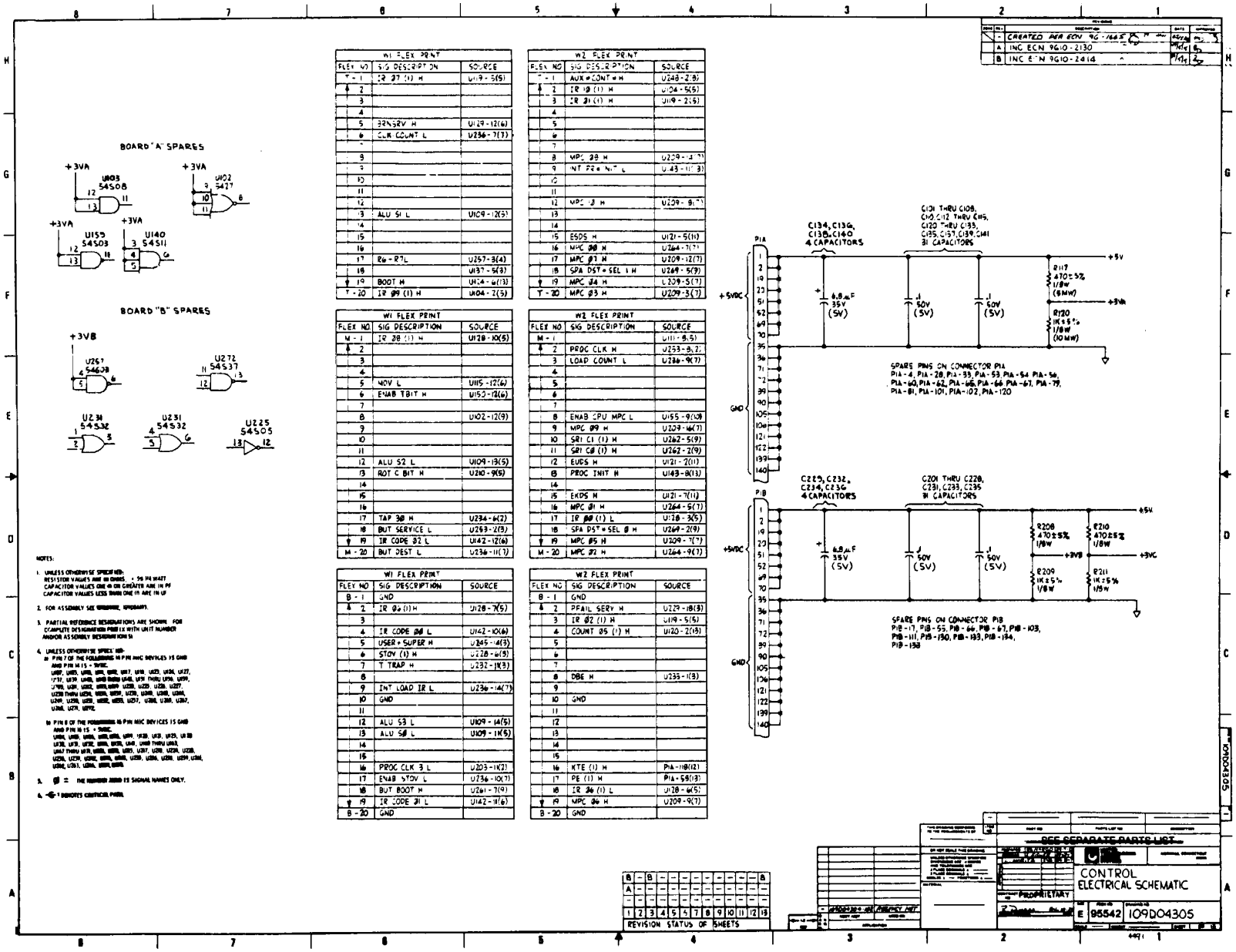
CACHE SCHEMATIC
(Sheet 12 of 14)



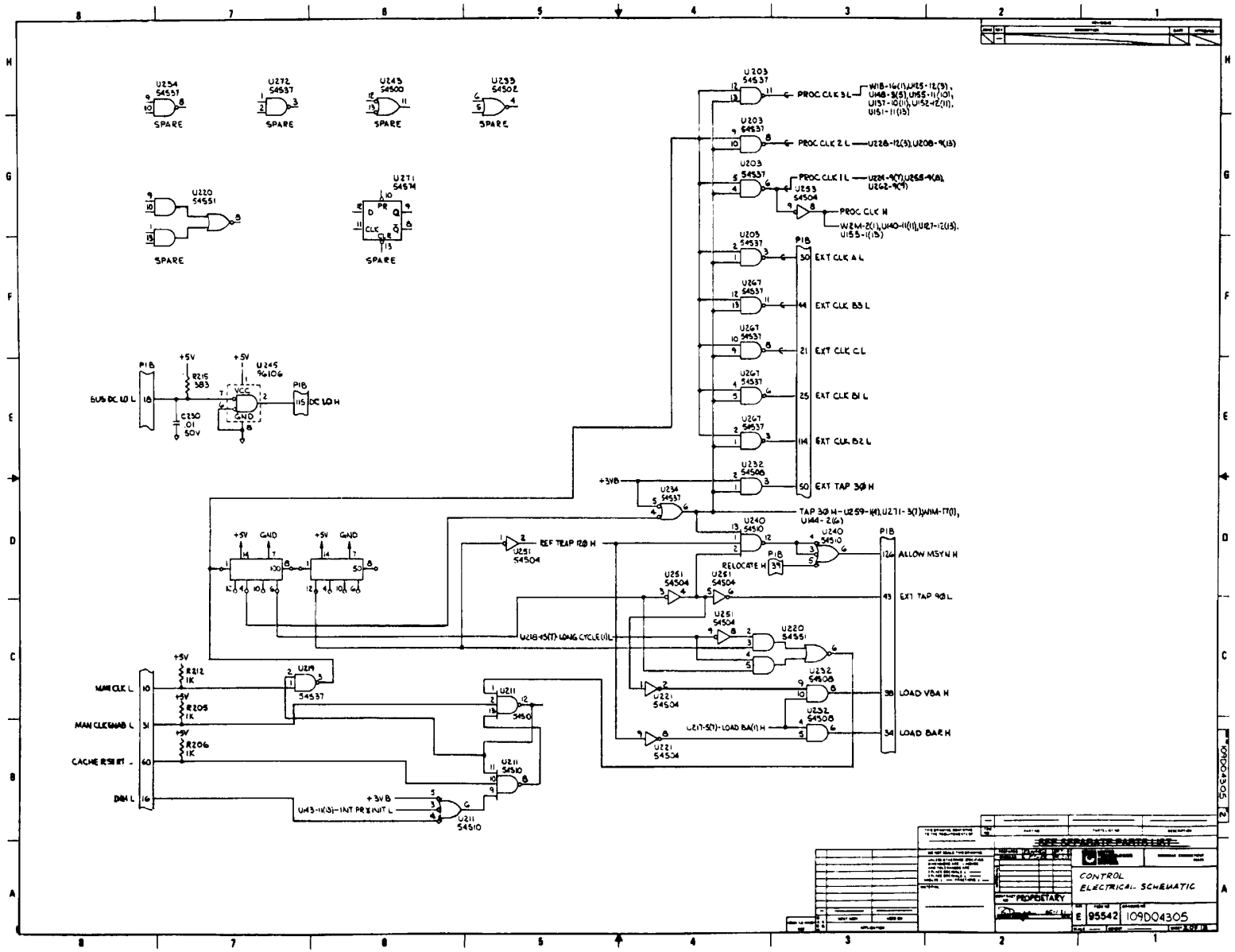
CACHE SCHEMATIC
(Sheet 13 of 14)



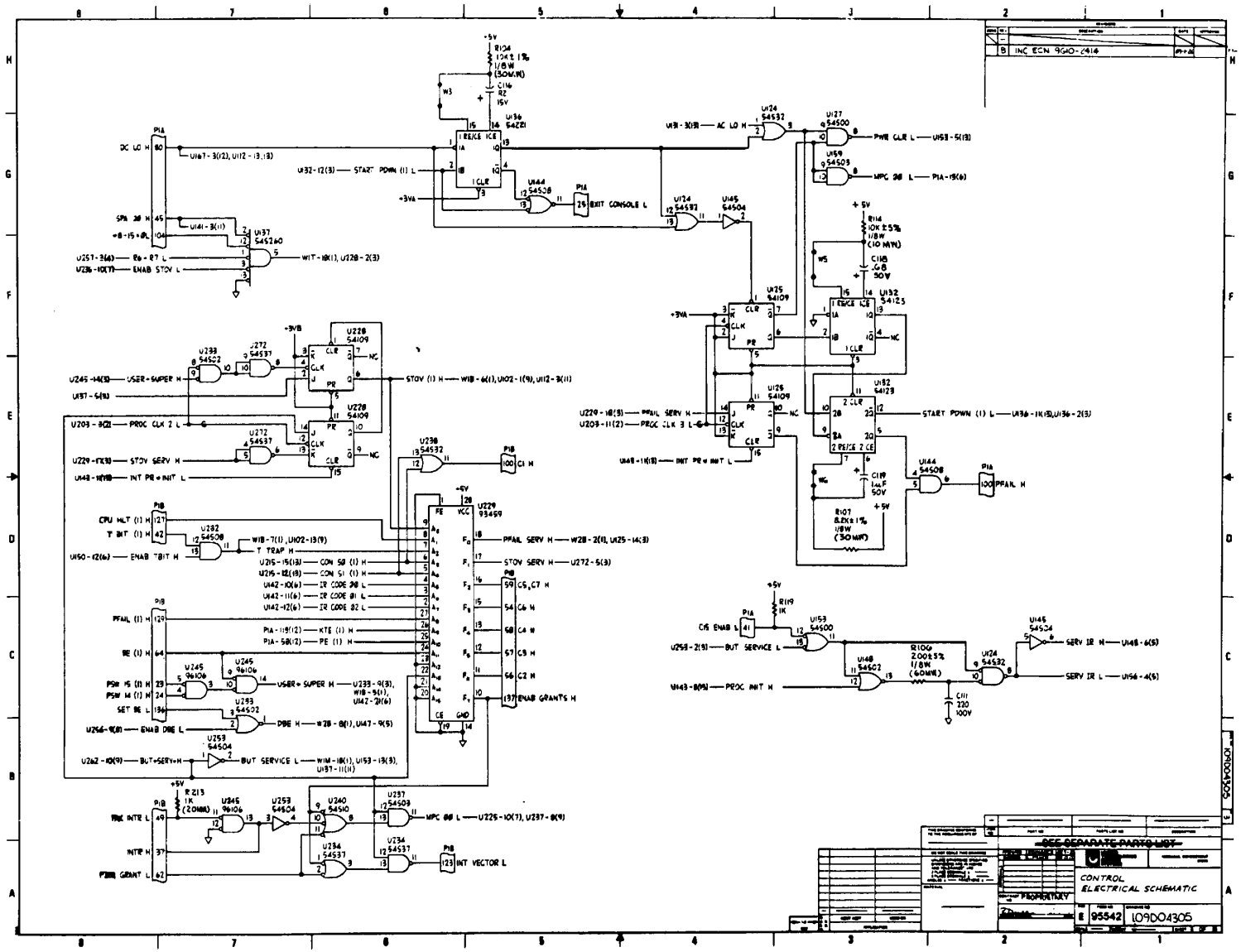
CACHE SCHEMATIC
(Sheet 14 of 14)



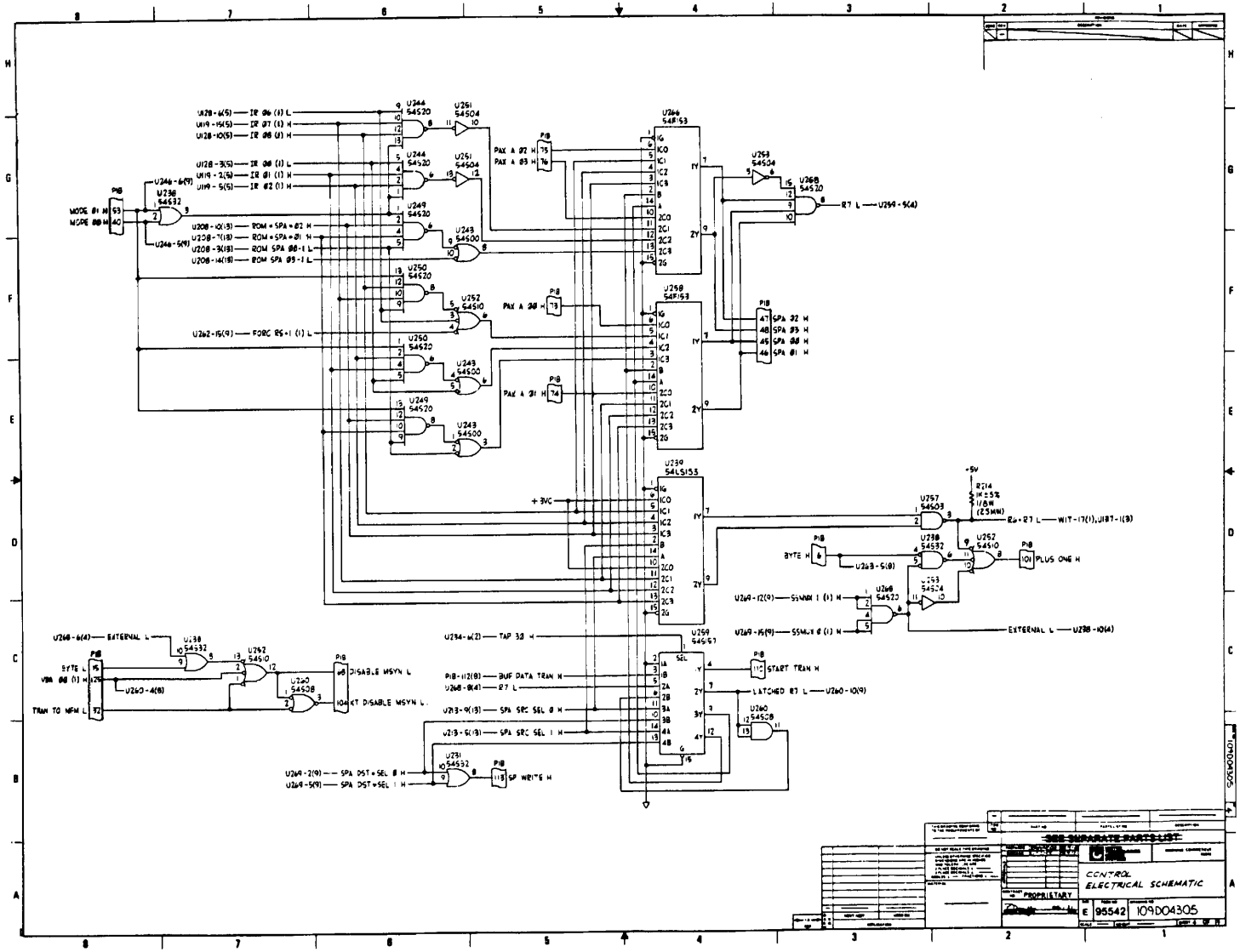
CONTROL SCHEMATIC
(Sheet 1 of 13)



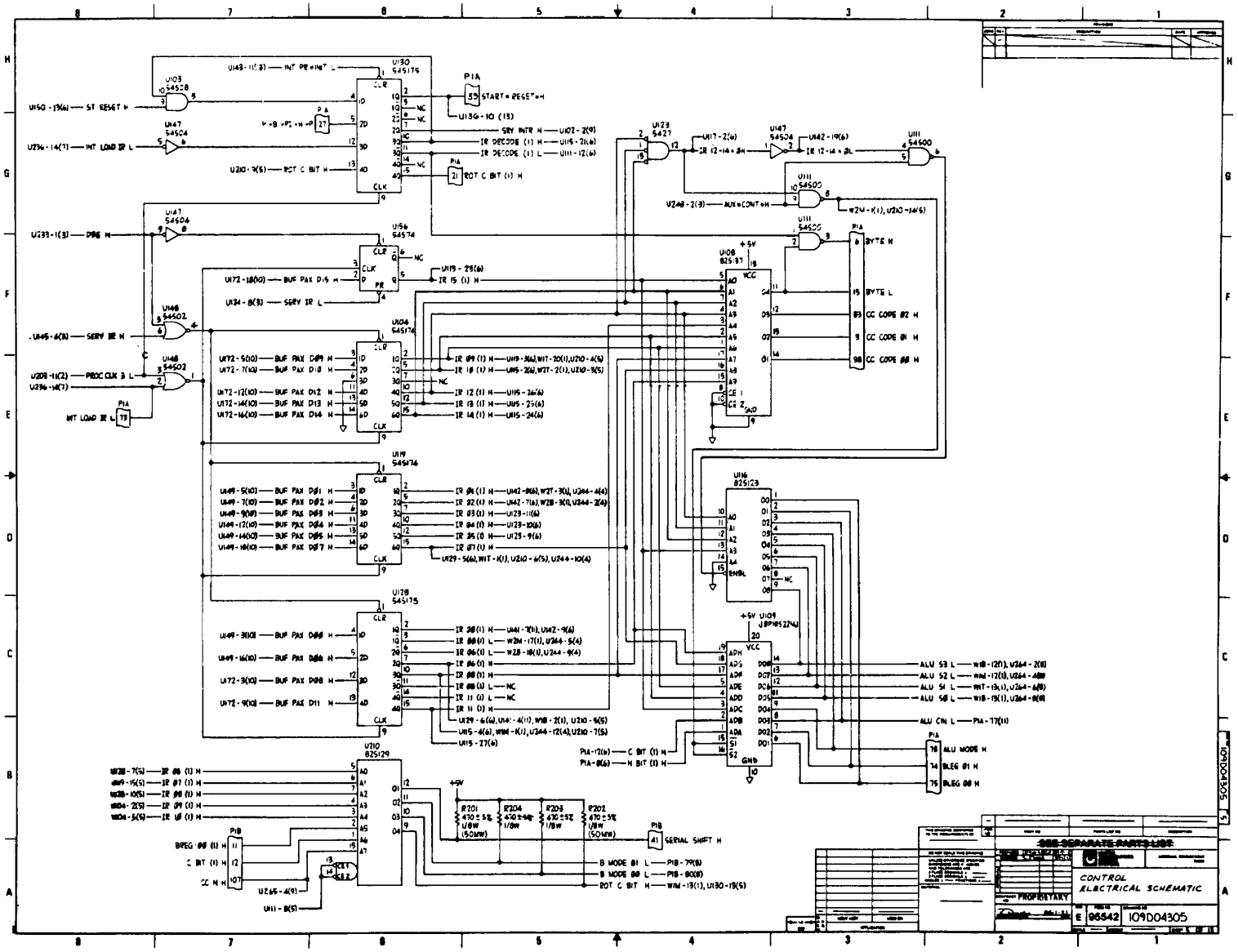
CONTROL SCHEMATIC
(Sheet 2 of 13)



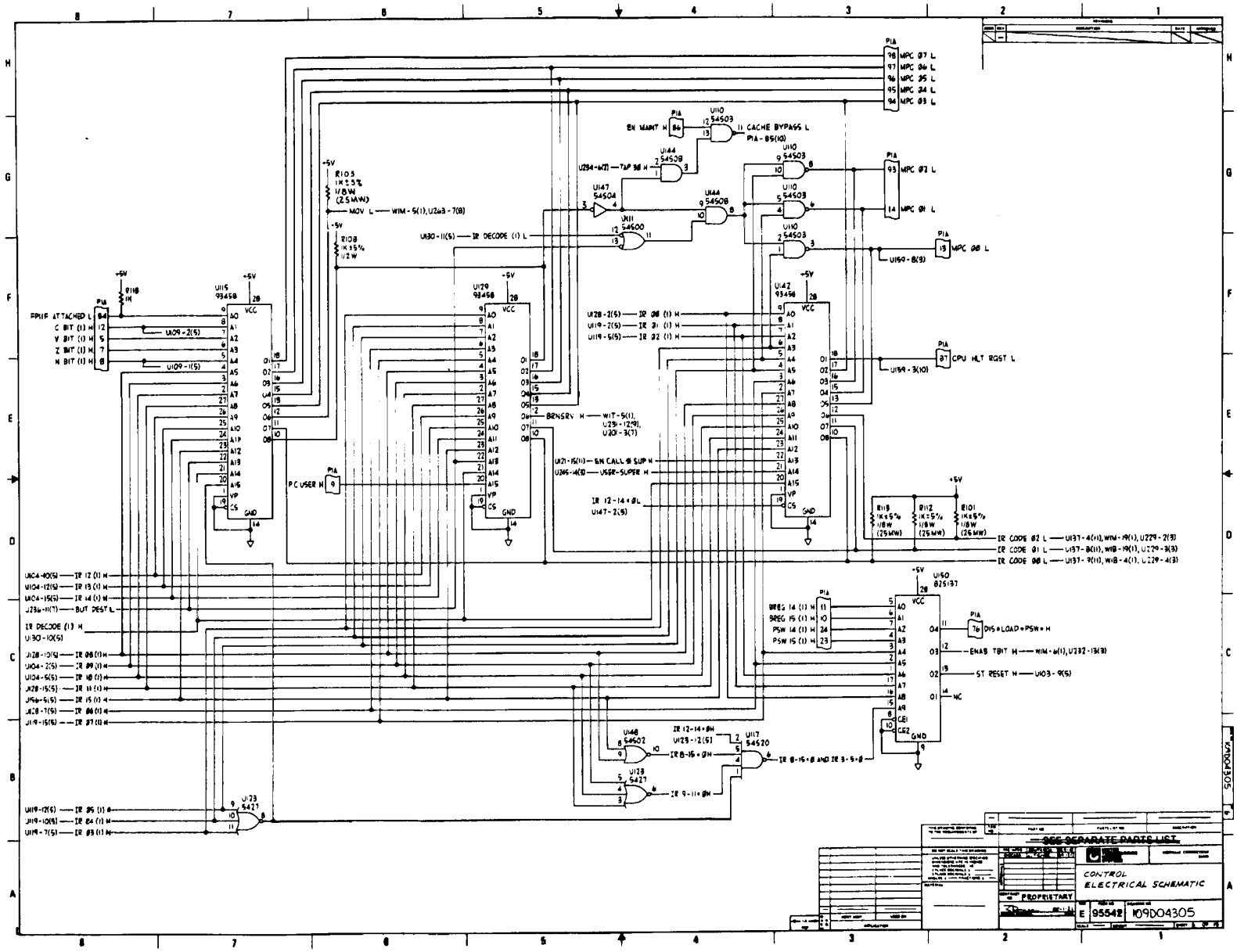
CONTROL SCHEMATIC
(Sheet 3 of 13)



CONTROL SCHEMATIC
(Sheet 4 of 13)

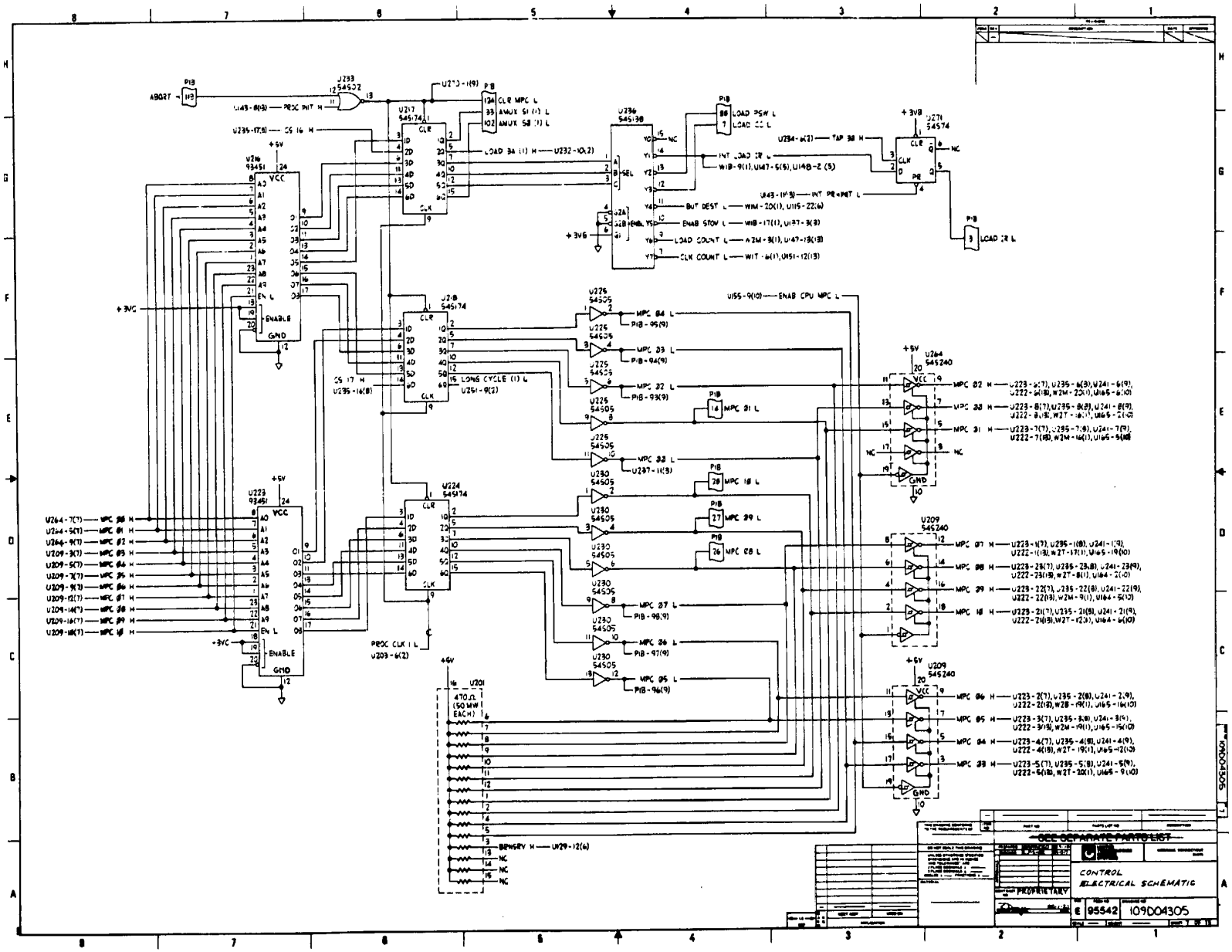


CONTROL SCHEMATIC
(Sheet 5 of 13)



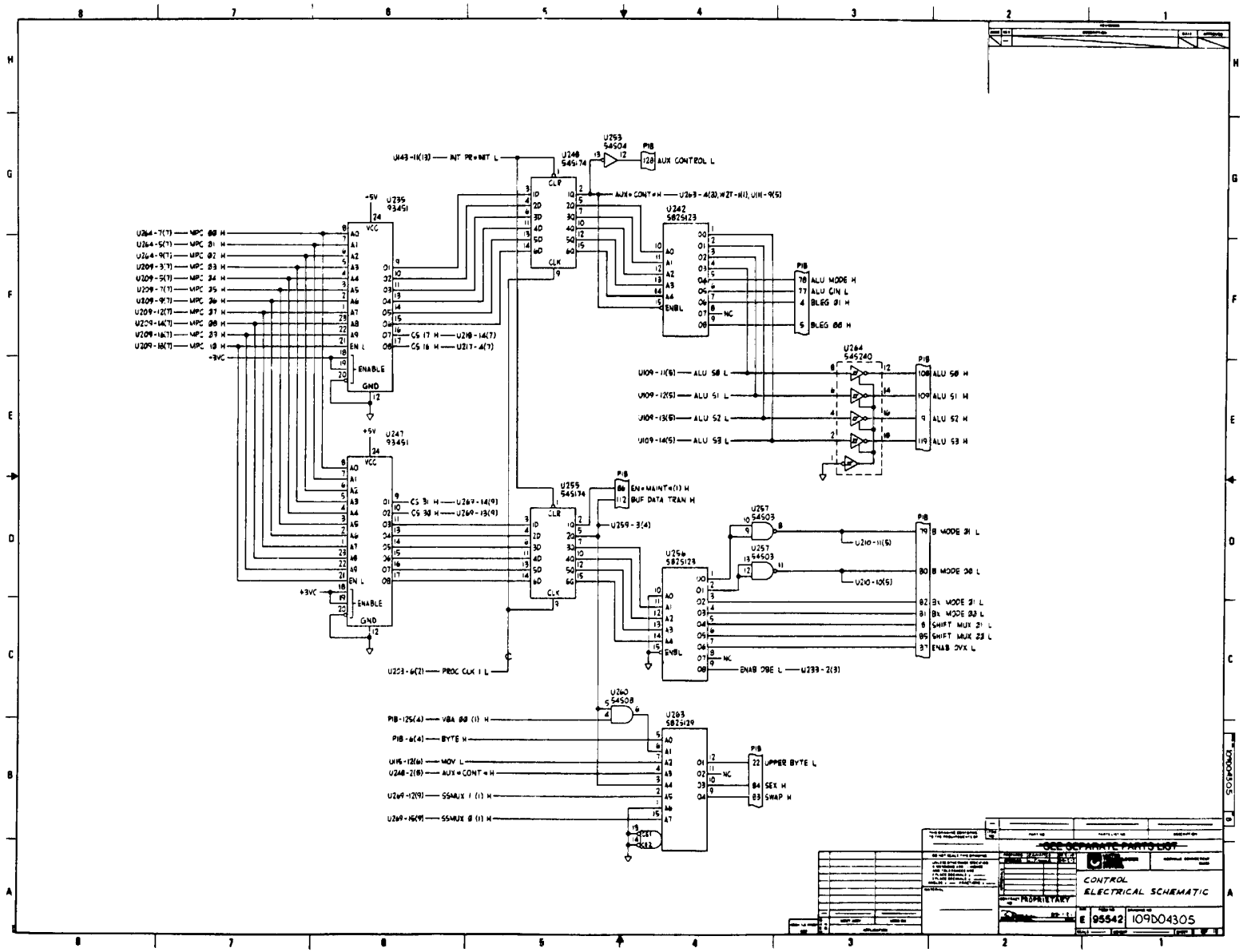
CONTROL SCHEMATIC

(Sheet 6 of 13)

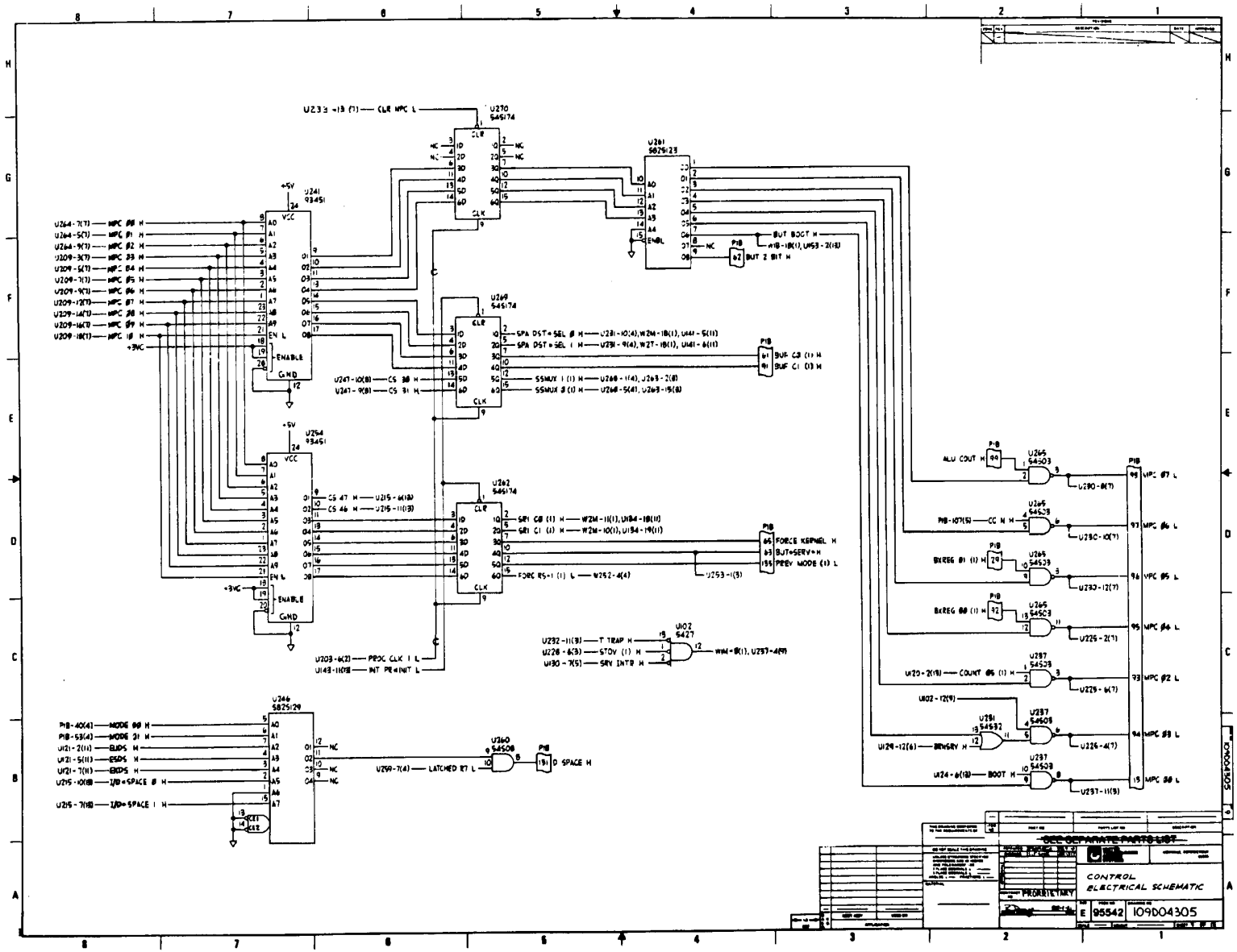


CONTROL SCHEMATIC

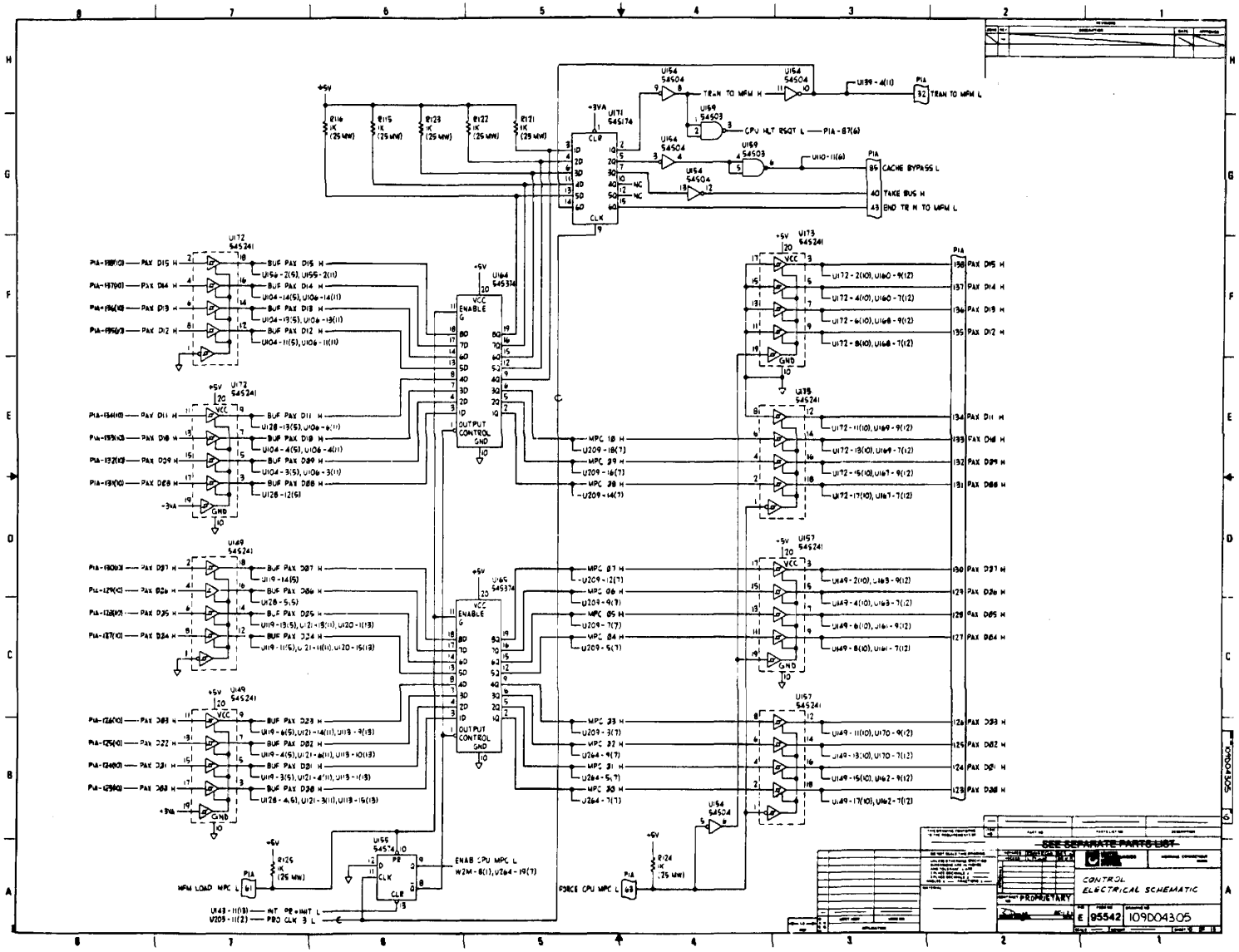
(Sheet 7 of 13)



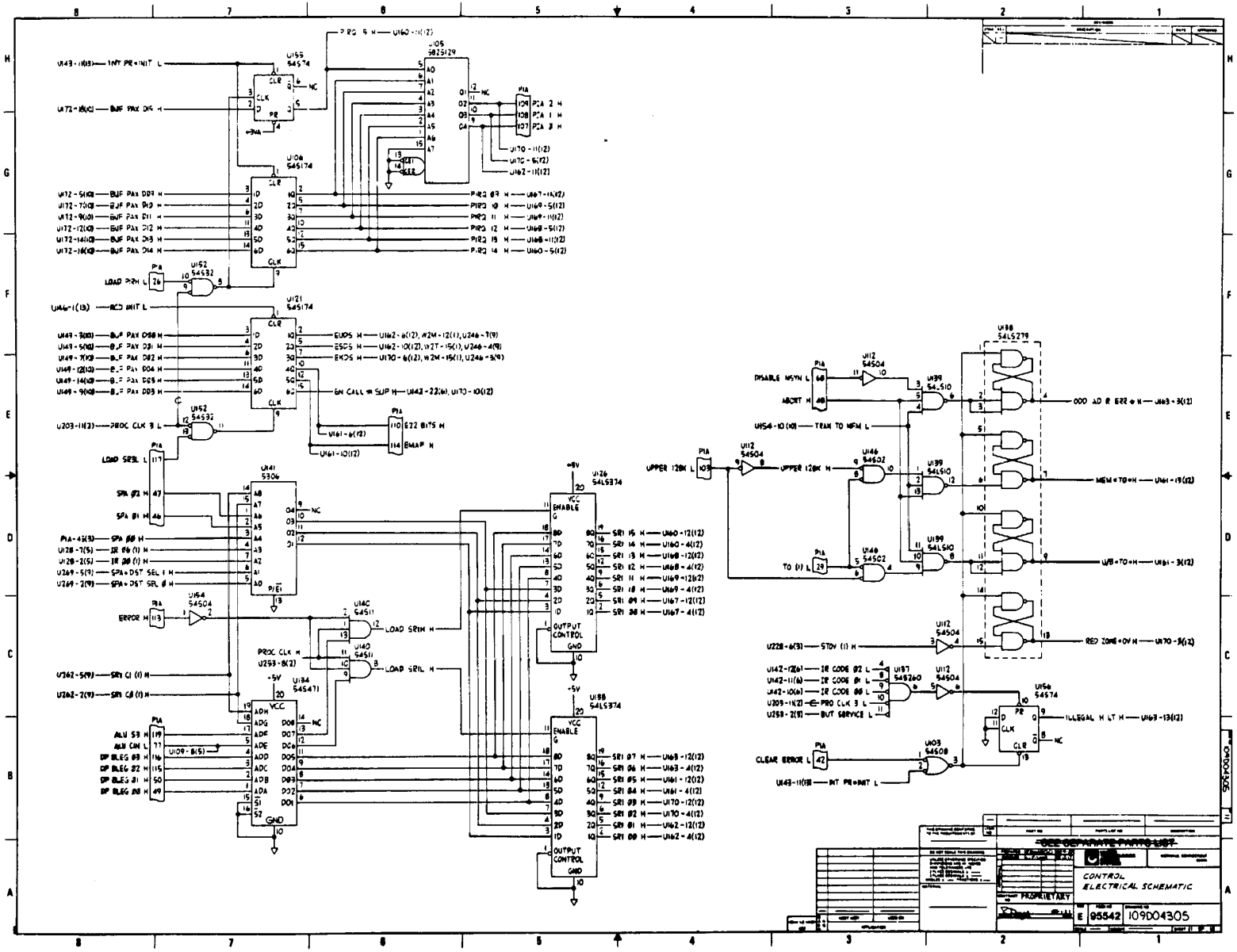
CONTROL SCHEMATIC
(Sheet 8 of 13)



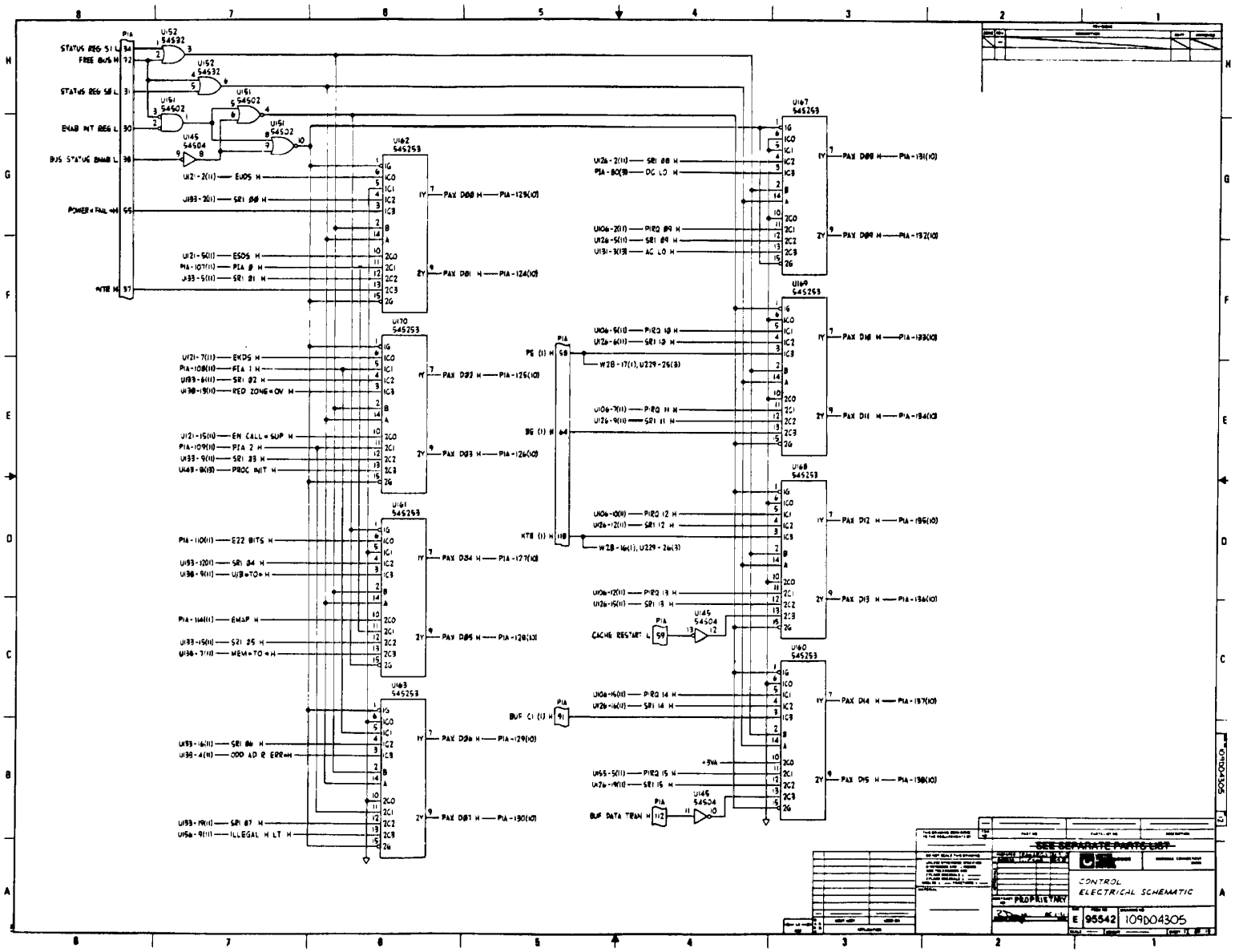
CONTROL SCHEMATIC
(Sheet 9 of 13)



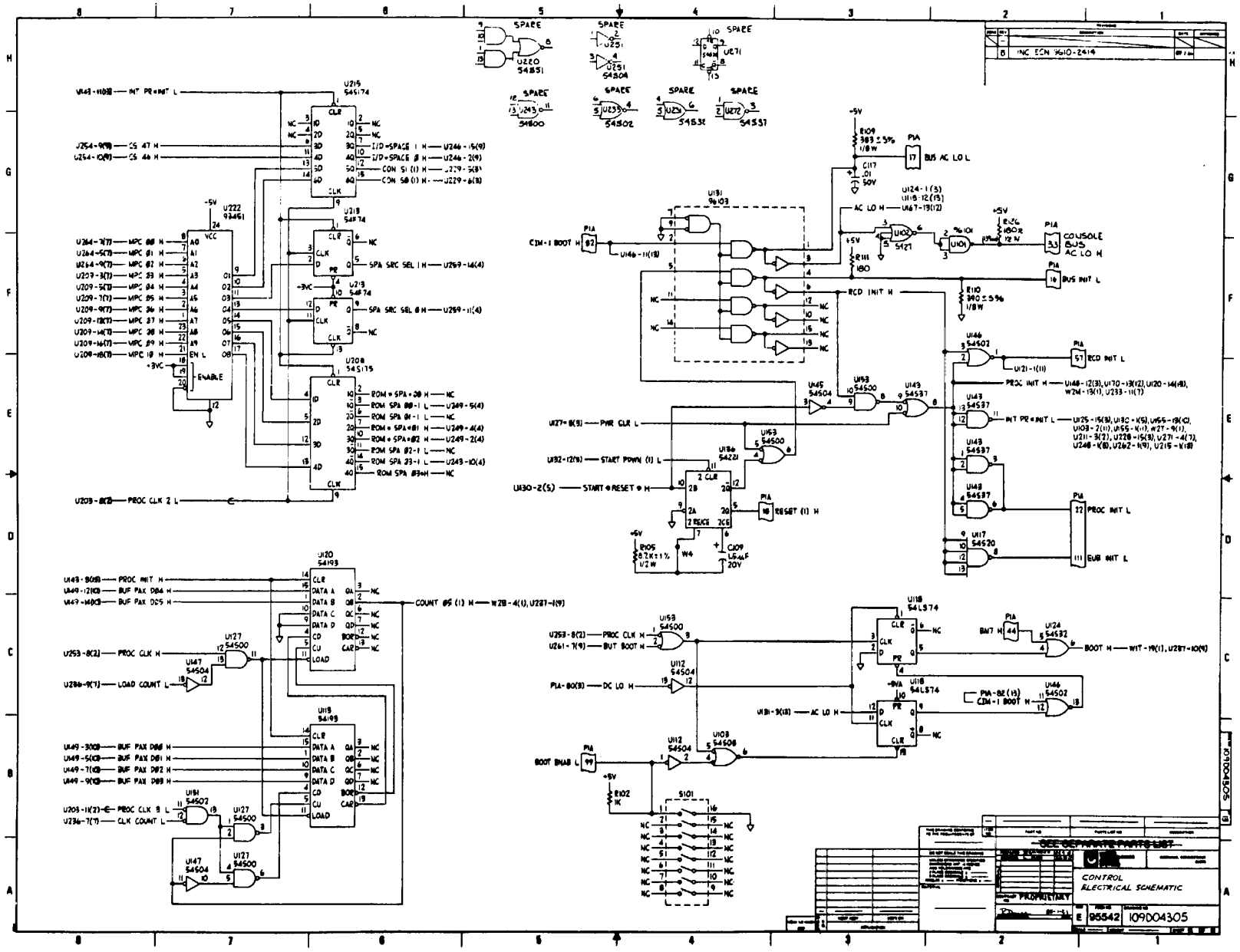
CONTROL SCHEMATIC
(Sheet 10 of 13)
I-60



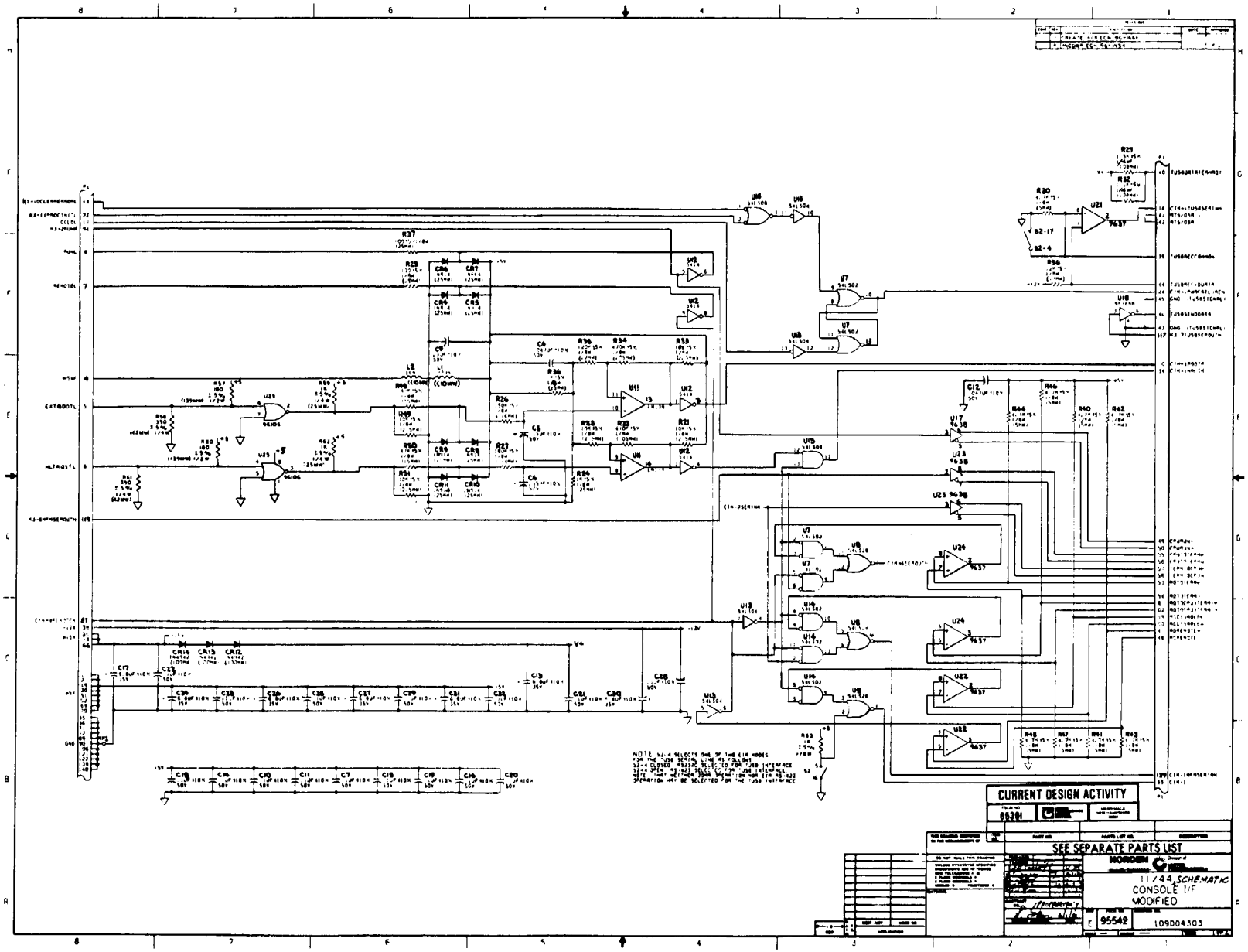
CONTROL SCHEMATIC
(Sheet 11 of 13)



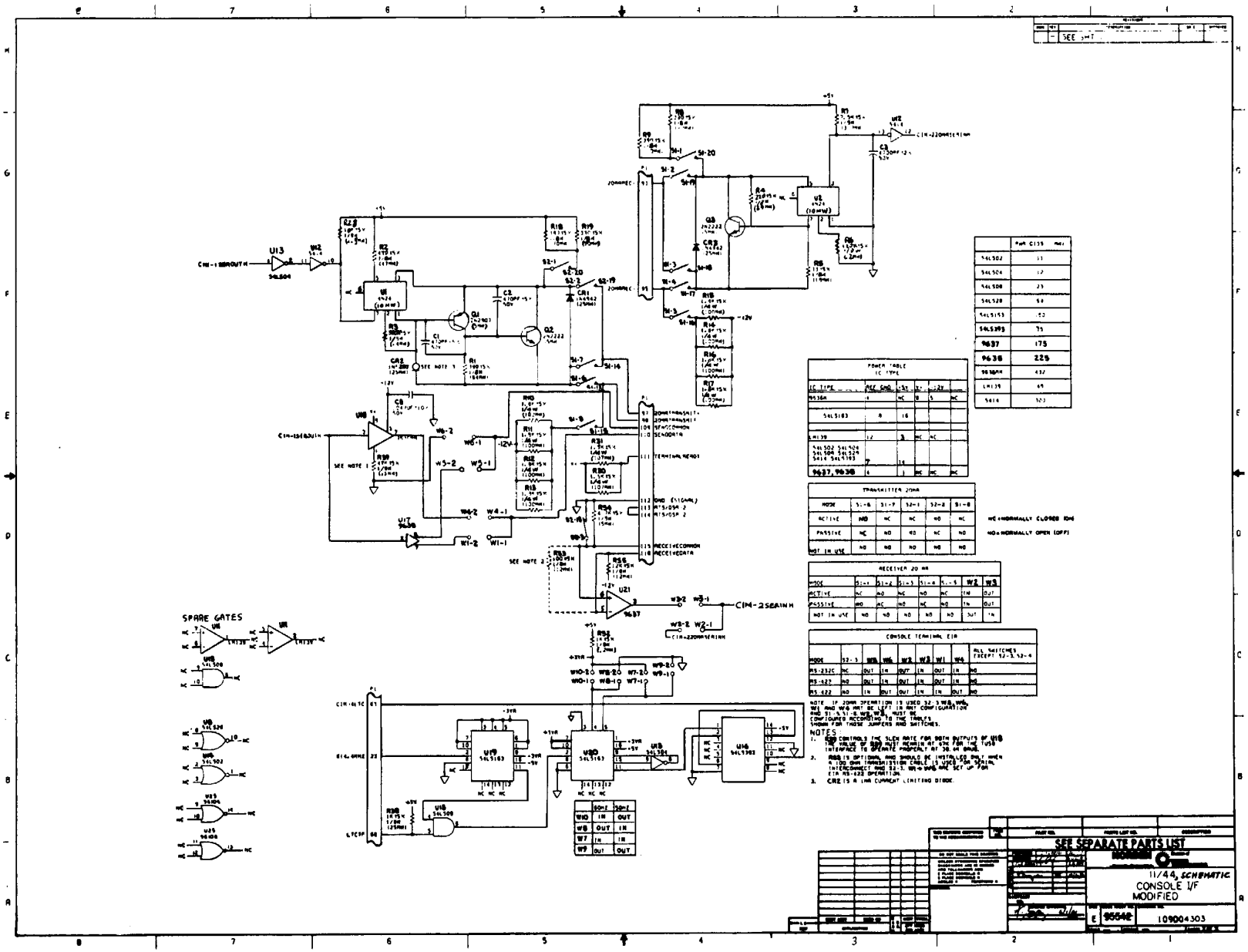
CONTROL SCHEMATIC
(Sheet 12 of 13)



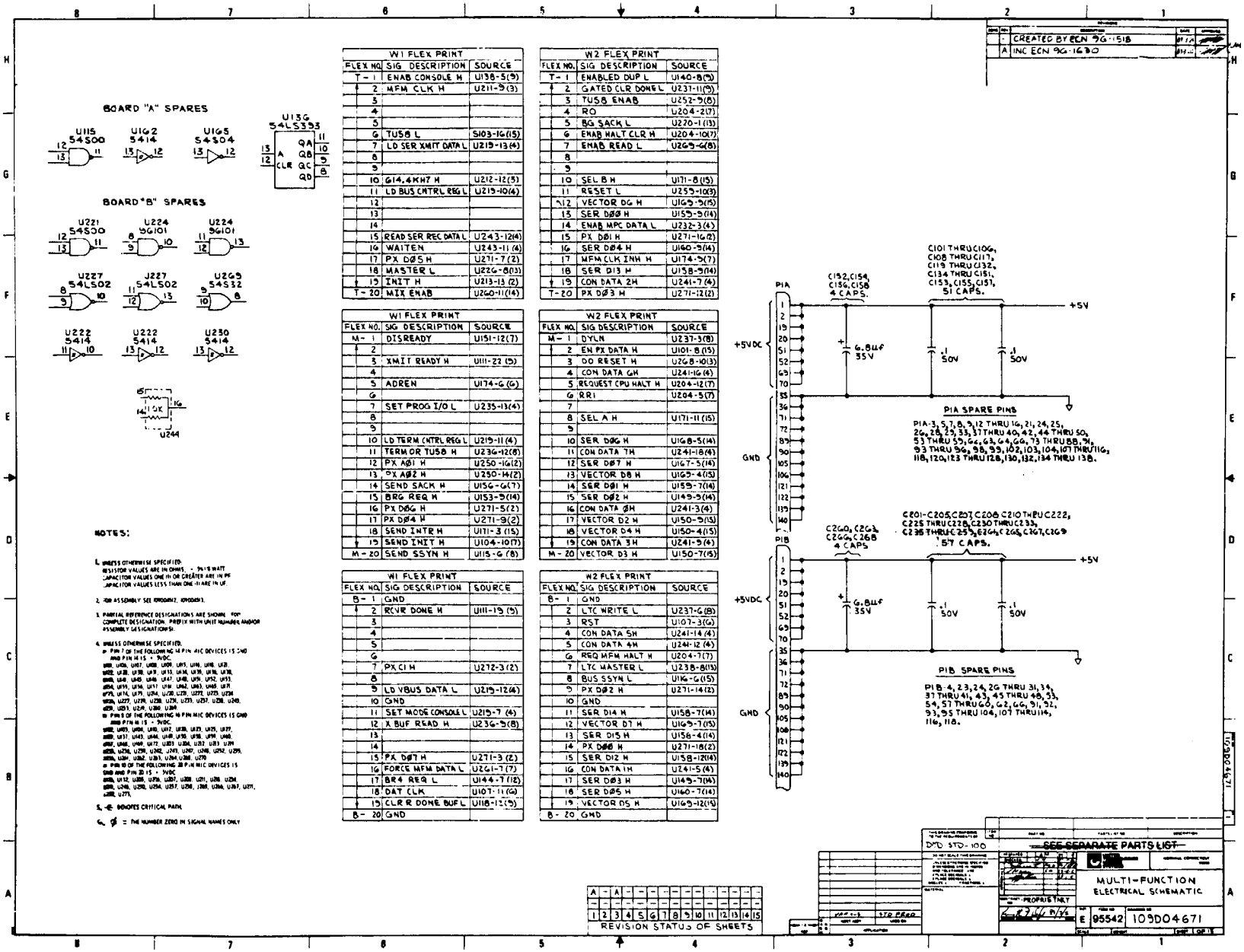
CONTROL SCHEMATIC
(Sheet 13 of 13)



CONSOLE I/F SCHEMATIC
(Sheet 1 of 2)

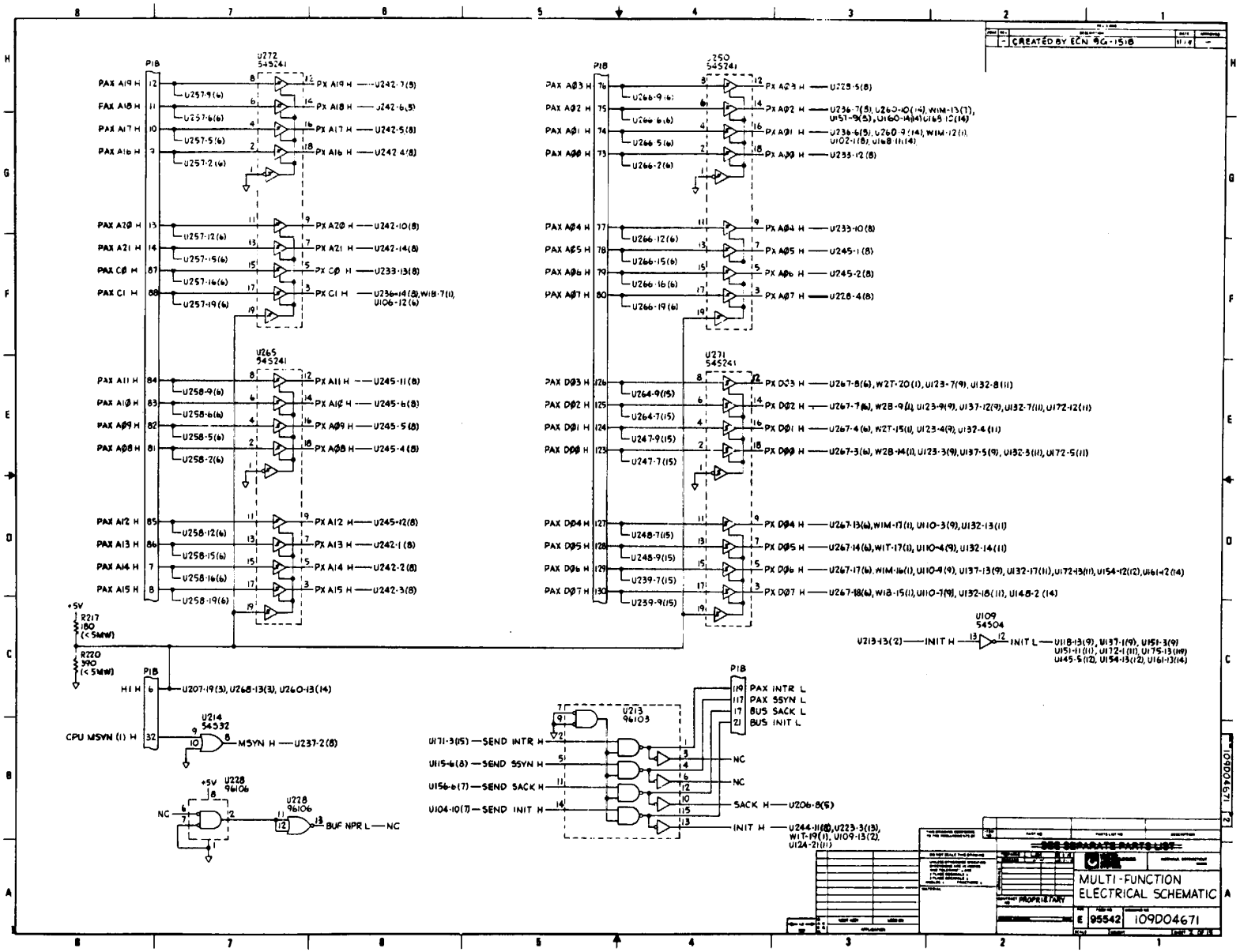


CONSOLE I/F SCHEMATIC
(Sheet 2 of 2)



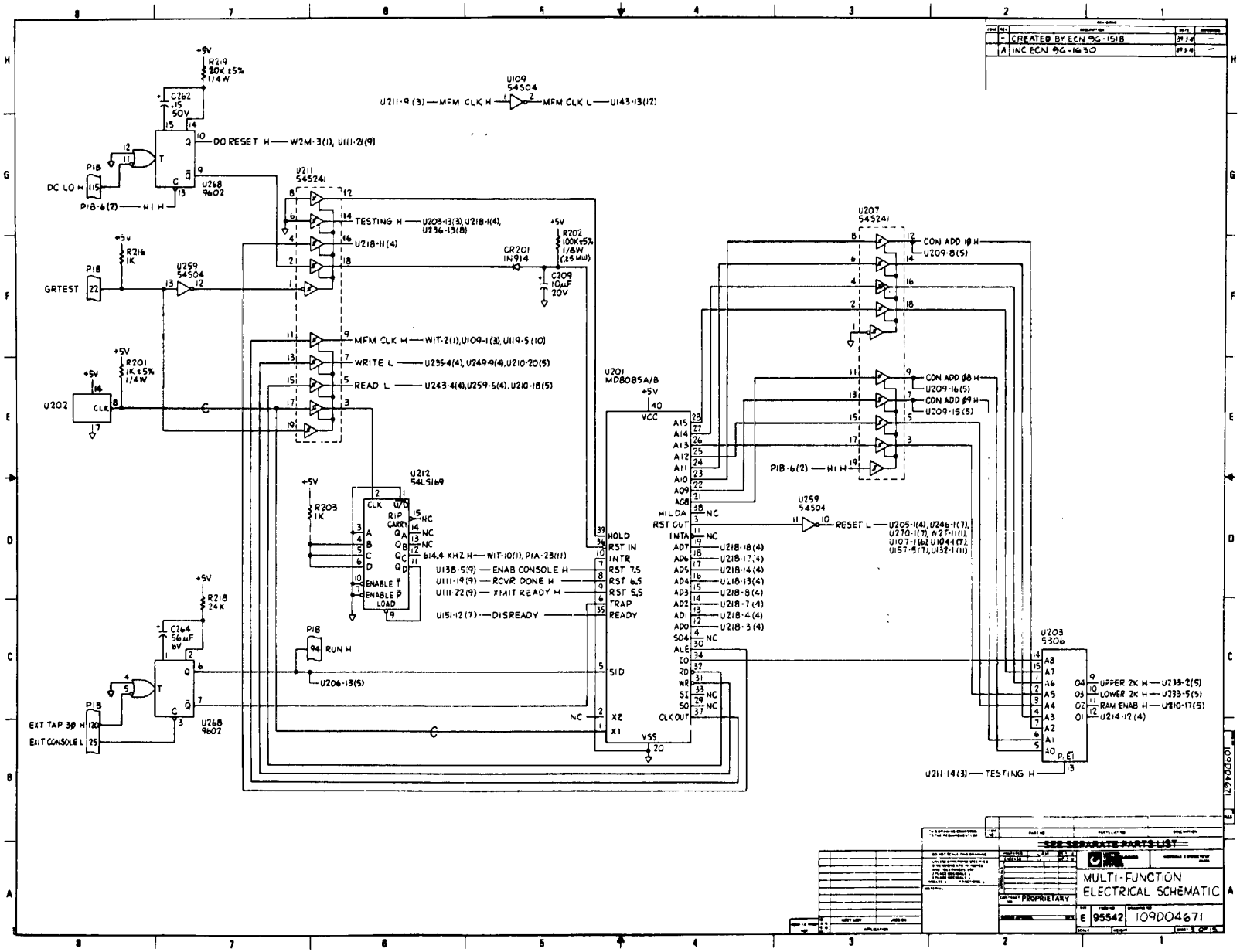
MULTI-FUNCTION SCHEMATIC

(Sheet 1 of 15)



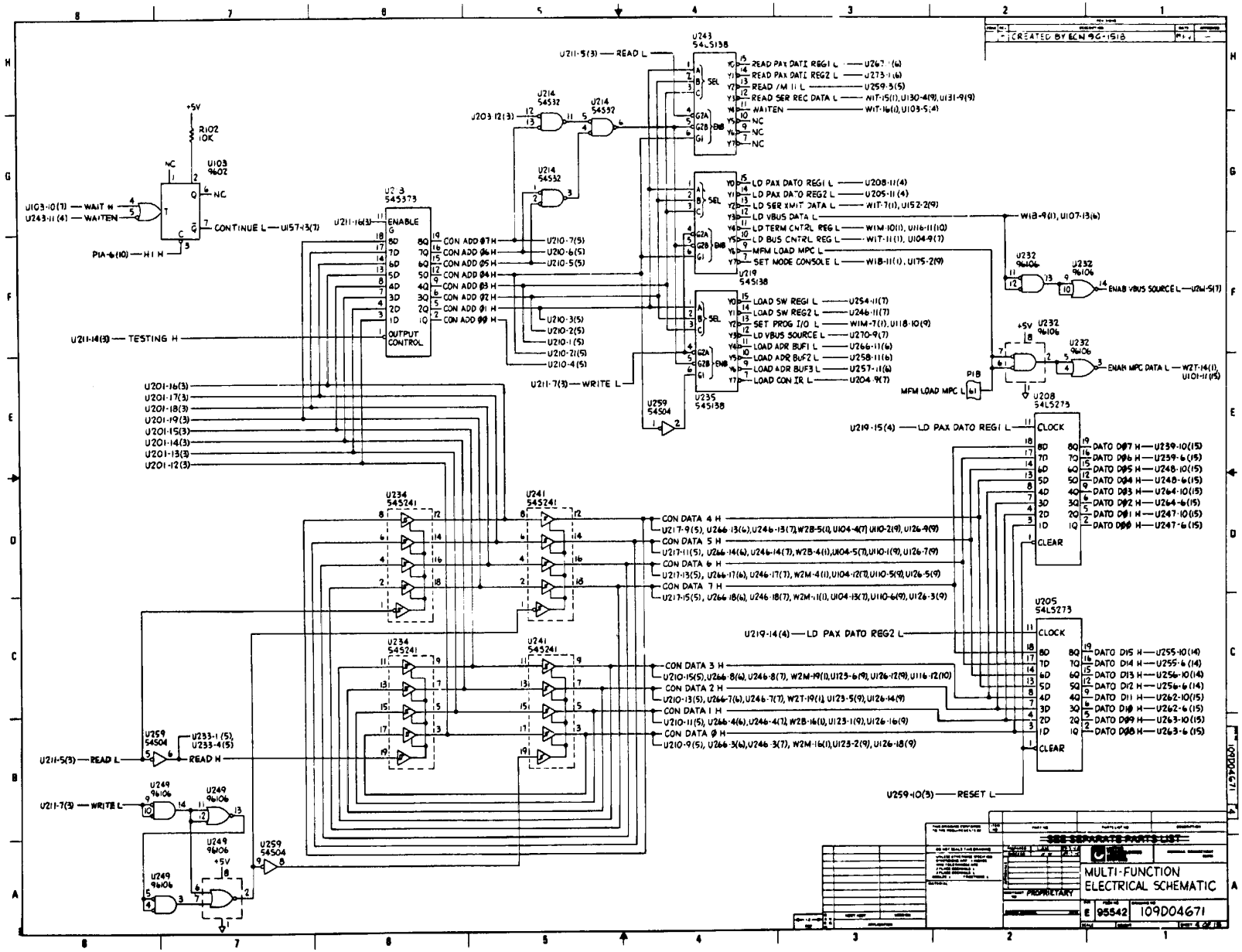
MULTI-FUNCTION SCHEMATIC

(Sheet 2 of 15)



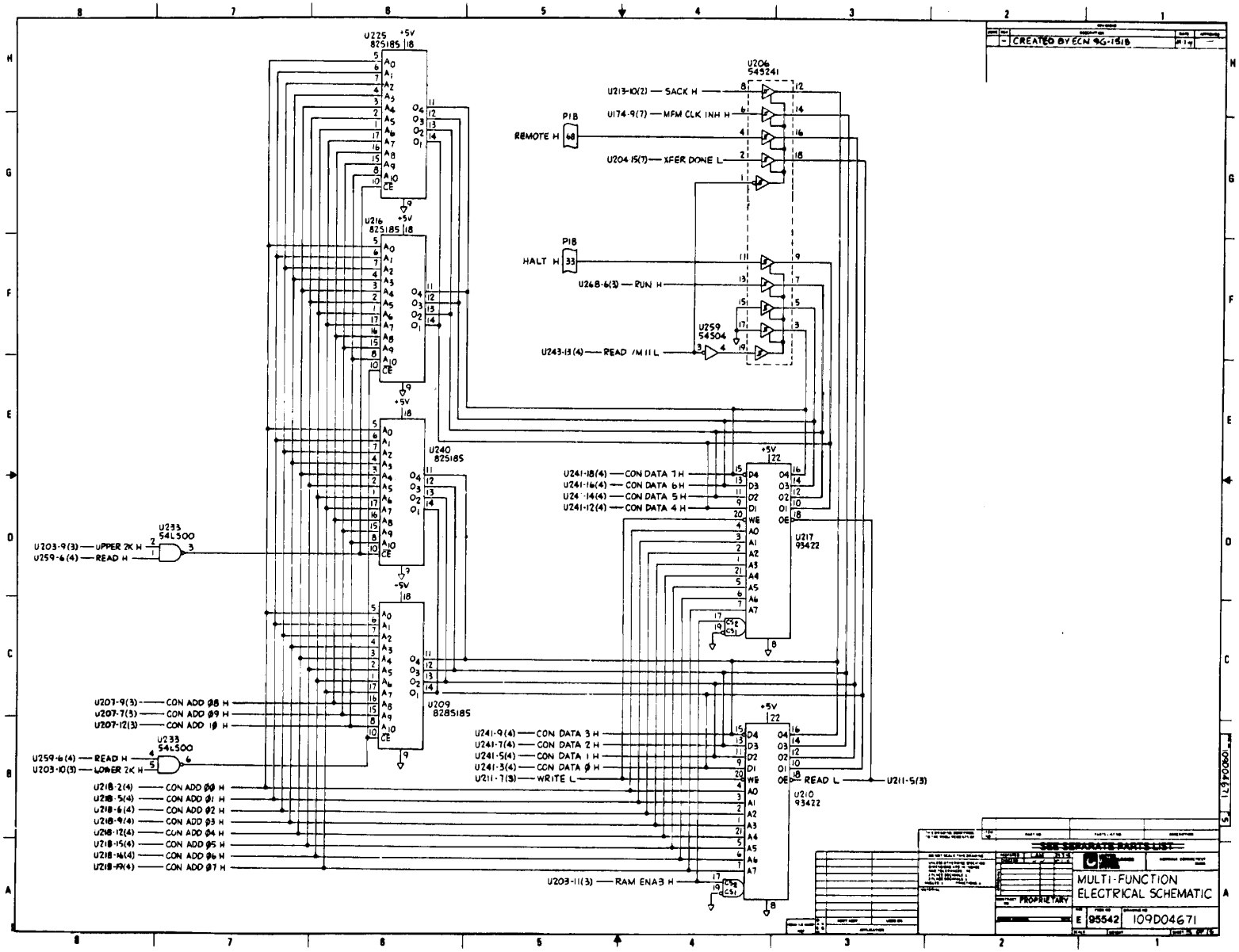
MULTI-FUNCTION SCHEMATIC

(Sheet 3 of 15)

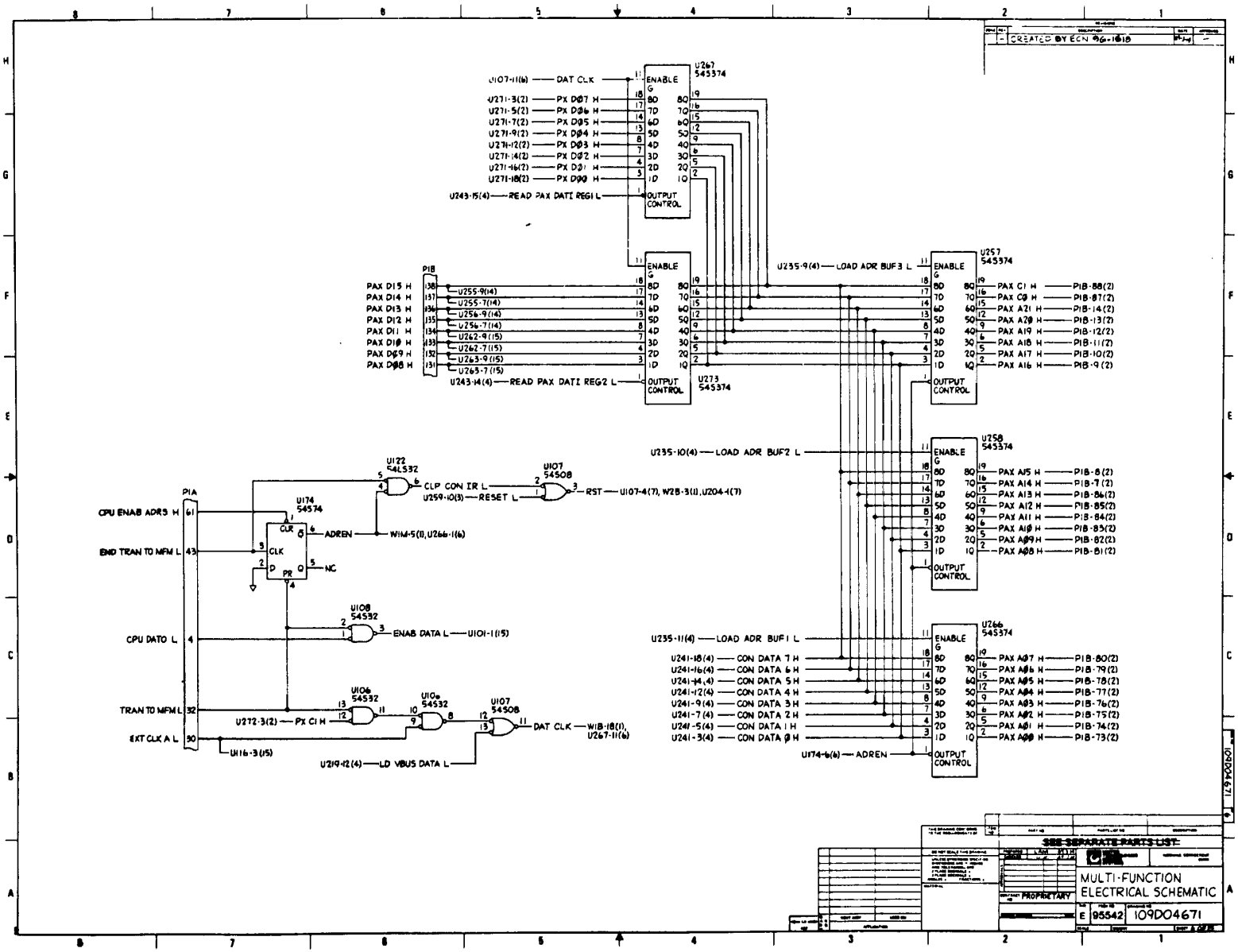


MULTI-FUNCTION SCHEMATIC

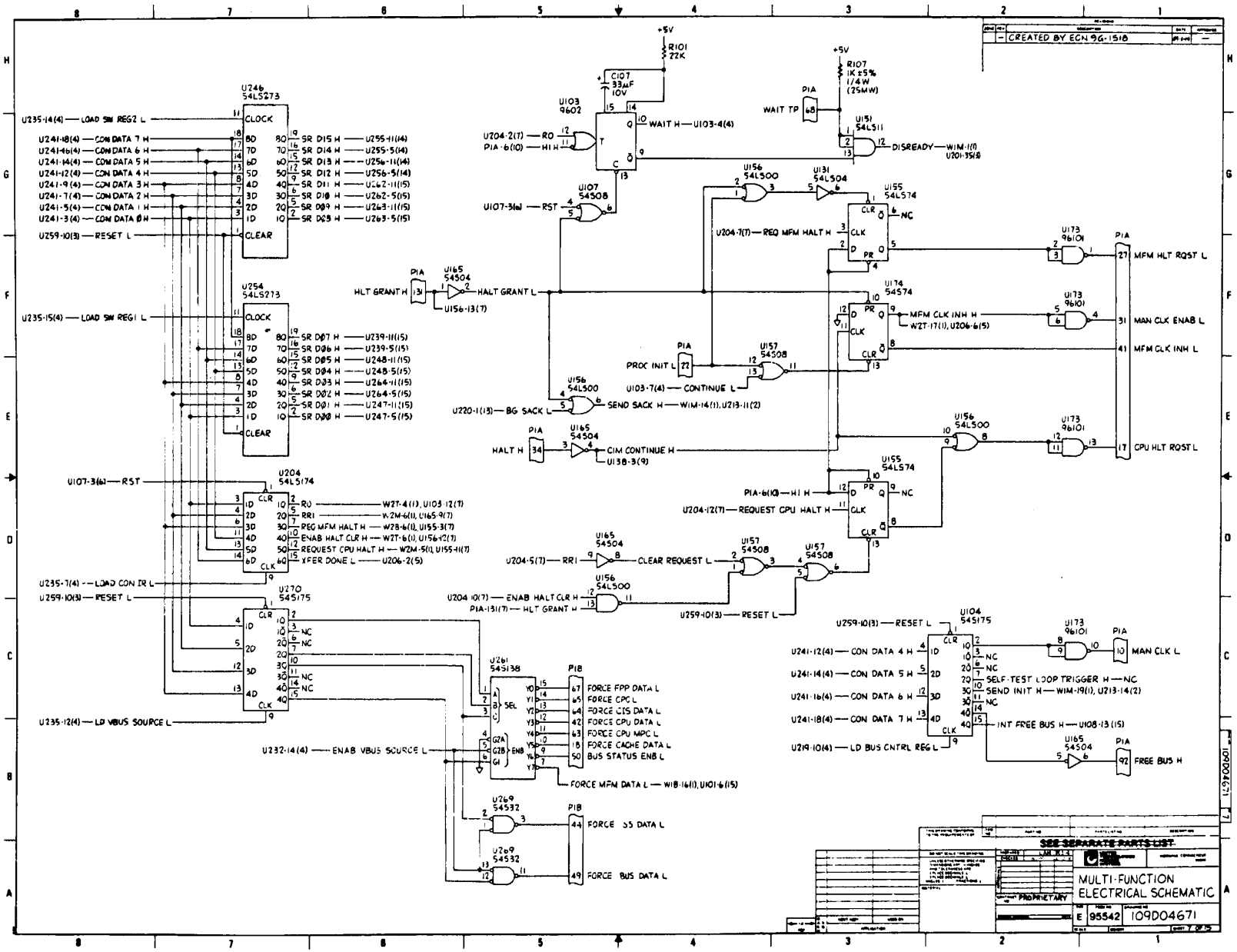
(Sheet 4 of 15)



MULTI-FUNCTION SCHEMATIC
(Sheet 5 of 15)

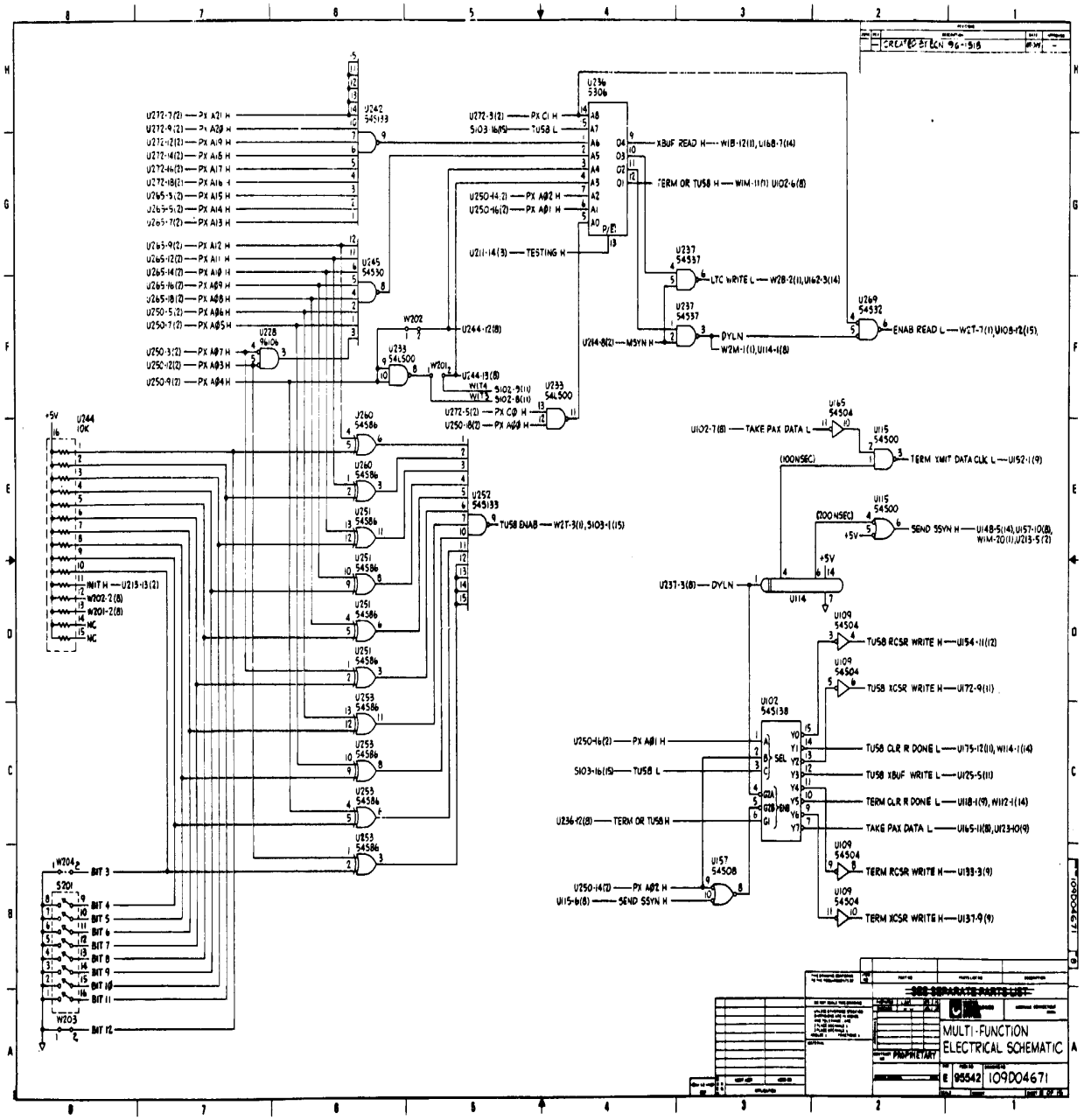


MULTI-FUNCTION SCHEMATIC
(Sheet 6 of 15)

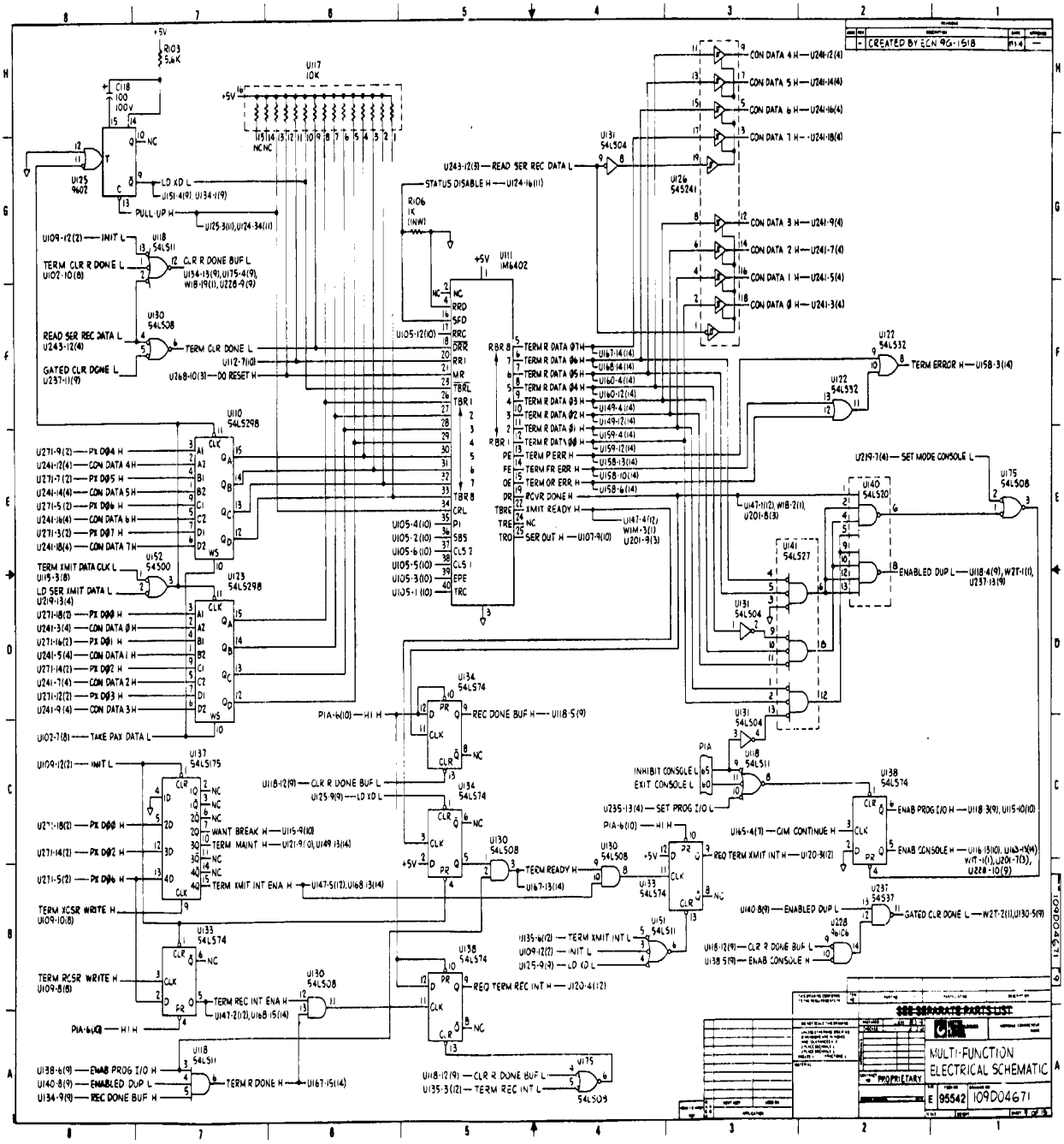


I1-72 MULTI-FUNCTION SCHEMATIC

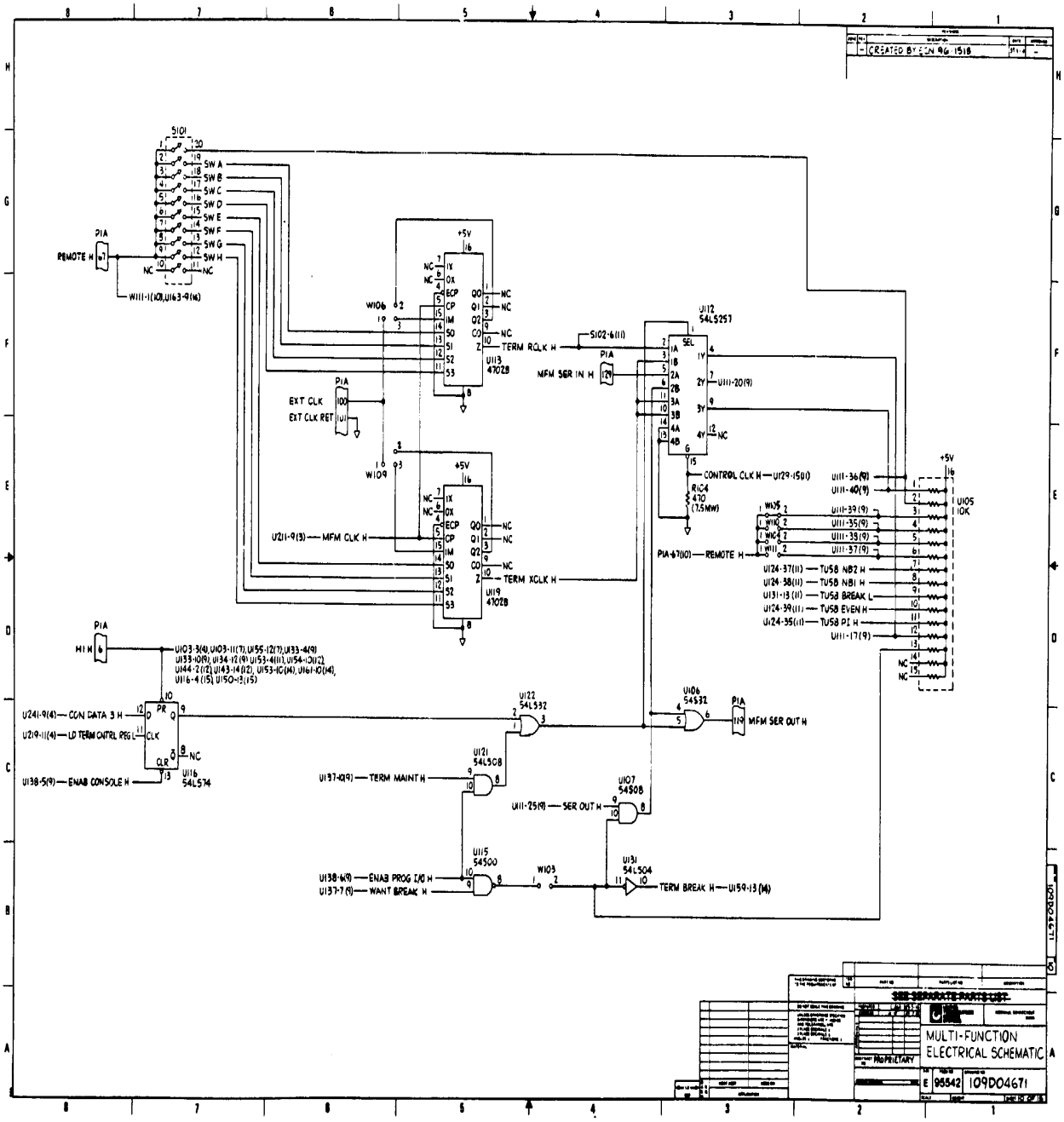
(Sheet 7 of 15)



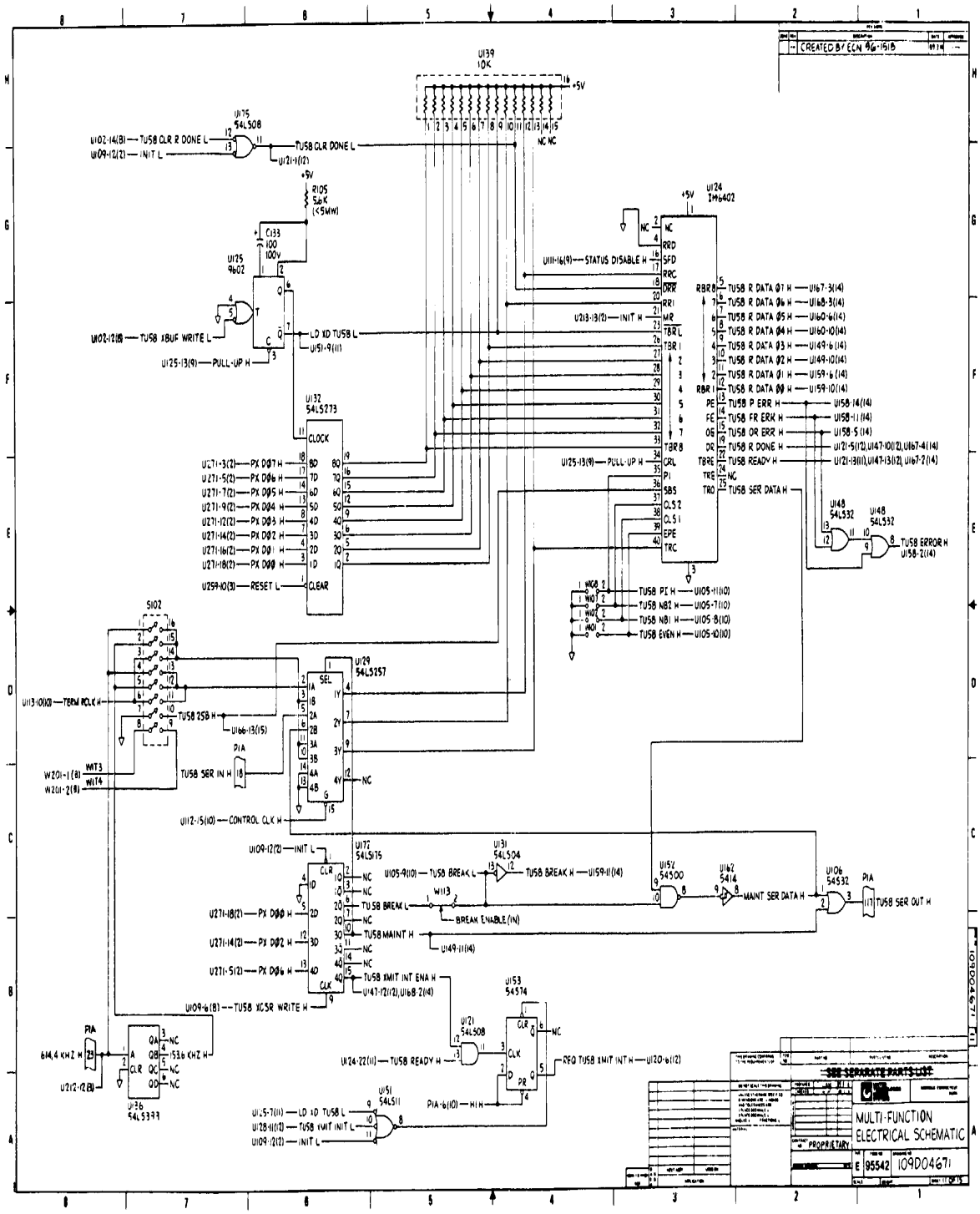
MULTI-FUNCTION SCHEMATIC
(Sheet 8 of 15)



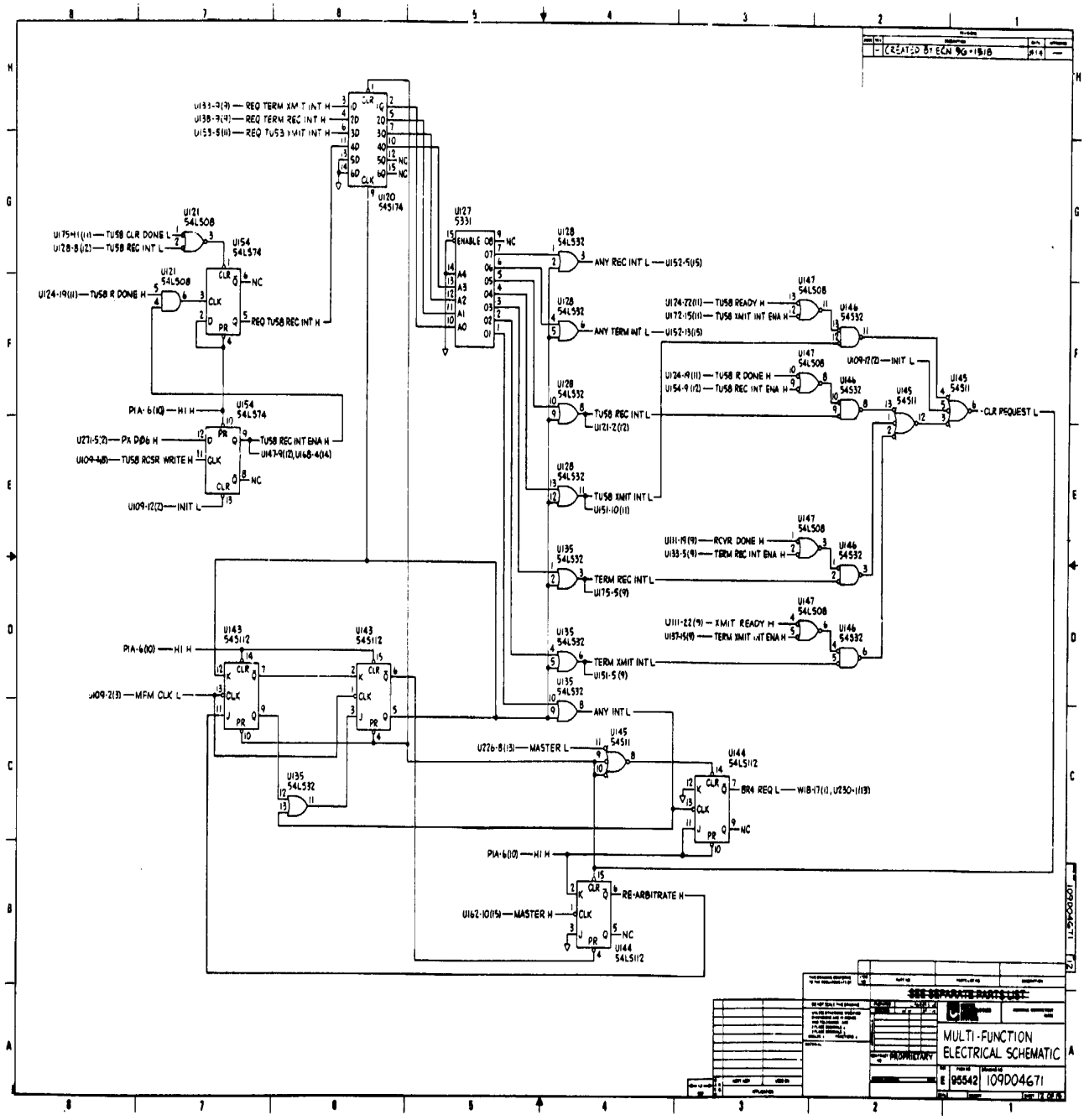
MULTI-FUNCTIN SCHEMATIC
(Sheet 9 of 15)



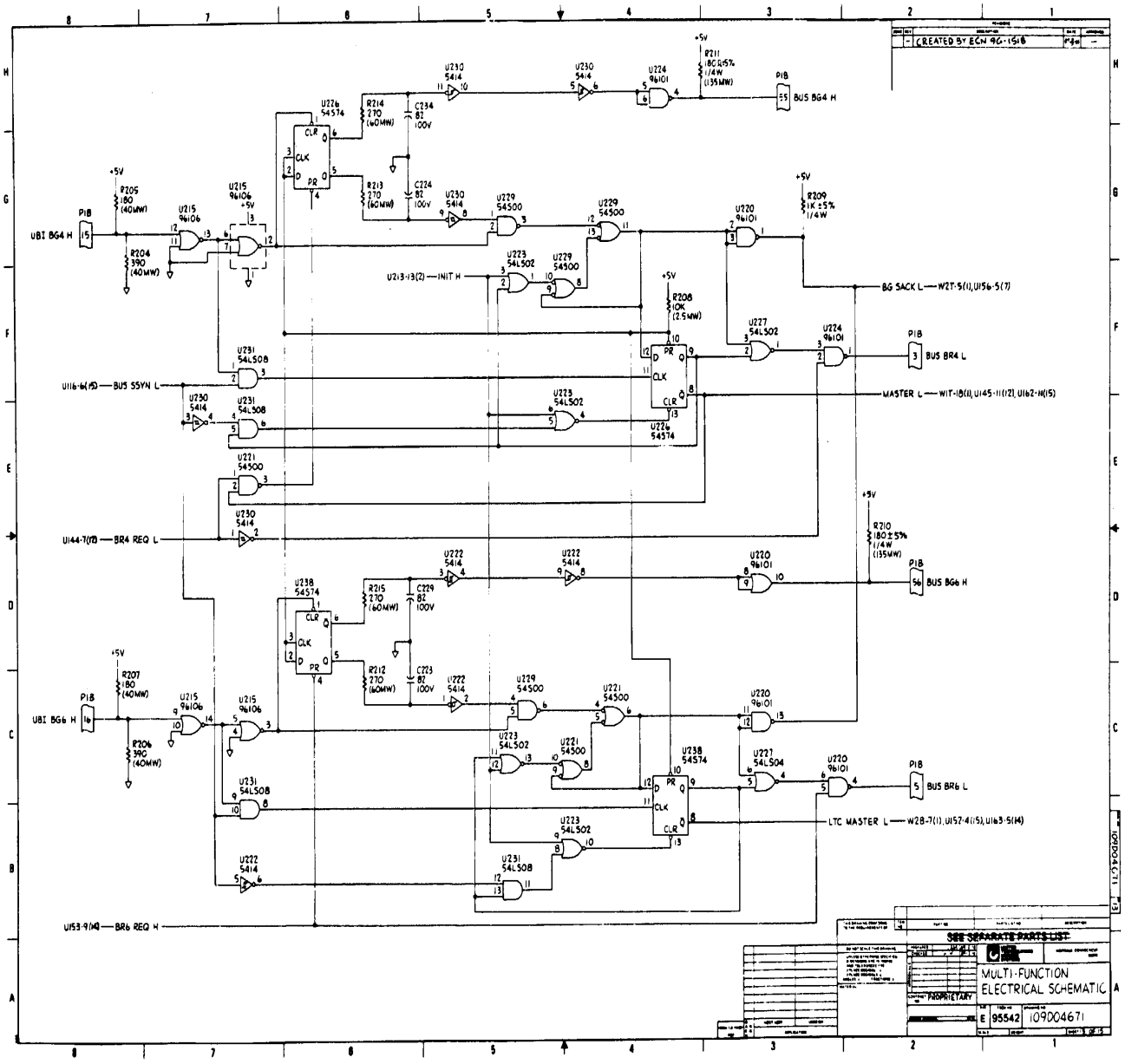
MULTI-FUNCTIION SCHEMATIC
(Sheet 10 of 15)



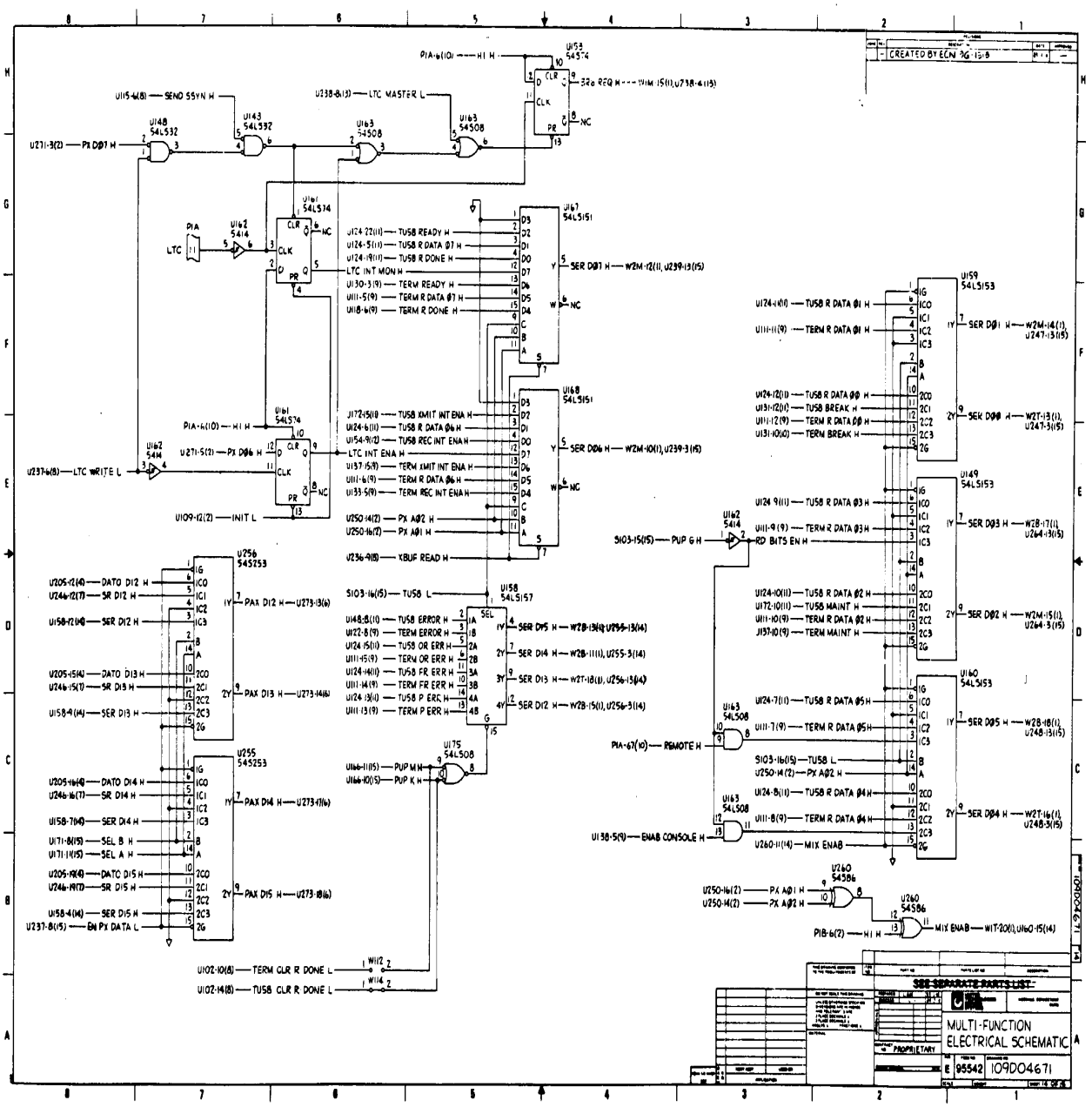
MULTI-FUNCTION SCHEMATIC
(Sheet 11 of 15)



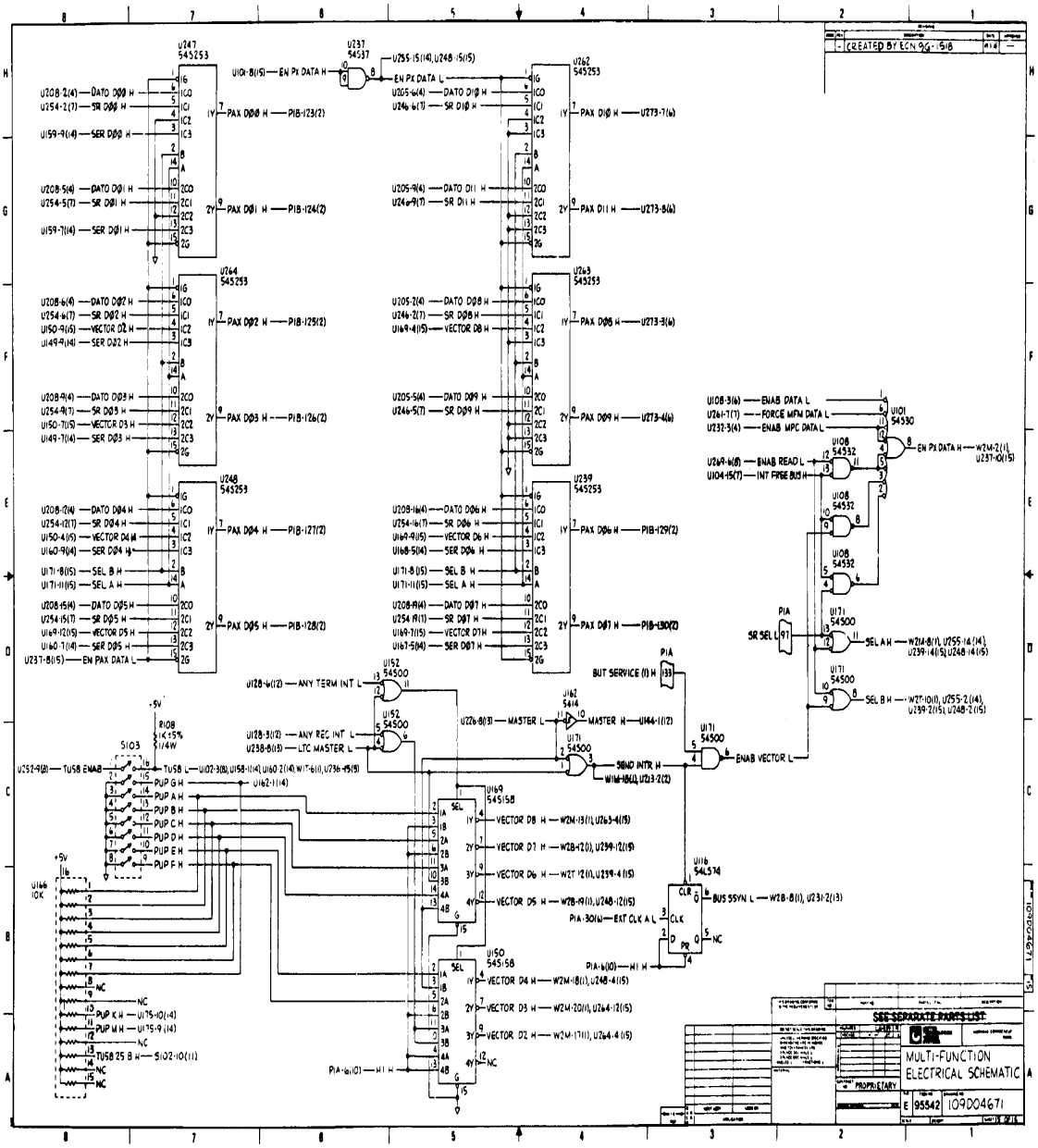
MULTI-FUNCTION SCHEMATIC
(Sheet 12 of 15)



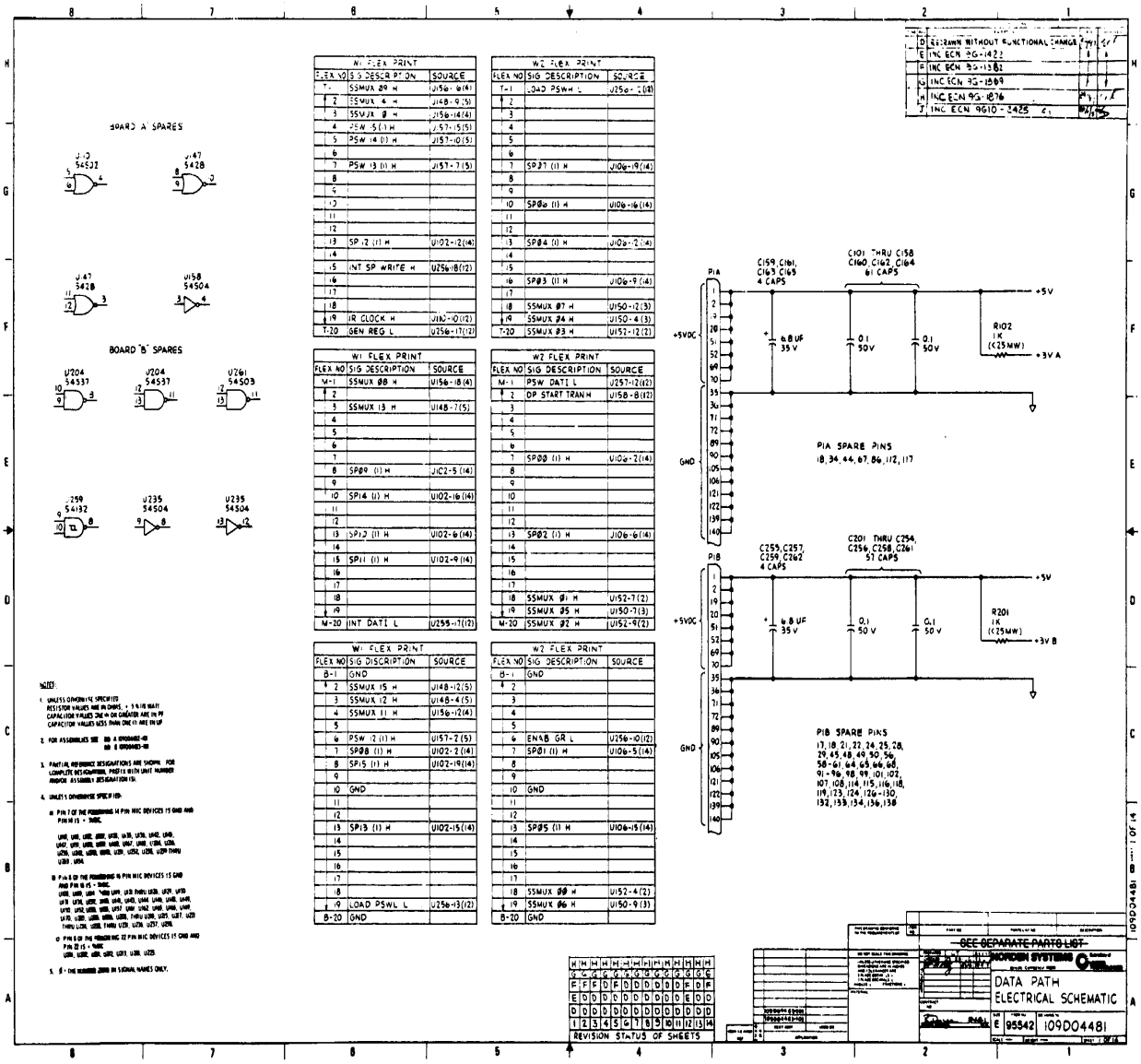
MULTI-FUNCTION SCHEMATIC
(Sheet 13 of 15)



MULTI-FUNCTION SCHEMATIC
(Sheet 14 of 15)

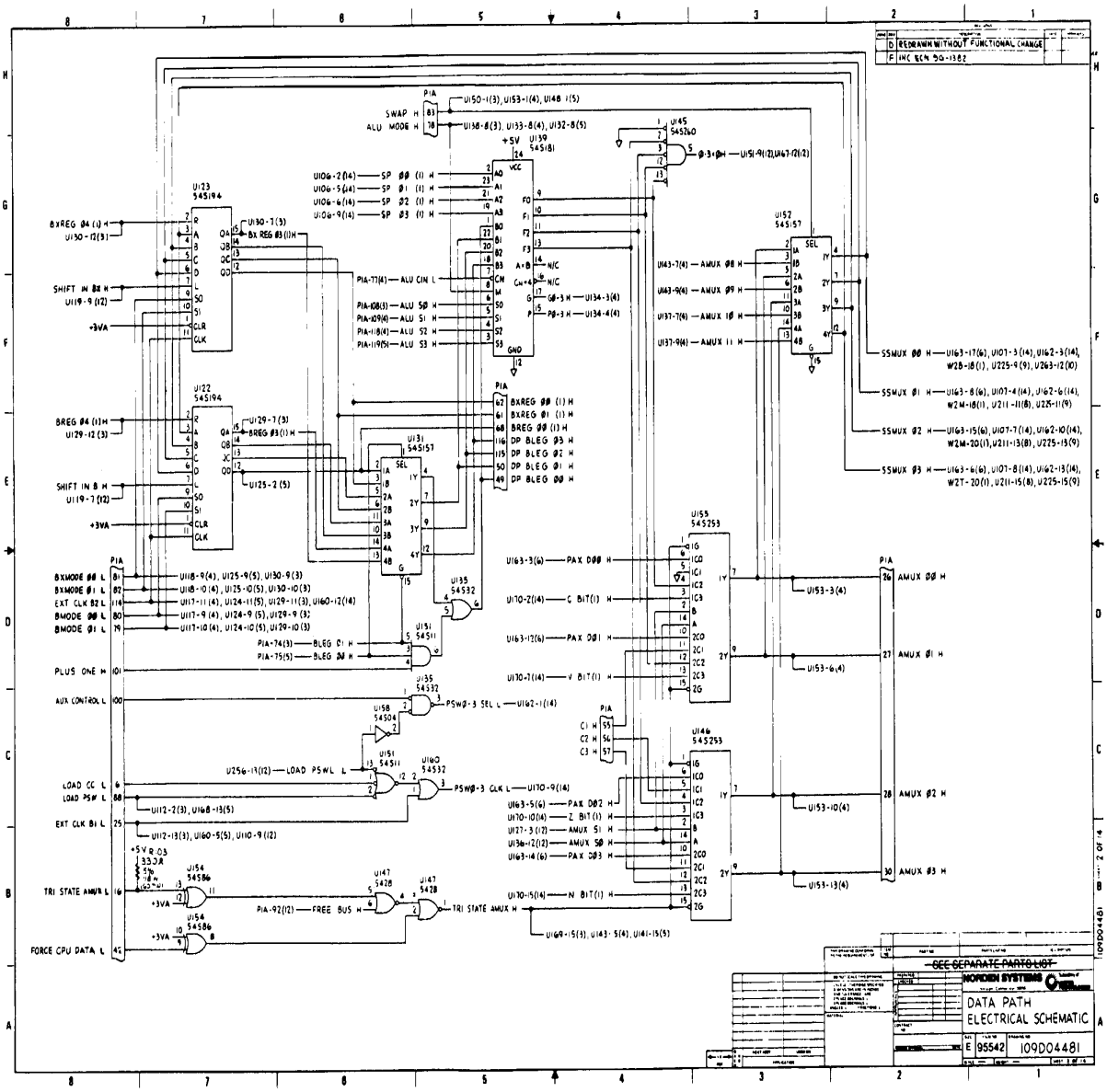


MULTI-FUNCTION SCHEMATIC
(Sheet 15 of 15)



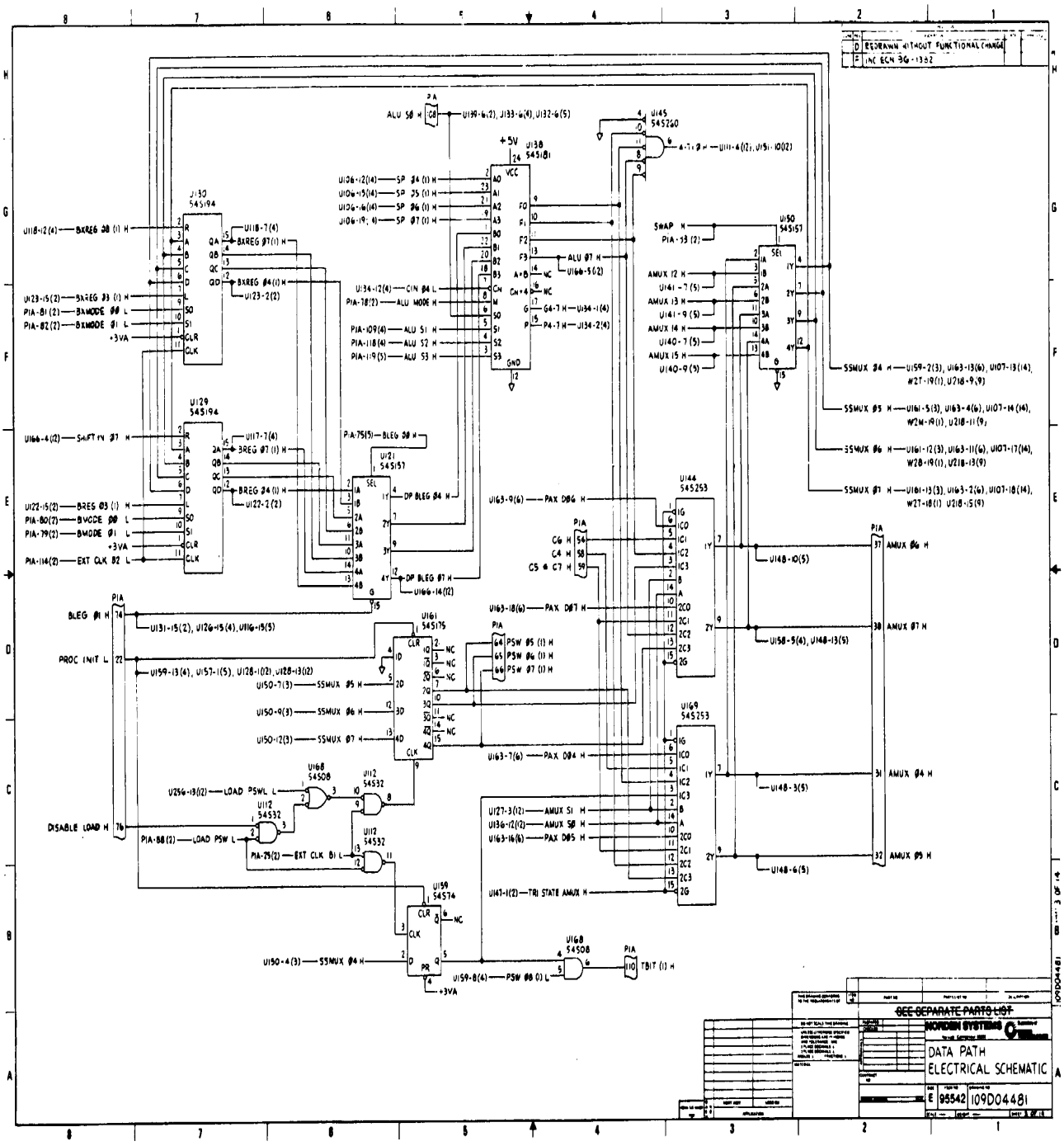
DATA PATH SCHEMATIC

(Sheet 1 of 14)



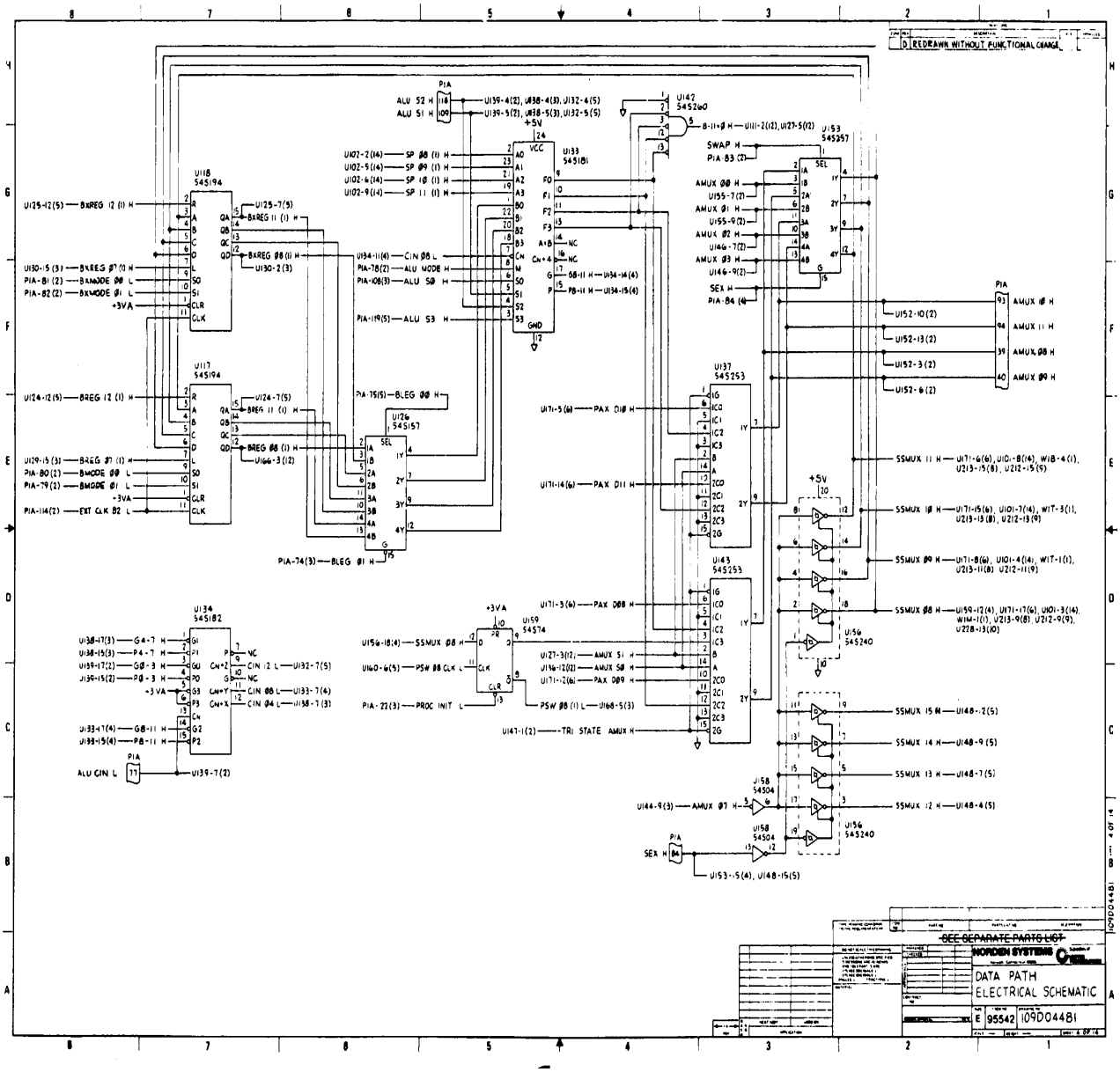
DATA PATH SCHEMATIC

(Sheet 2 of 14)



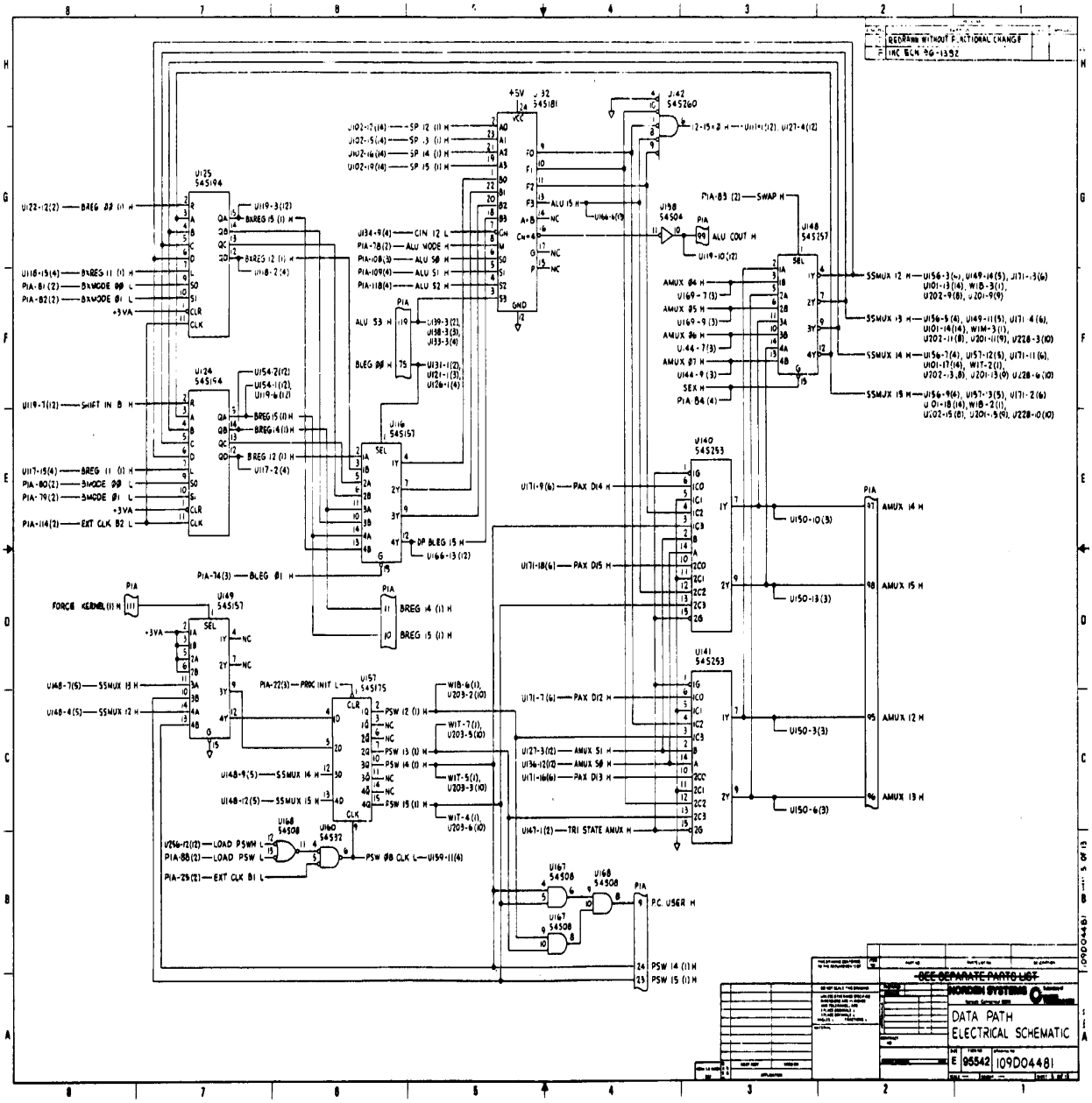
DATA PATH SCHEMATIC

(Sheet 3 of 14)



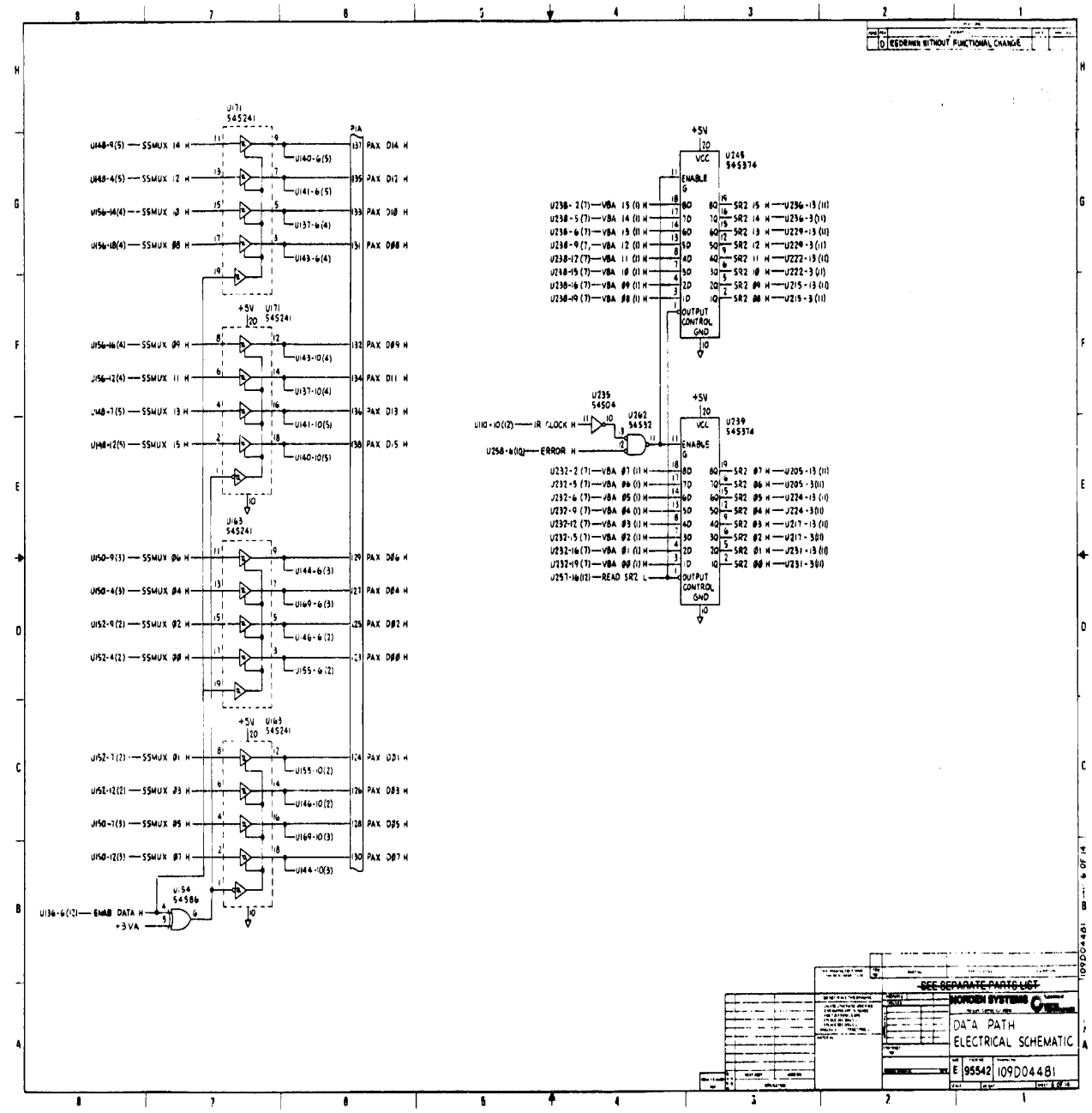
DATA PATH SCHEMATIC

(Sheet 4 of 15)



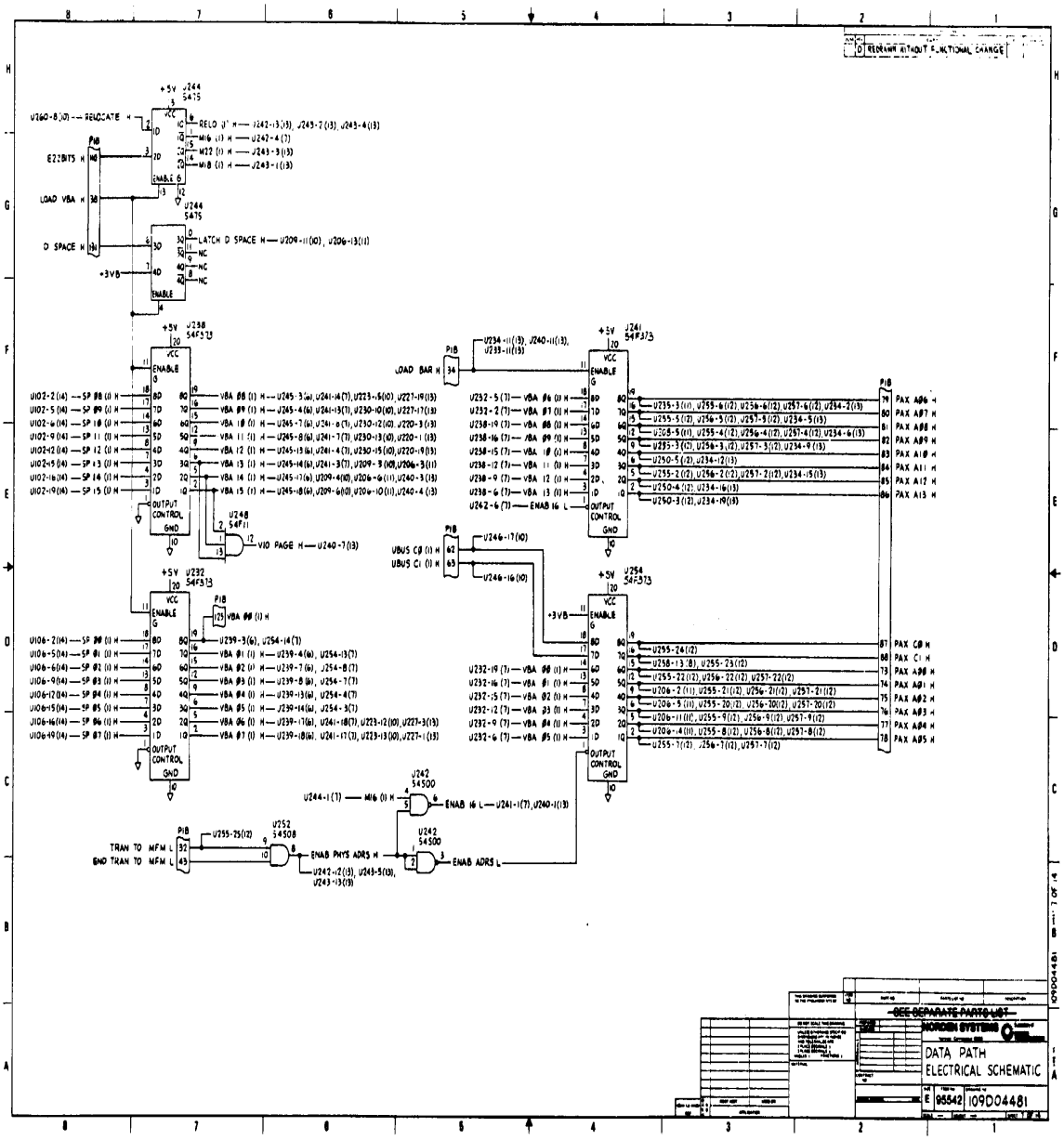
DATA PATH SCHEMATIC

(Sheet 5 of 14)



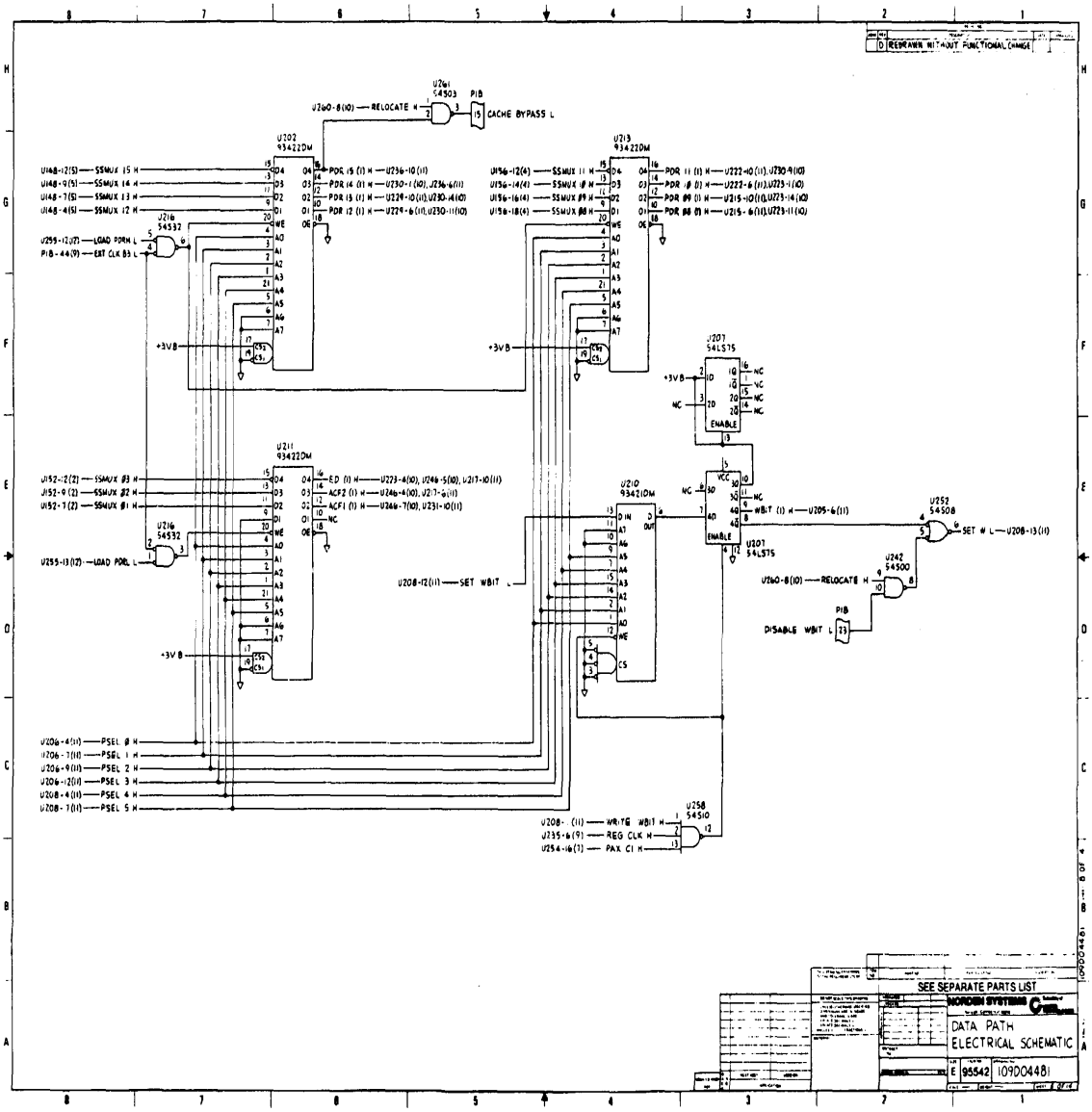
DATA PATH SCHEMATIC

(Sheet 6 of 14)



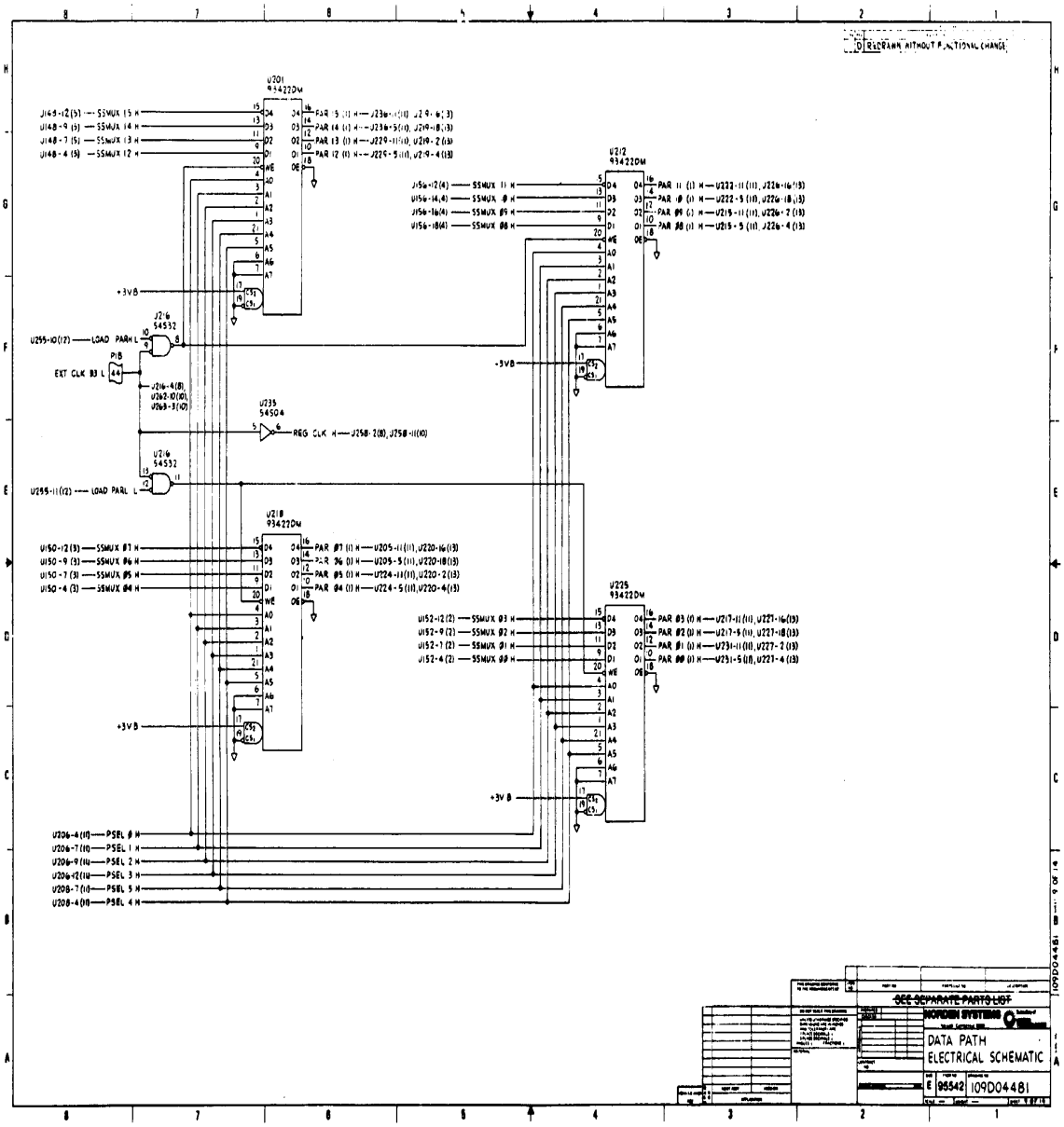
DATA PATH SCHEMATIC

(Sheet 7 of 14)

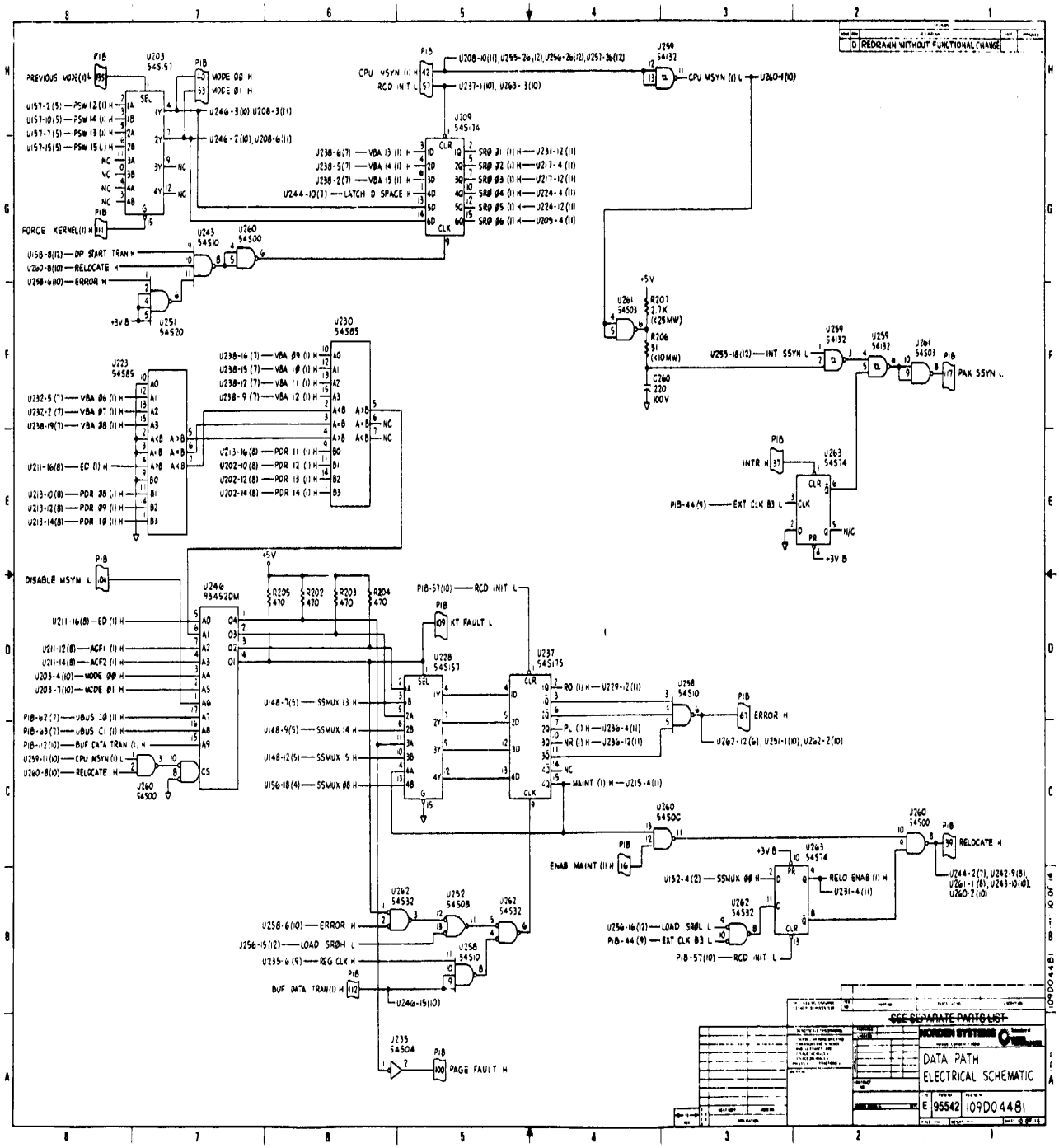


DATA PATH SCHEMATIC

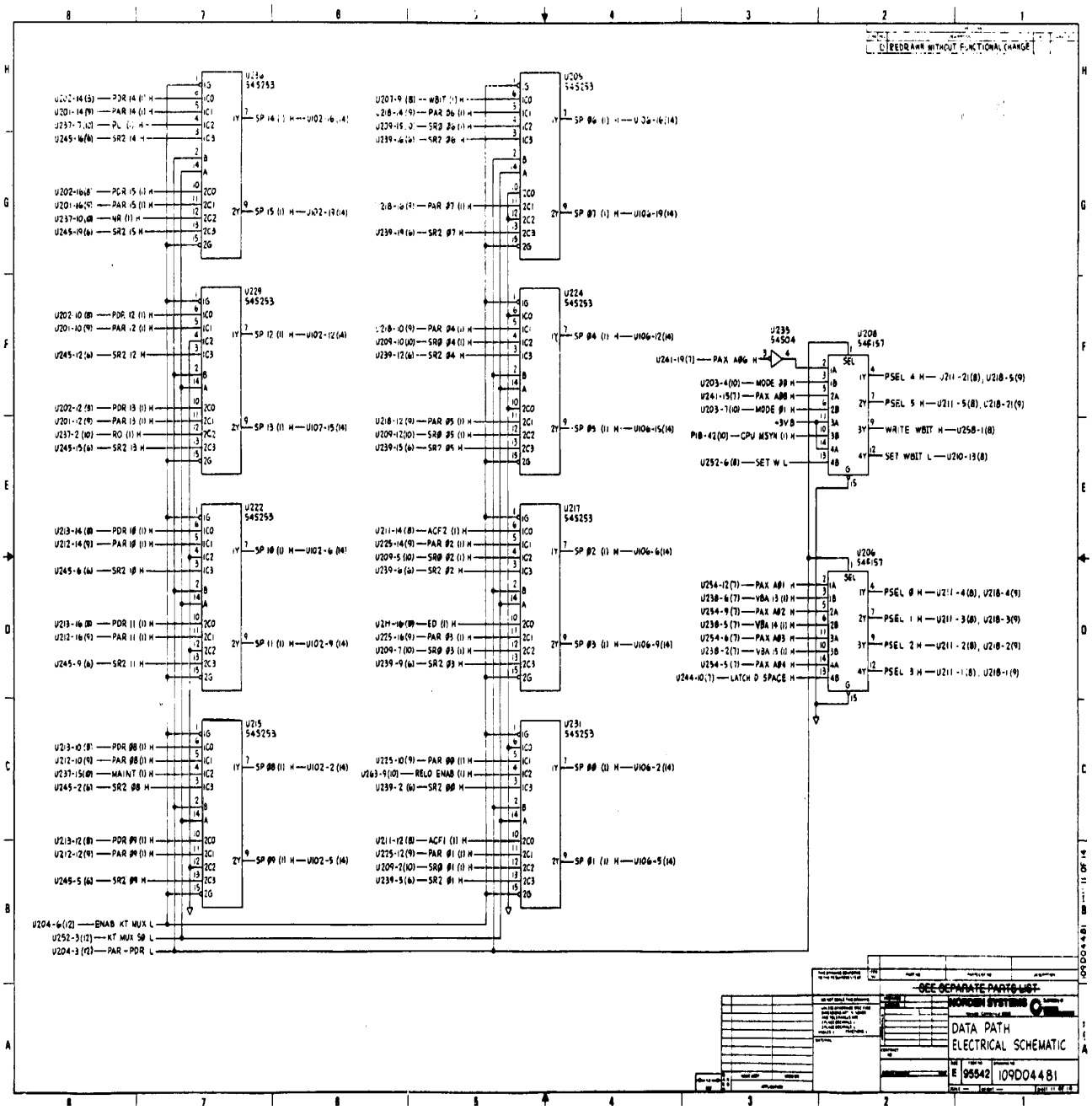
(Sheet 8 of 14)



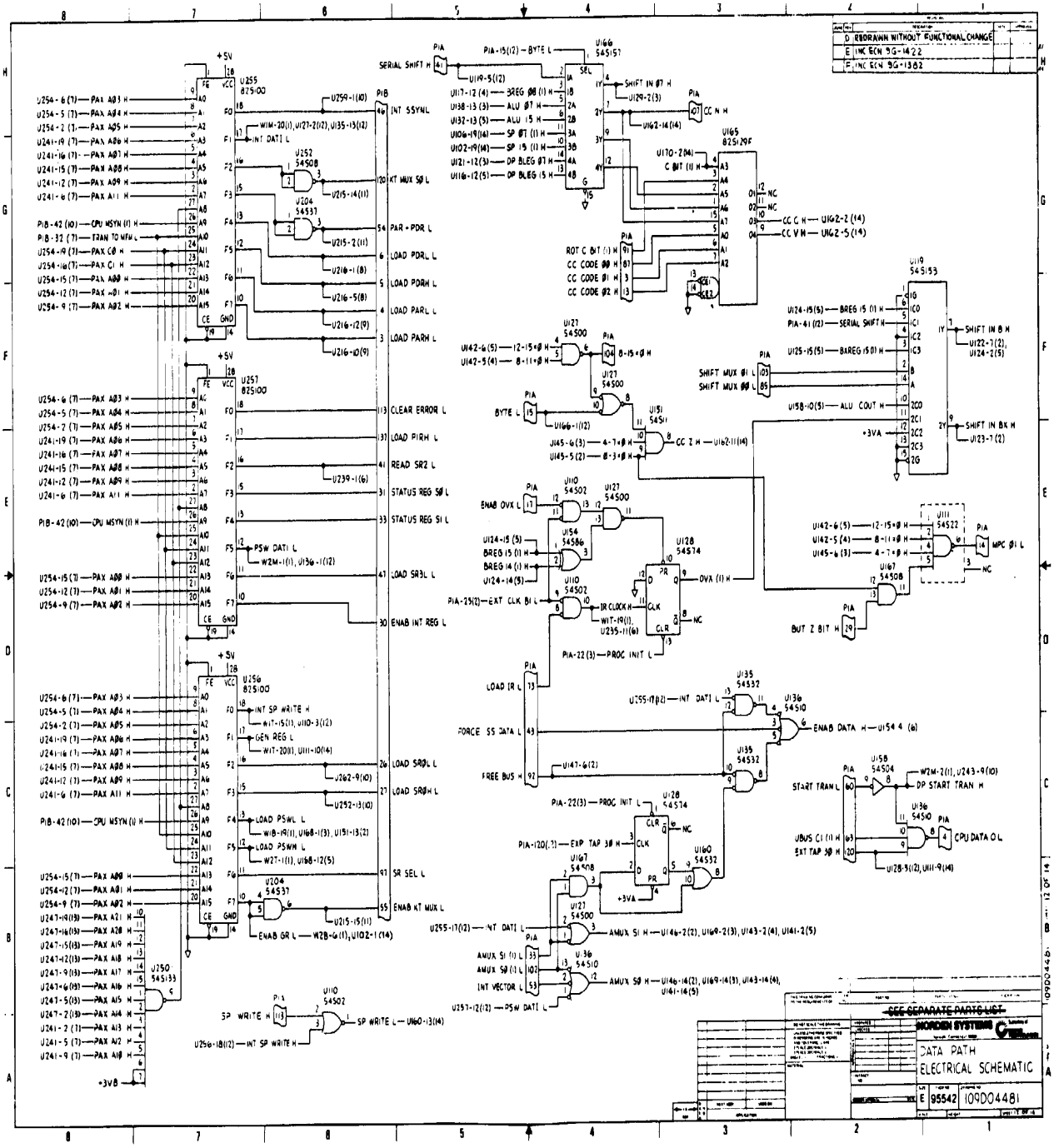
DATA PATH SCHEMATIC
(Sheet 9 of 14)



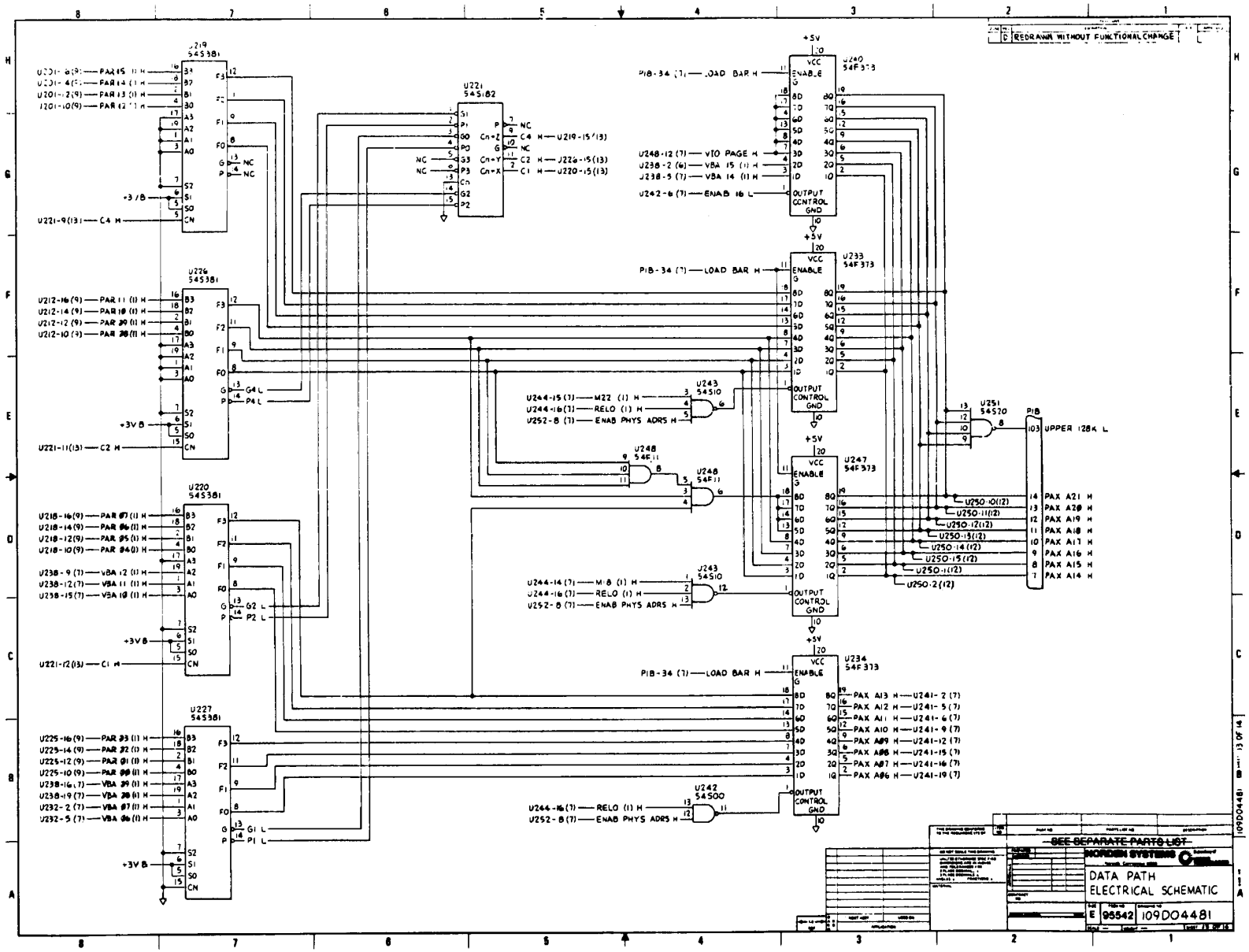
DATA PATH SCHEMATIC
(Sheet 10 of 14)



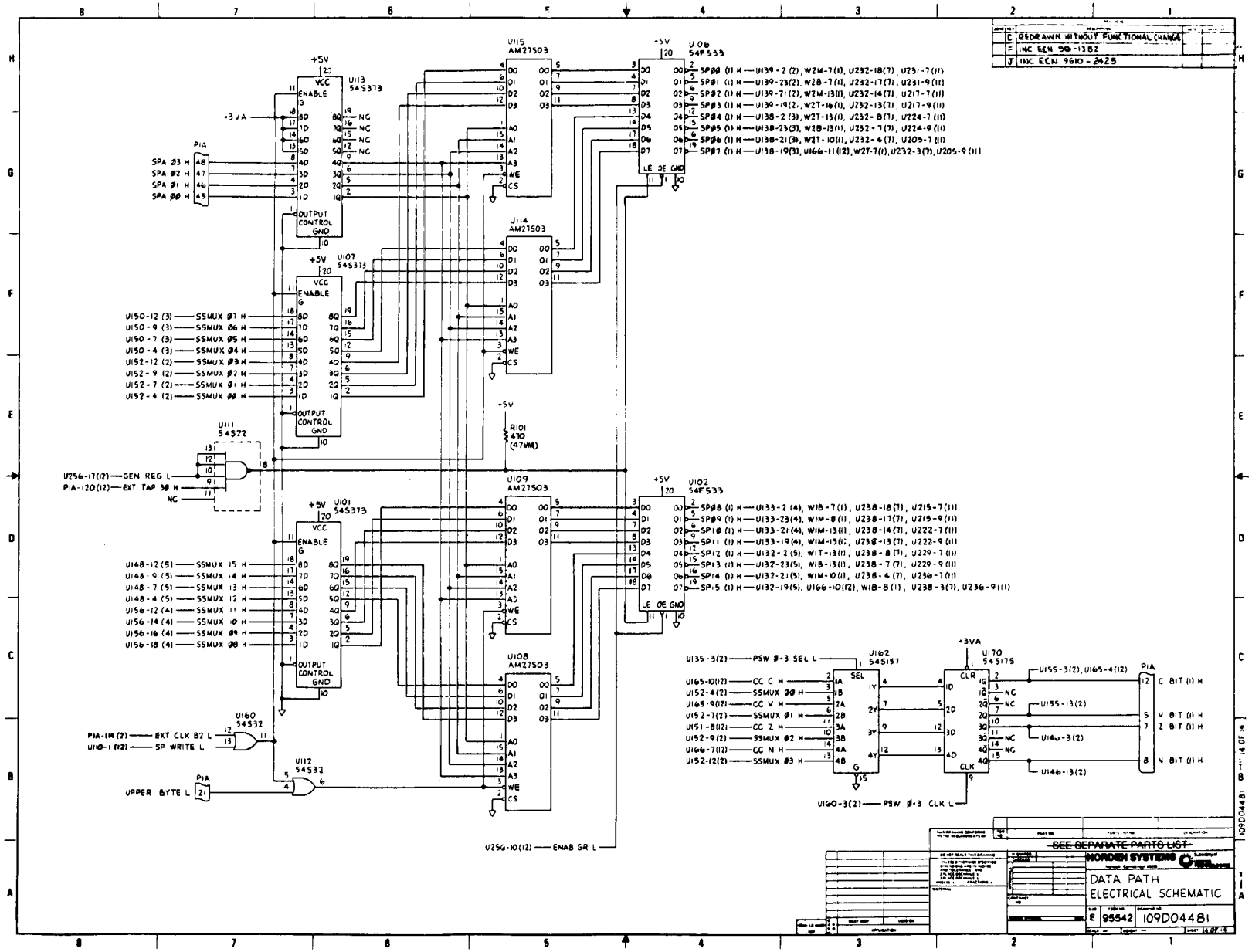
DATA PATH SCHEMATIC
(Sheet 11 of 14)



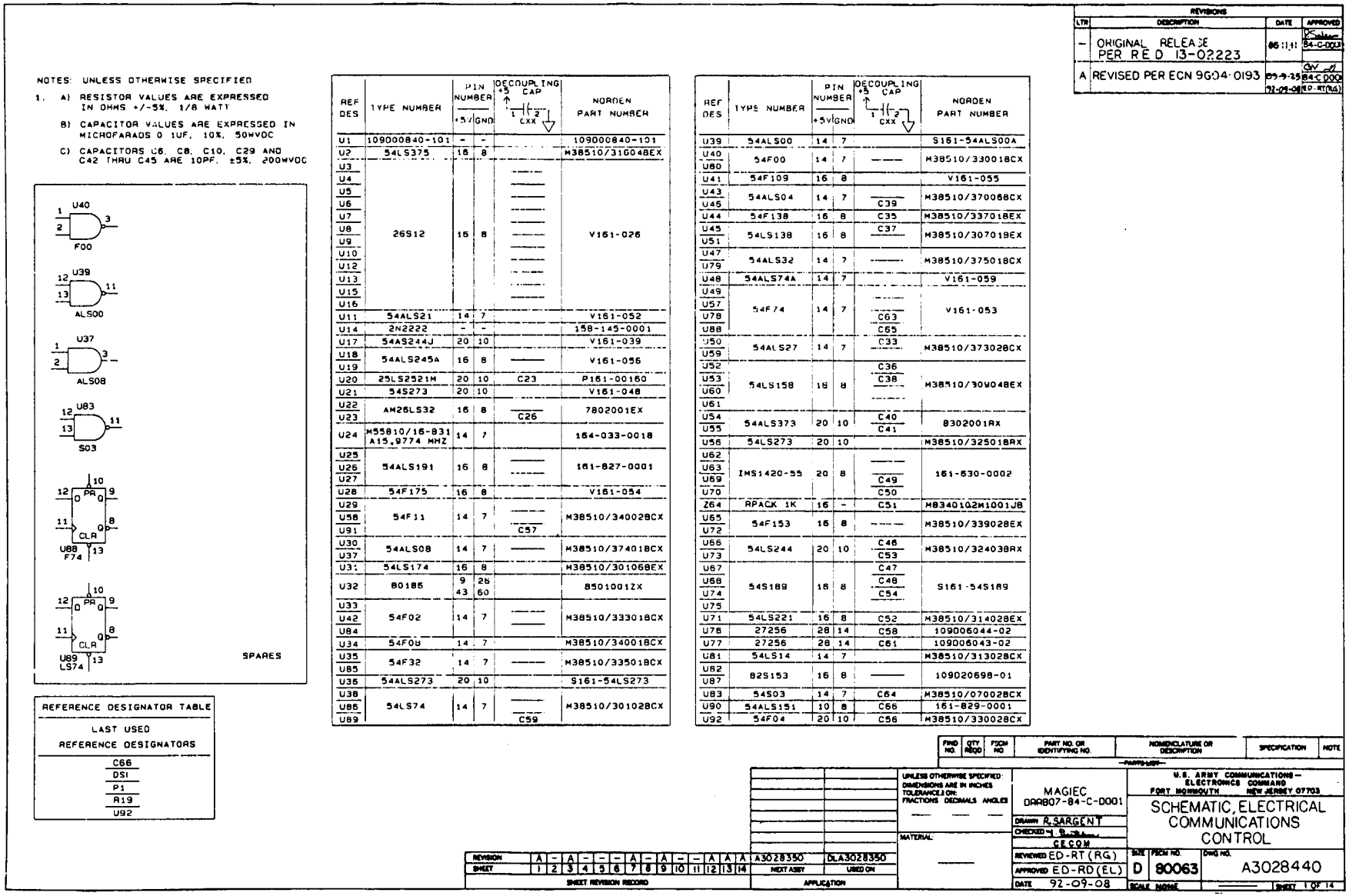
DATA PATH SCHEMATIC
(Sheet 12 of 14)



DATA PATH SCHEMATIC
(Sheet 13 of 14)

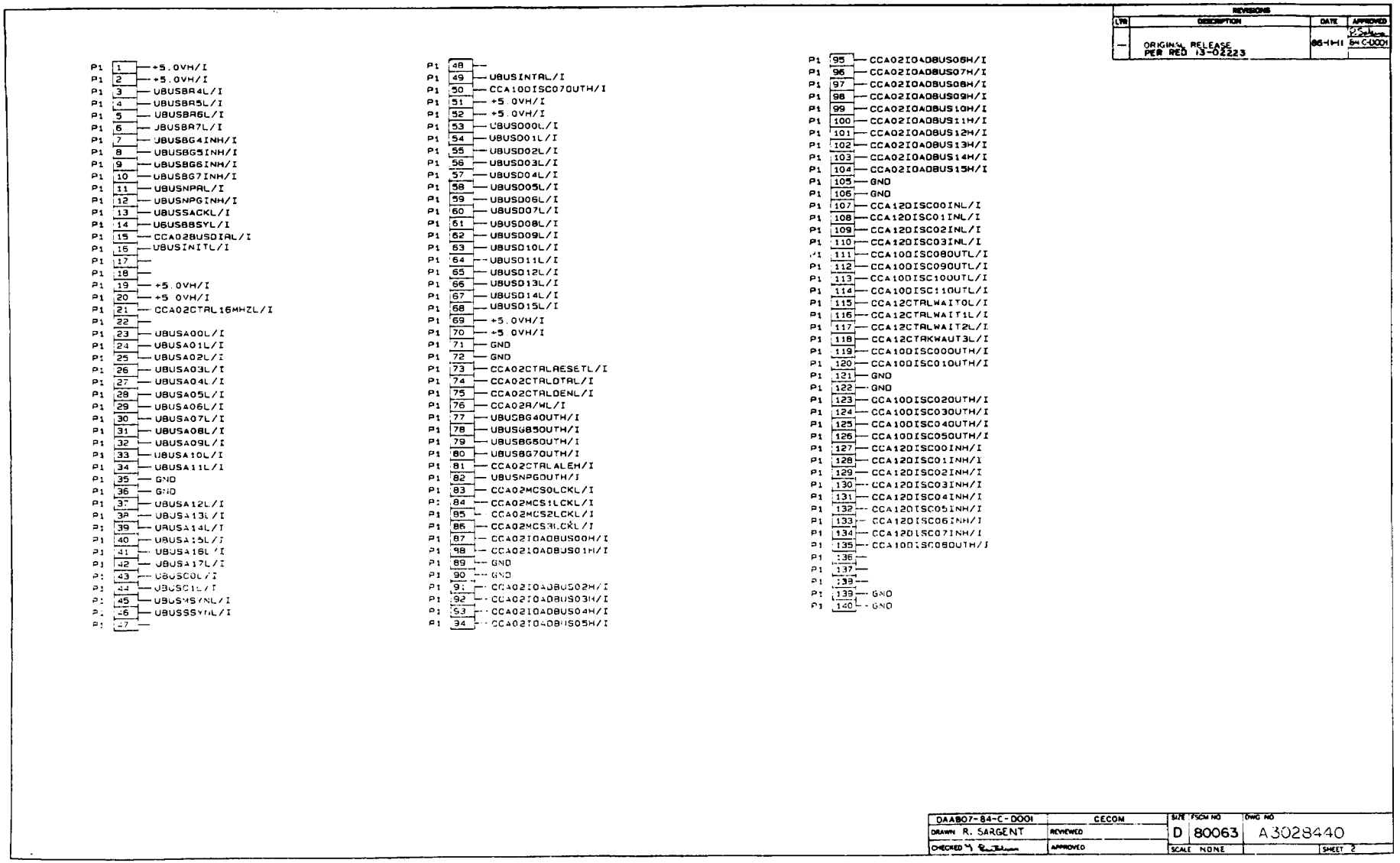


I-94 DATA PATH SCHEMATIC
(Sheet 14 of 14)



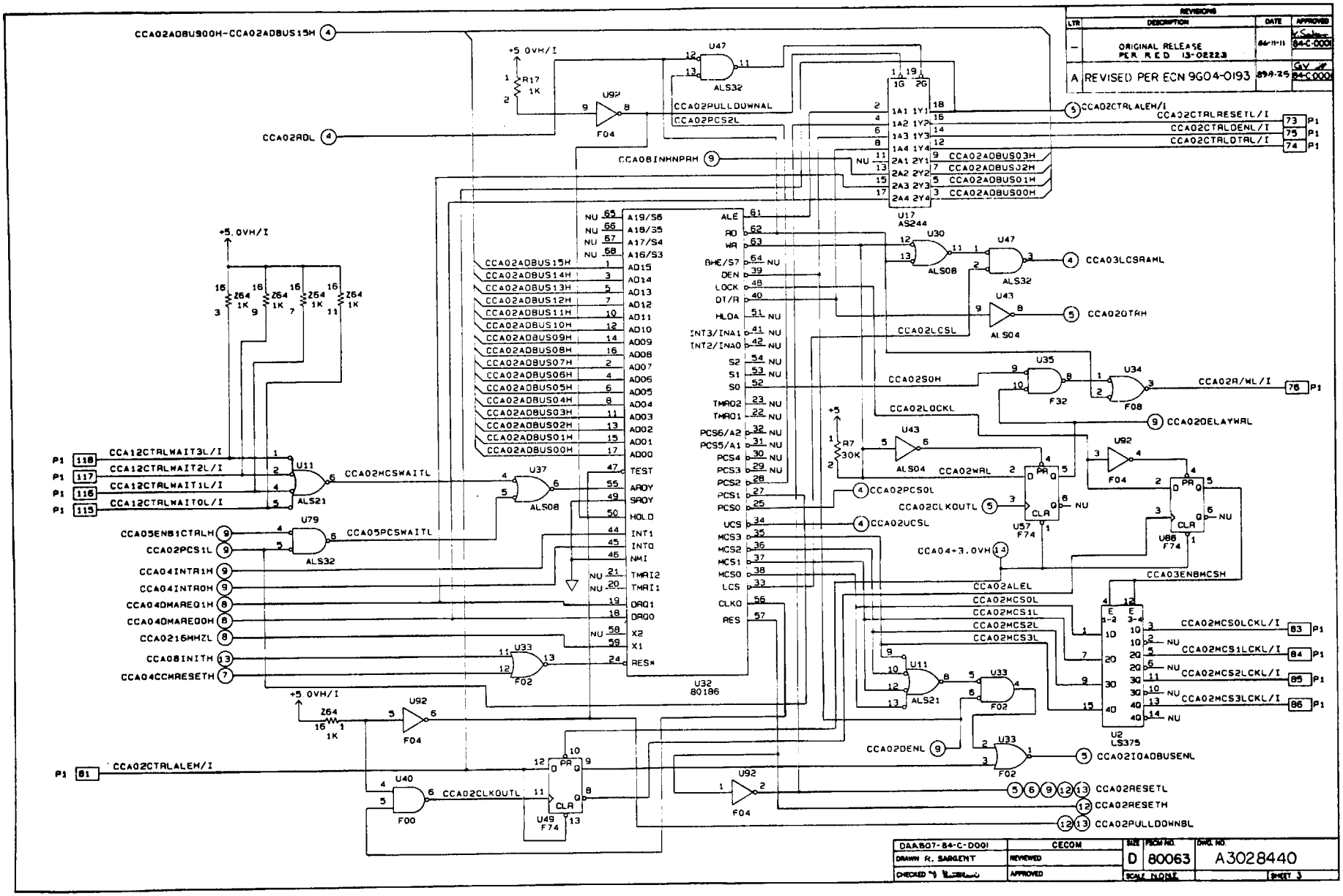
SMI SCHEMATIC

(Sheet 1 of 14)



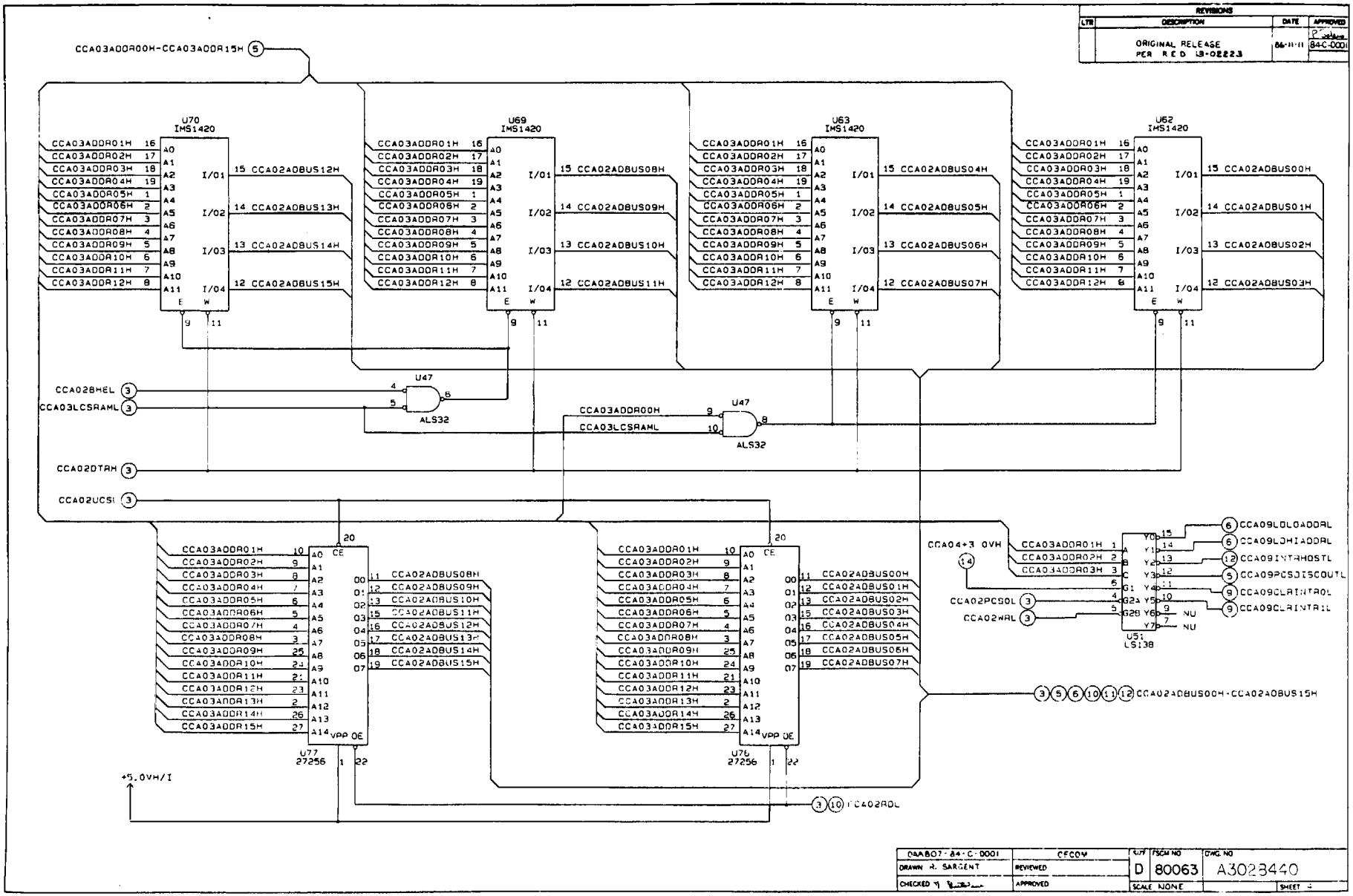
SMI SCHEMATIC

(Sheet 2 of 14)

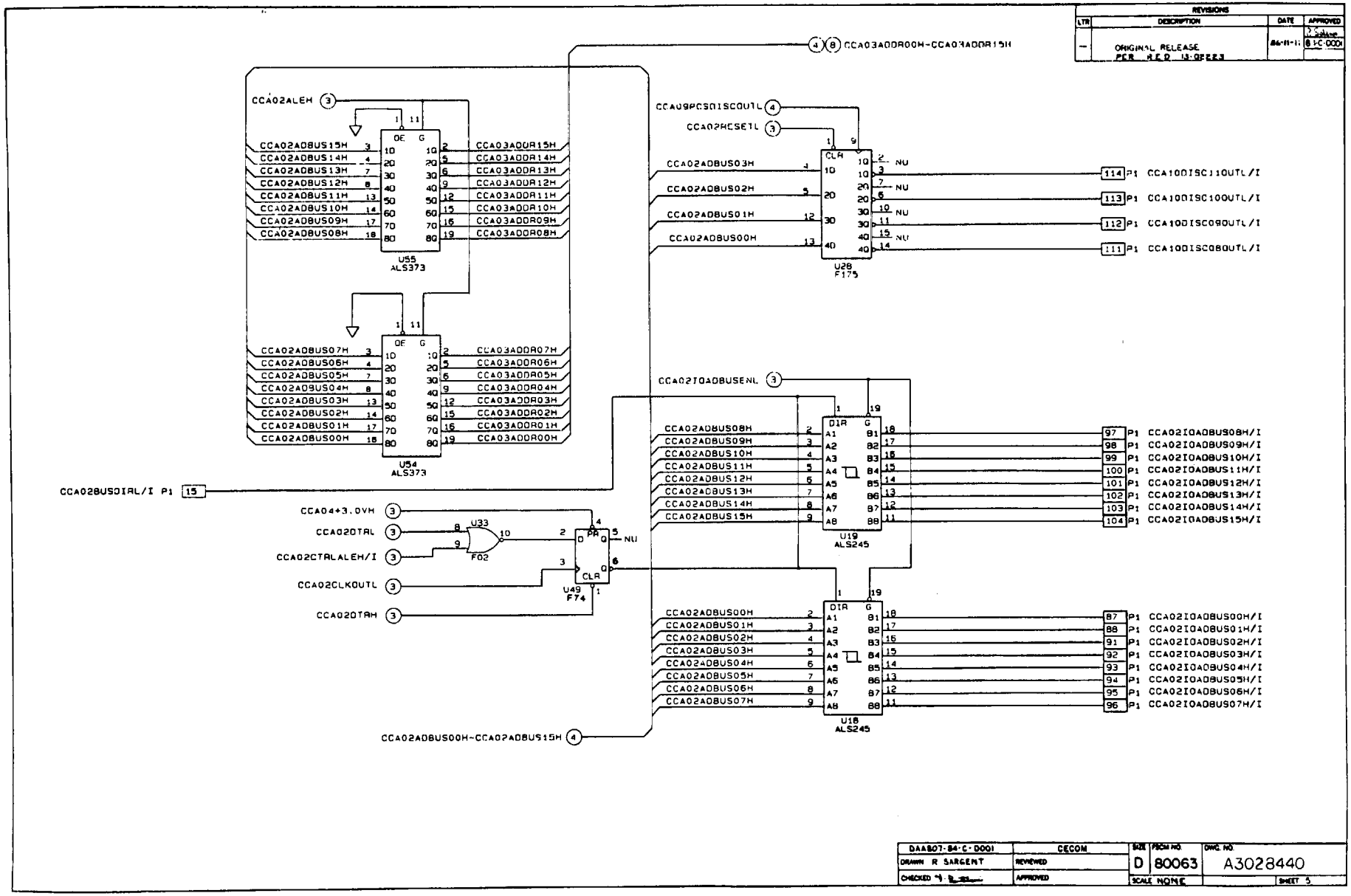


SMI SCHEMATIC T-97

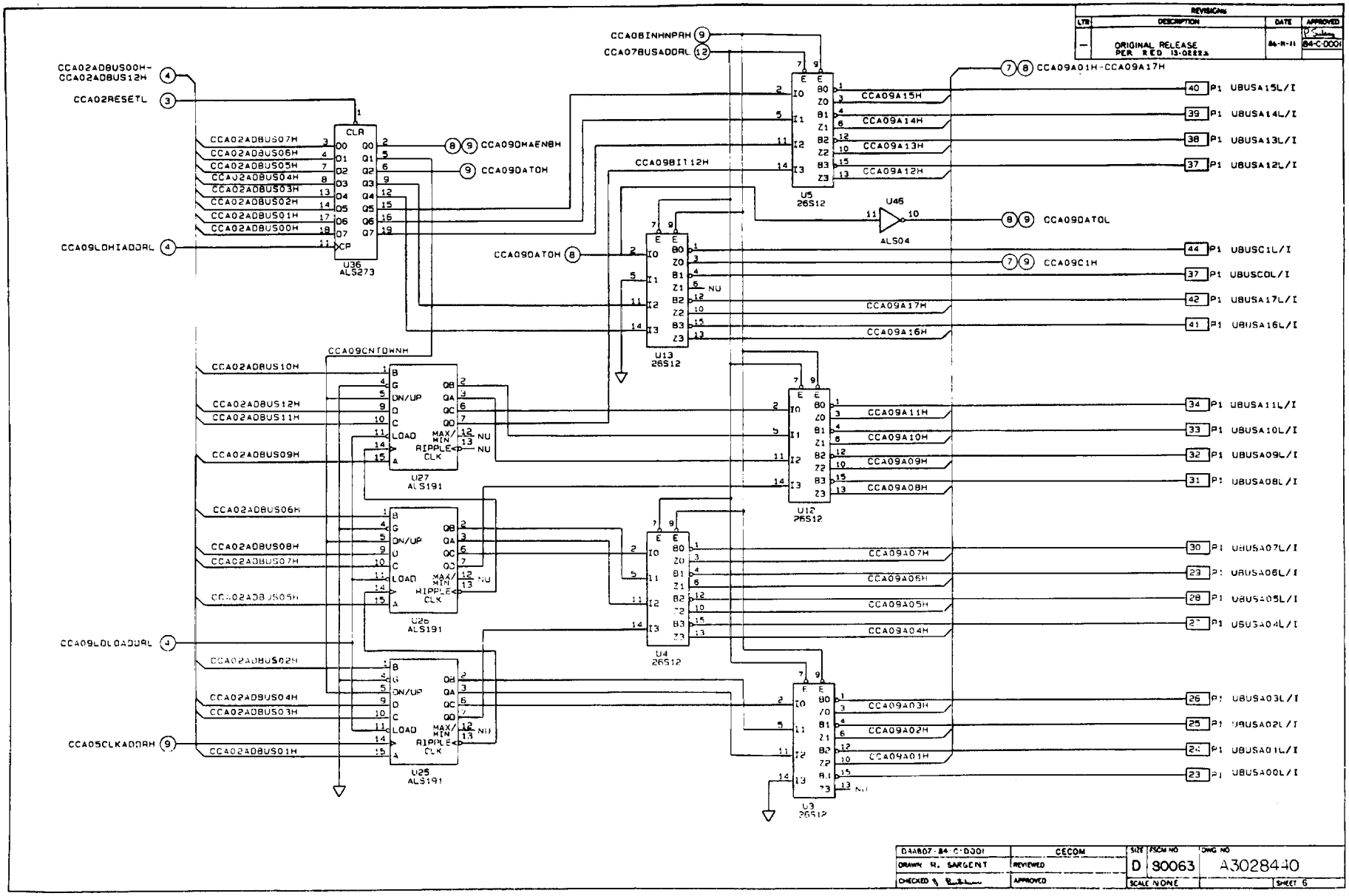
SMI SCHEMATIC
(Sheet 3 of 14)



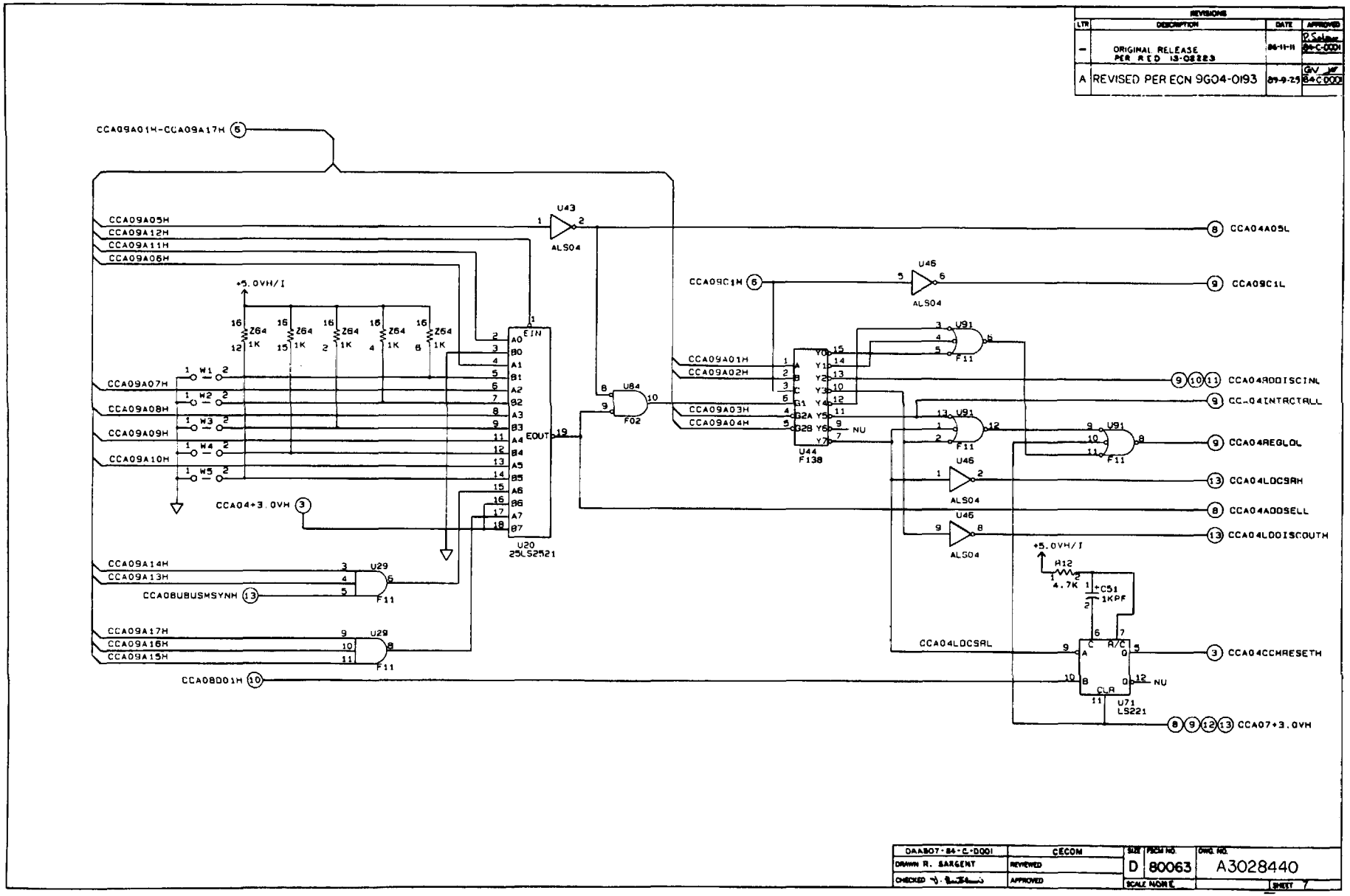
SMI SCHEMATIC
(Sheet 4 of 14)



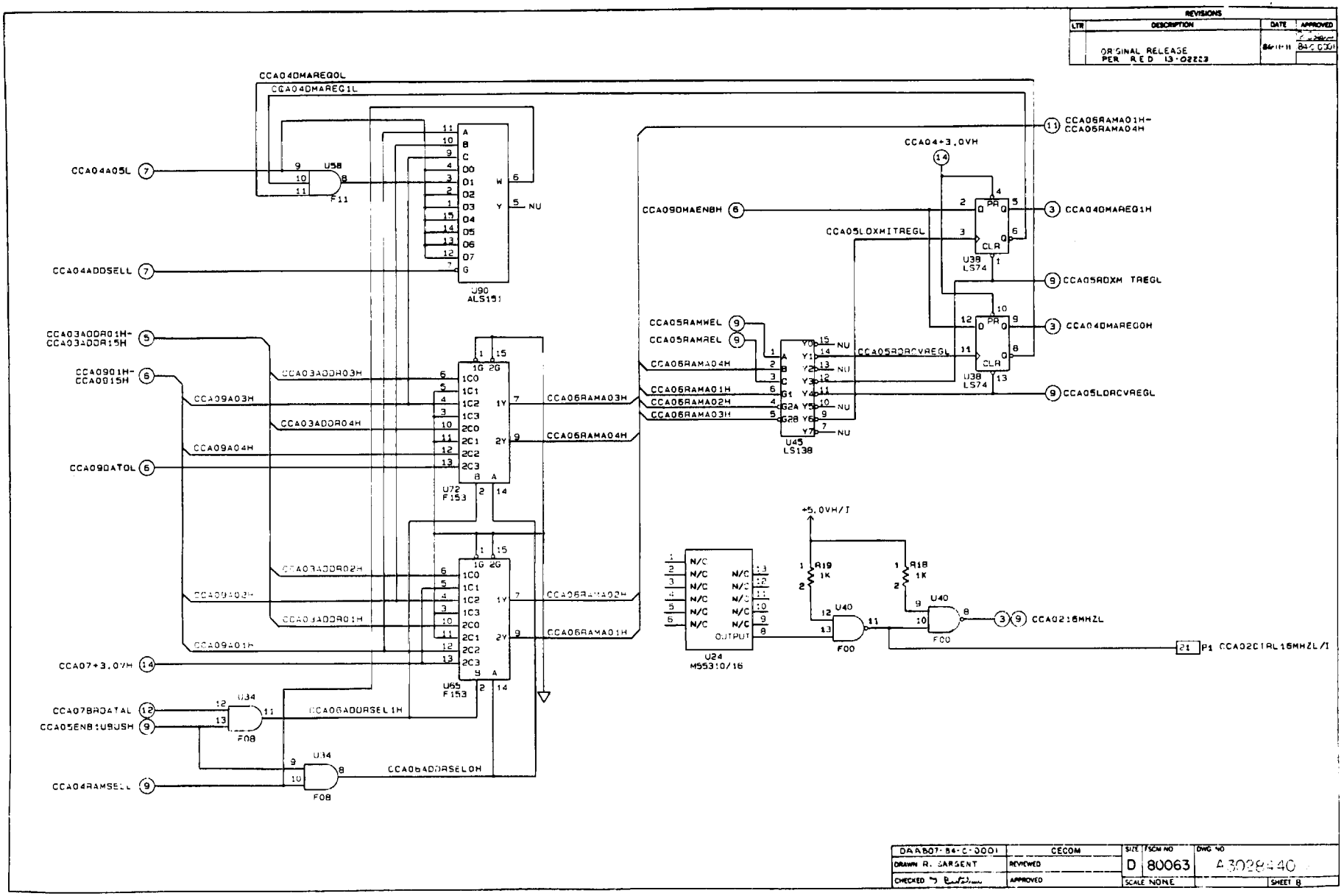
SMI SCHEMATIC
(Sheet 5 of 14)



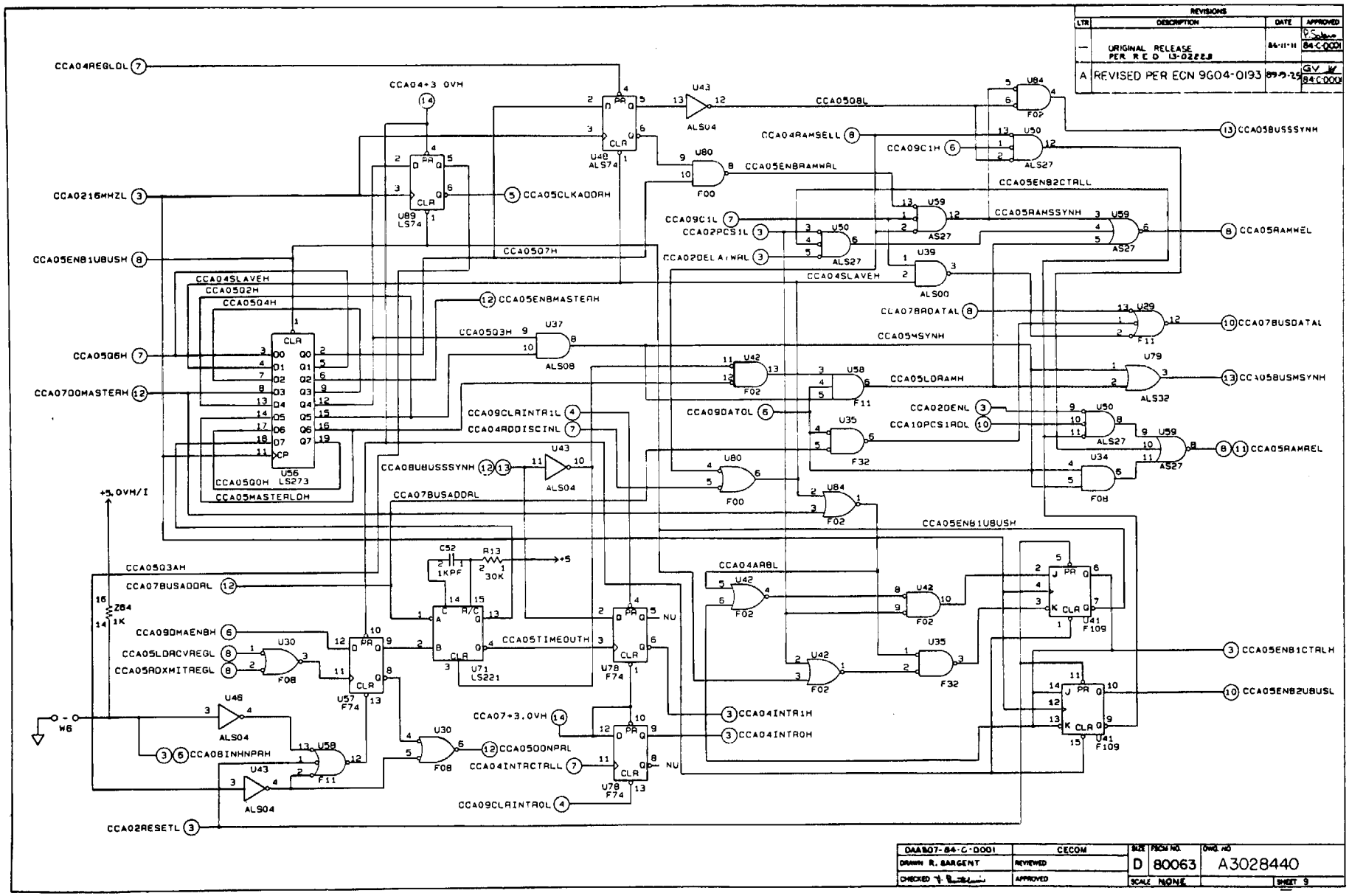
SMI SCHEMATIC
(Sheet 6 of 14)
I-100



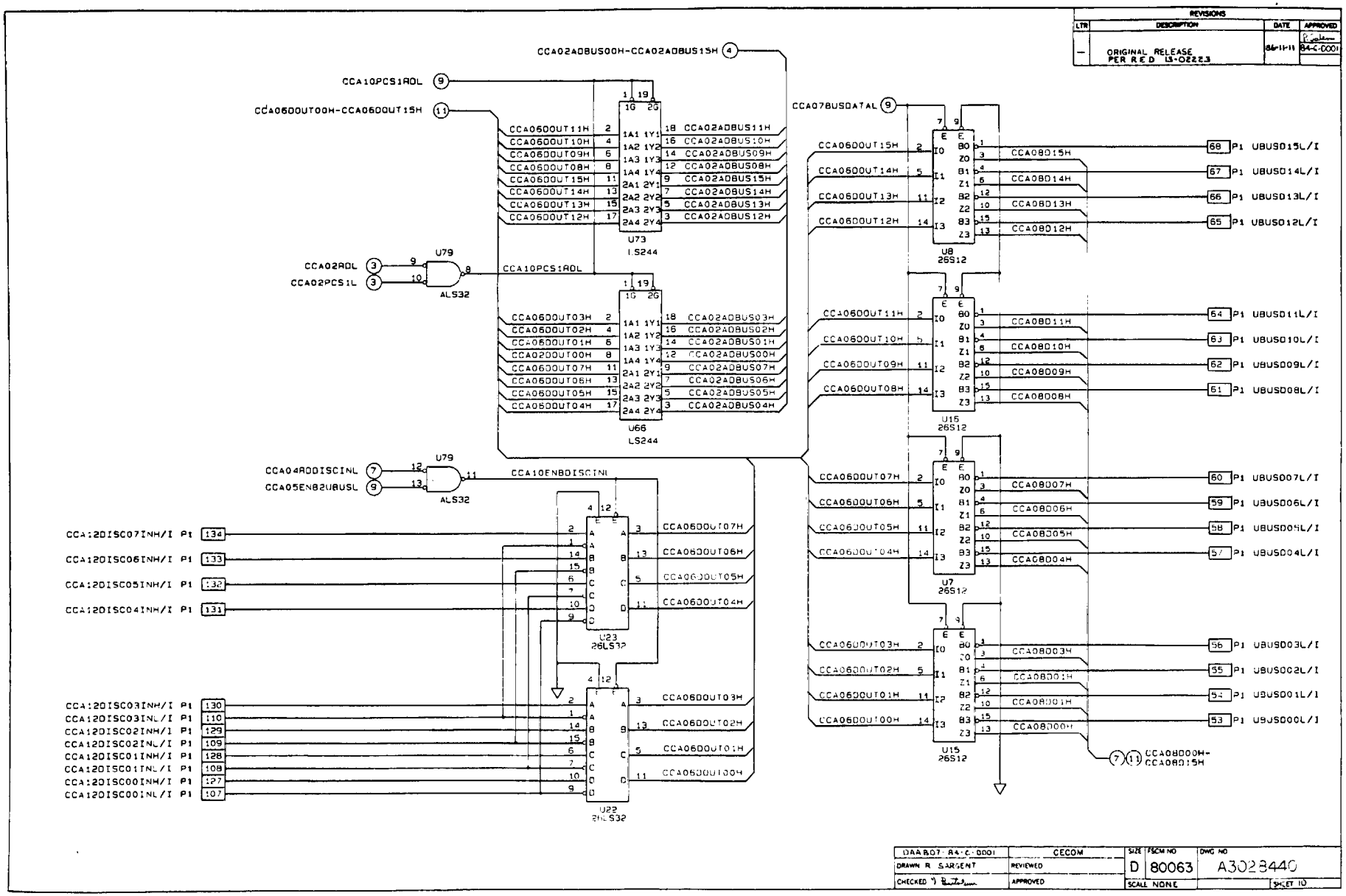
SMI SCHEMATIC
(Sheet 7 of 14)



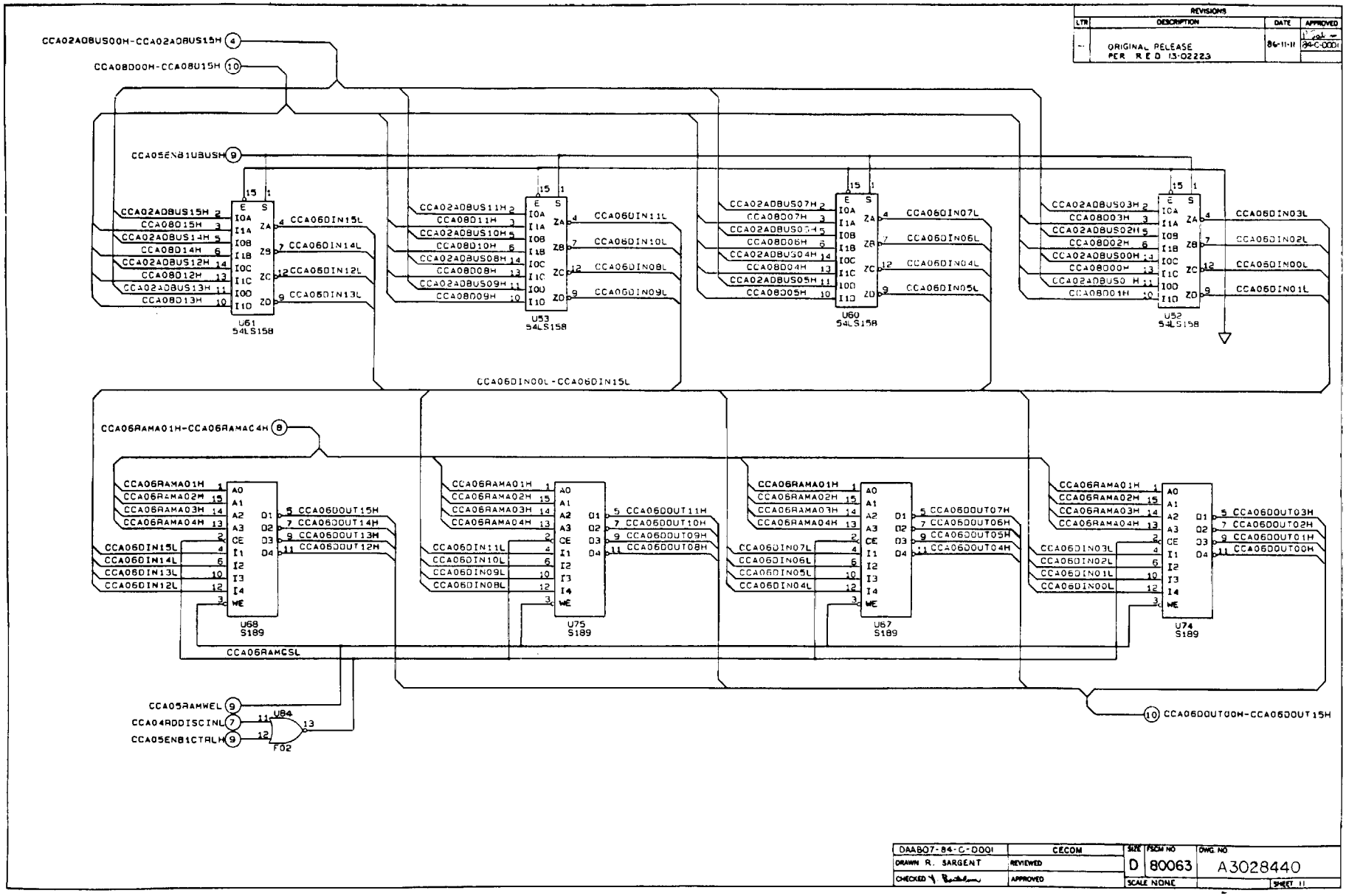
SMI SCHEMATIC
(Sheet 8 of 14)
I-102



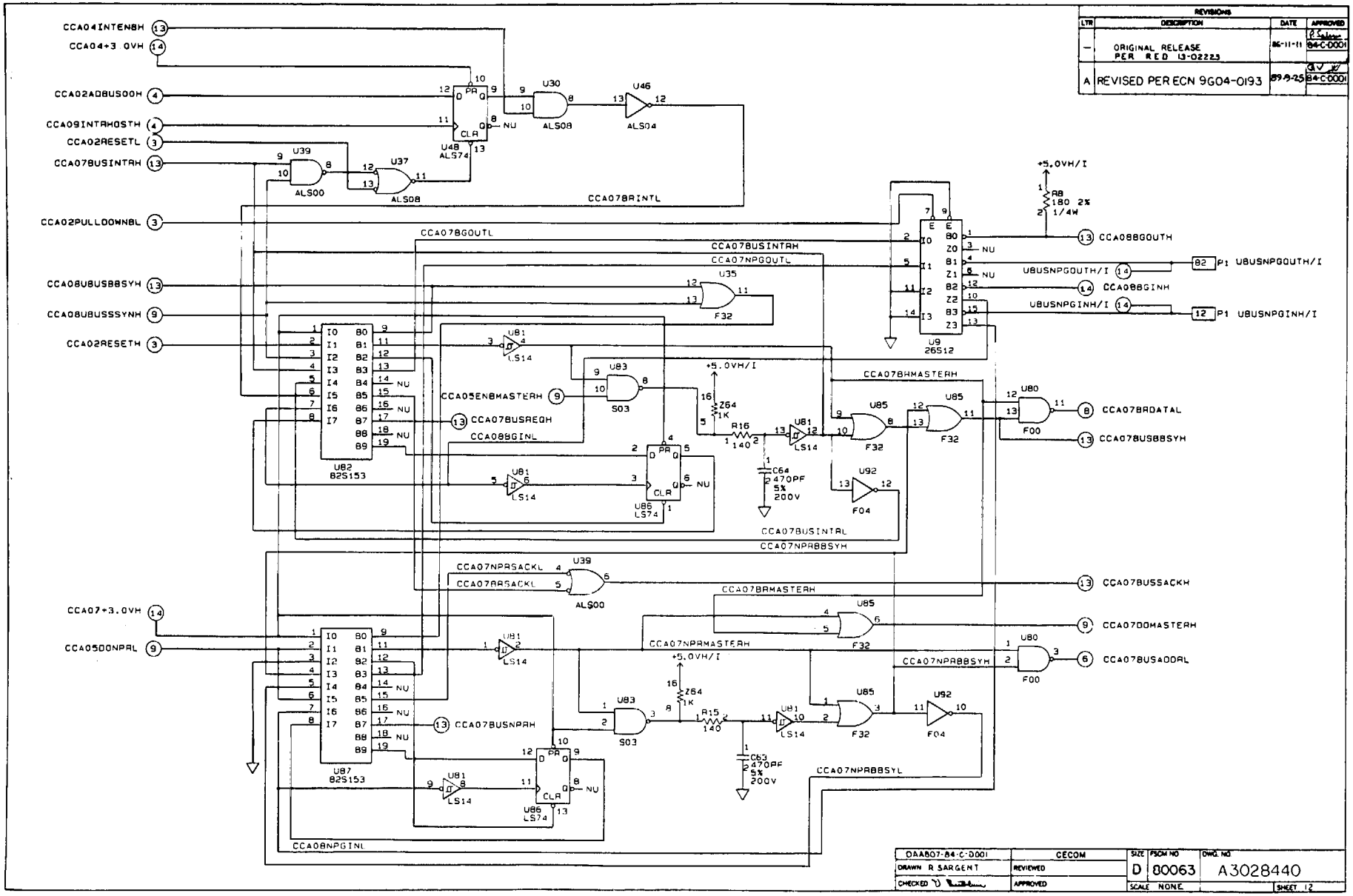
SMI SCHEMATIC
(Sheet 9 of 14)



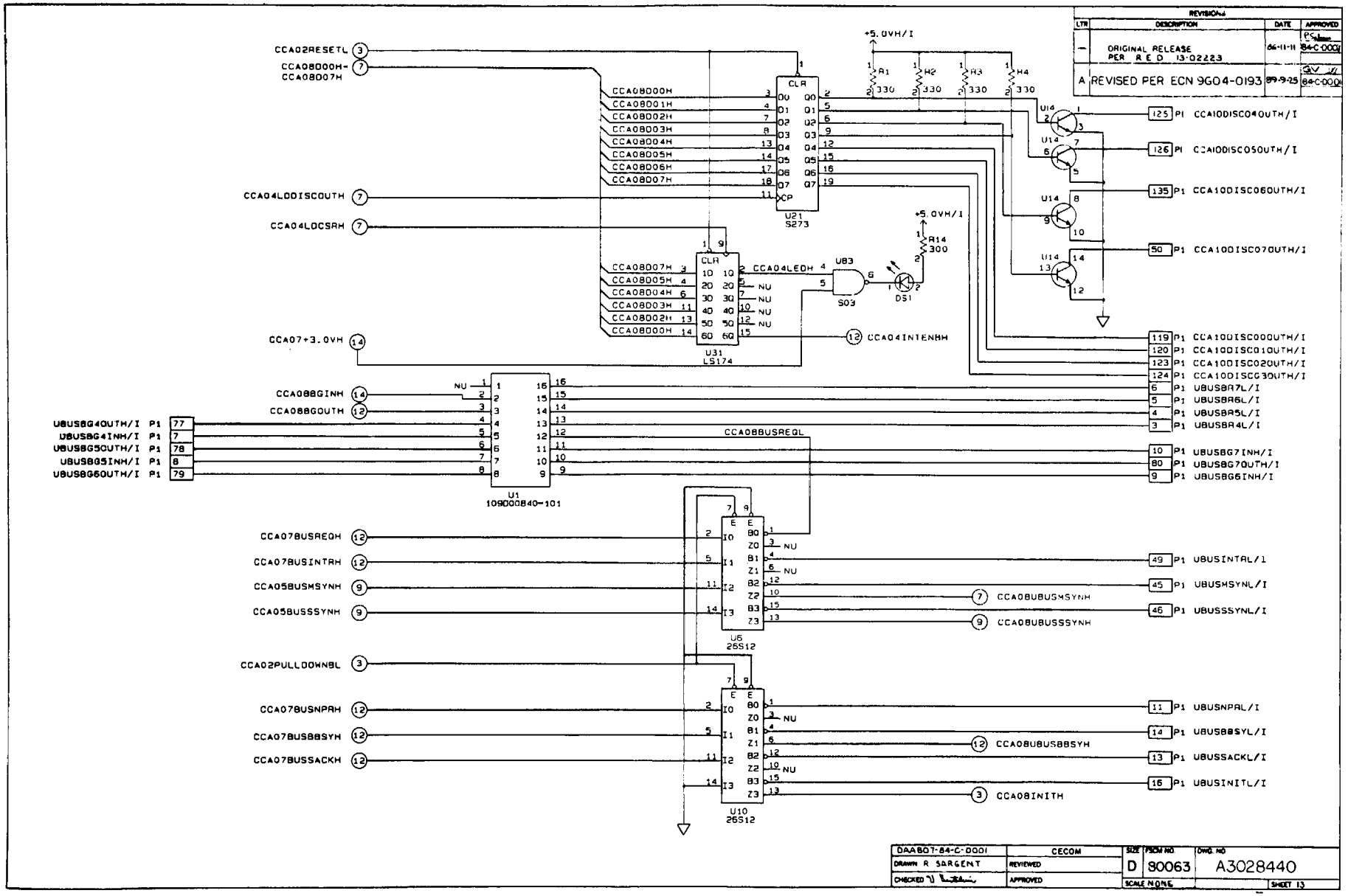
SMI SCHEMATIC
(Sheet 10 of 14)



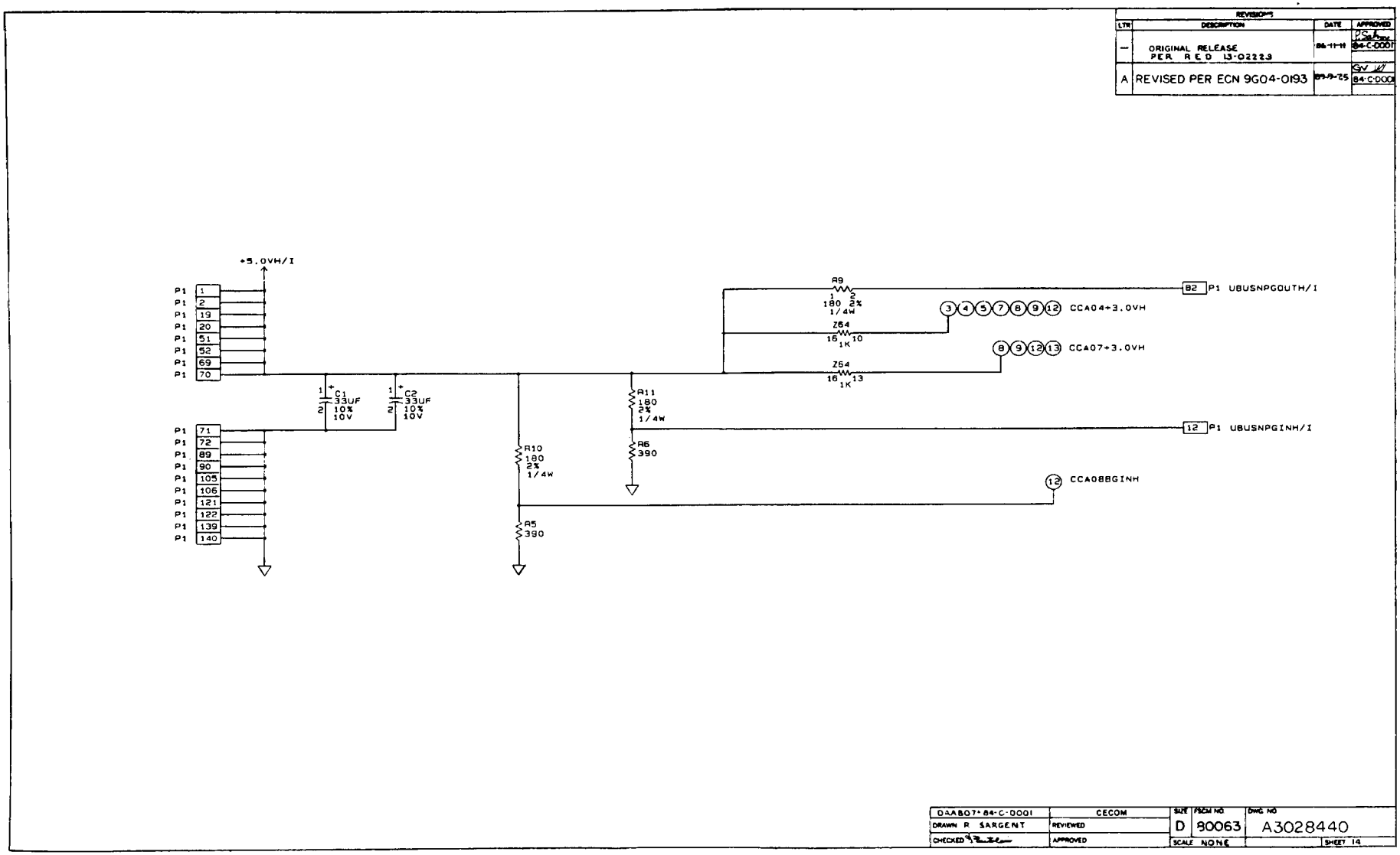
SMI SCHEMATIC
(Sheet 11 of 14)
I-105



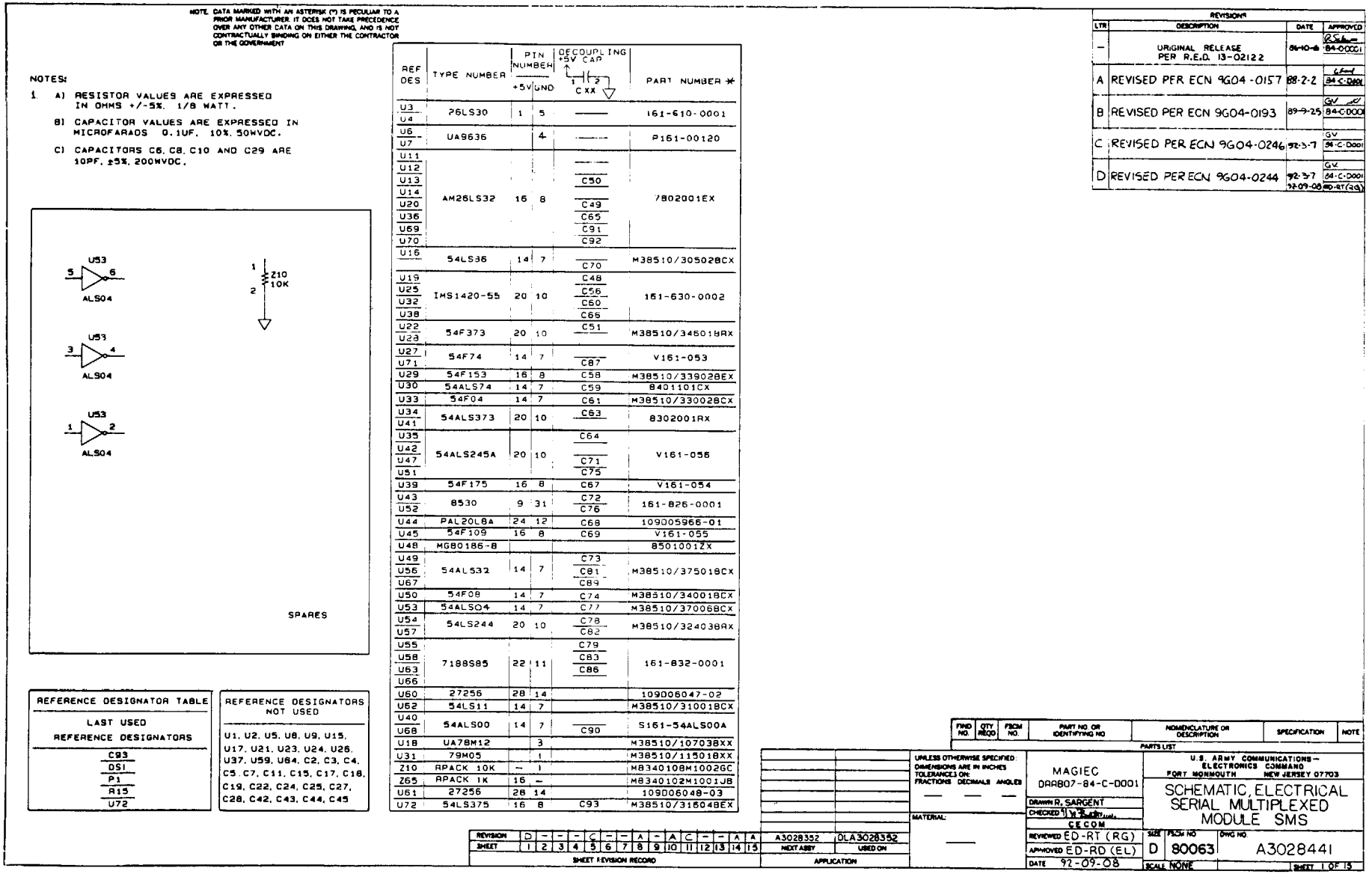
SMI SCHEMATIC
(Sheet 12 of 14)



SMI SCHEMATIC
(Sheet 13 of 14)
I-107



SMI SCHEMATIC
(Sheet 14 of 14)



NOTE: DATA MARKED WITH AN ASTERISK (*) IS PECULIAR TO A PRIOR MANUFACTURER IT DOES NOT TAKE PRECEDENCE OVER ANY OTHER DATA ON THIS DRAWING, AND IS NOT CONTRACTUALLY BINDING ON EITHER THE CONTRACTOR OR THE GOVERNMENT

NOTES:

1. A) RESISTOR VALUES ARE EXPRESSED IN OHMS +/-5%. 1/8 WATT.
   B) CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS 0.1UF. 10%. 50WVDC.
   C) CAPACITORS C6, C8, C10 AND C29 ARE 10PF, ±5%, 200WVDC.

U53 ALS04 (5, 6)
U53 ALS04 (3, 4)
U53 ALS04 (1, 2)
Z10 10K (1, 2)
SPARES

REFDES	TYPE NUMBER	PIN NUMBER +5V	PIN NUMBER GND	DECOUPLING +5V CAP C XX	PART NUMBER *
U3	26LS30	1	5	——	161-610-0001
U4					
U6	UA9636		4	——	P161-00120
U7					
U11				——	
U12				——	
U13				C50	
U14	AM26LS32	16	8	——	7802001EX
U20				C49	
U36				C65	
U69				C91	
U70				C92	
U16	54LS36	14	7	——	M38510/30502BCX
				C70	
U19				C48	
U25	IMS1420-55	20	10	C56	161-630-0002
U32				C60	
U38				C66	
U22	54F373	20	10	C51	M38510/34601BRX
U28					
U27	54F74	14	7	——	V161-053
U71				C87	
U29	54F153	16	8	C58	M38510/33902BEX
U30	54ALS74	14	7	C59	8401101CX
U33	54F04	14	7	C61	M38510/33002BCX
U34	54ALS373	20	10	C63	8302001RX
U41					
U35				C64	
U42	54ALS245A	20	10	——	V161-056
U47				C71	
U51				C75	
U39	54F175	16	8	C67	V161-054
U43	8530	9	31	C72	161-826-0001
U52				C76	
U44	PAL20L8A	24	12	C68	109005966-01
U45	54F109	16	8	C69	V161-055
U48	MG80186-8				8501001ZX
U49				C73	
U56	54ALS32	14	7	C81	M38510/37501BCX
U67				C89	
U50	54F08	14	7	C74	M38510/34001BCX
U53	54ALS04	14	7	C77	M38510/37006BCX
U54	54LS244	20	10	C78	M38510/32403BRX
U57				C82	
U55				C79	
U58	7188S85	22	11	C83	161-832-0001
U63				C86	
U66					
U60	27256	28	14		109006047-02
U62	54LS11	14	7		M38510/31001BCX
U40	54ALS00	14	7	C90	S161-54ALS00A
U68					
U18	UA78M12		3		M38510/10703BXX
U31	79M05		1		M38510/11501BXX
Z10	RPACK 10K	—	1		M8340108M1002GC
Z65	RPACK 1K	16	—		M8340102M1001JB
U61	27256	28	14		109D06048-03
U72	54LS375	16	8	C93	M38510/31504BEX

REFERENCE DESIGNATOR TABLE — LAST USED REFERENCE DESIGNATORS
C93
DSI
P1
R15
U72

REFERENCE DESIGNATORS NOT USED
U1, U2, U5, U8, U9, U15, U17, U21, U23, U24, U26, U37, U59, U64, C2, C3, C4, C5, C7, C11, C15, C17, C18, C19, C22, C24, C25, C27, C28, C42, C43, C44, C45

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
—	ORIGINAL RELEASE PER R.E.O. 13-02122	86-10-16	84-C-0001
A	REVISED PER ECN 9G04-0157	88-2-2	84-C-D001
B	REVISED PER ECN 9G04-0193	89-9-25	GV 84-C-D001
C	REVISED PER ECN 9G04-0246	92-3-7	GV 84-C-D001
D	REVISED PER ECN 9G04-0244	92-3-7 / 92-09-08	GV 84-C-D001 RD-RT (2d)

FIND NO.	QTY REQD	FSCM NO.	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	NOTE
PARTS LIST						

REVISION	D	-	-	-	C	-	-	A	-	A	C	-	-	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

SHEET REVISION RECORD

A3028352	DLA3028352
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS DECIMALS ANGLES — — —

MATERIAL: —

MAGIEC
DAA807-84-C-0001

DRAWN R. SARGENT
CHECKED
CECOM
REVIEWED ED-RT (RG)
APPROVED ED-RD (EL)
DATE 92-09-08

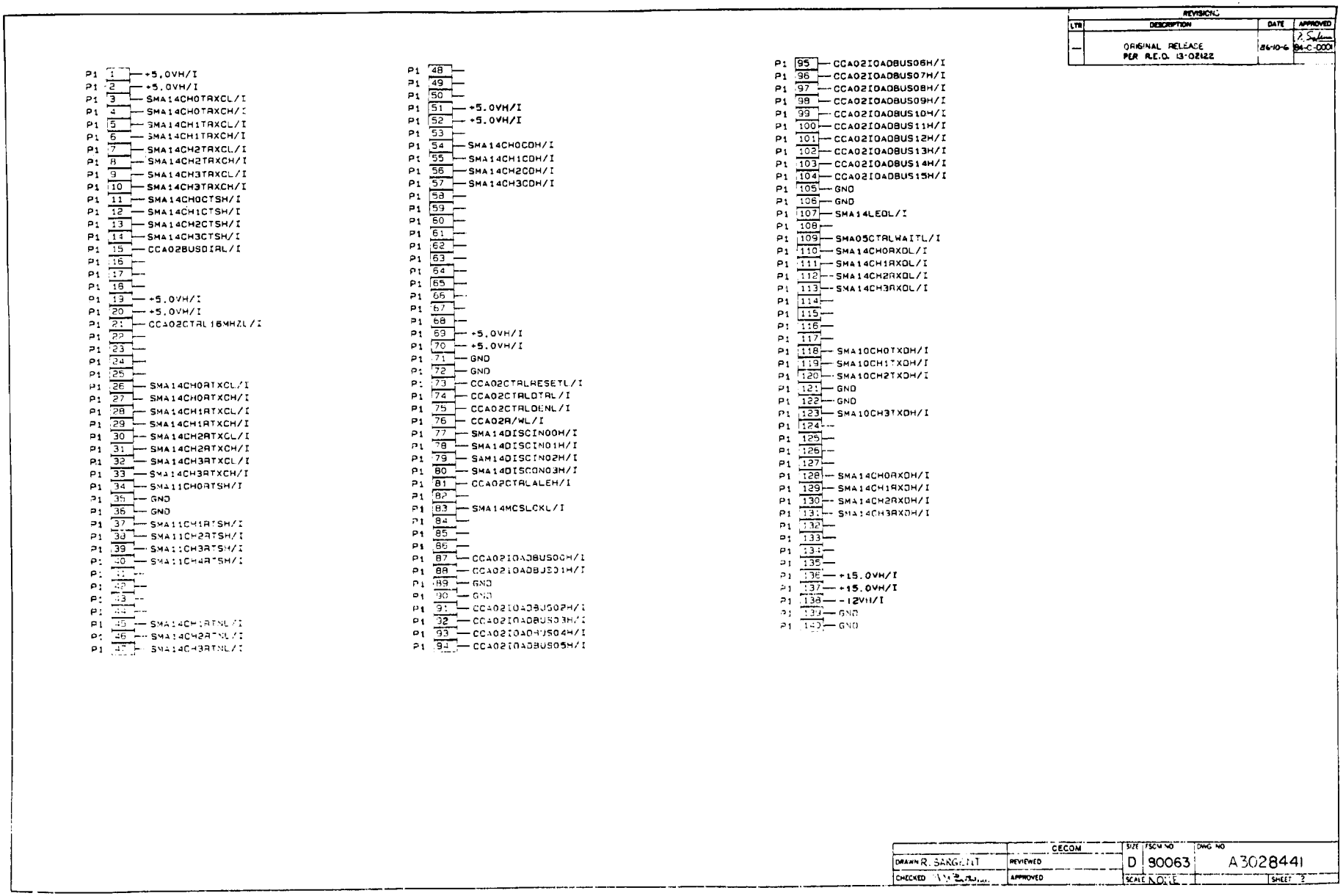
U.S. ARMY COMMUNICATIONS — ELECTRONICS COMMAND
FORT MONMOUTH NEW JERSEY 07703

SCHEMATIC, ELECTRICAL SERIAL MULTIPLEXED MODULE SMS

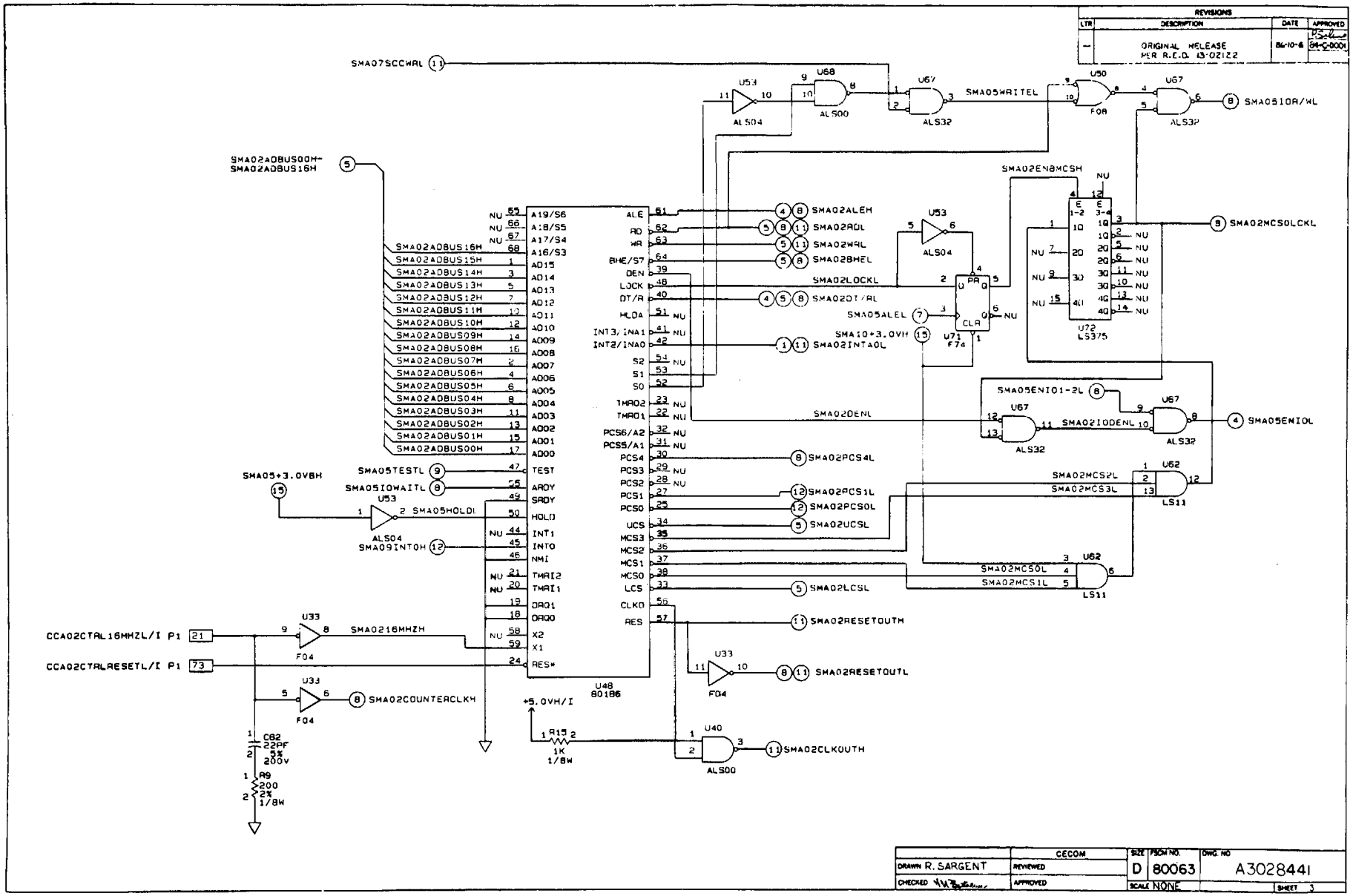
SIZE D | FSCM NO 80063 | DWG NO A3028441

SCALE NONE | SHEET 1 OF 15

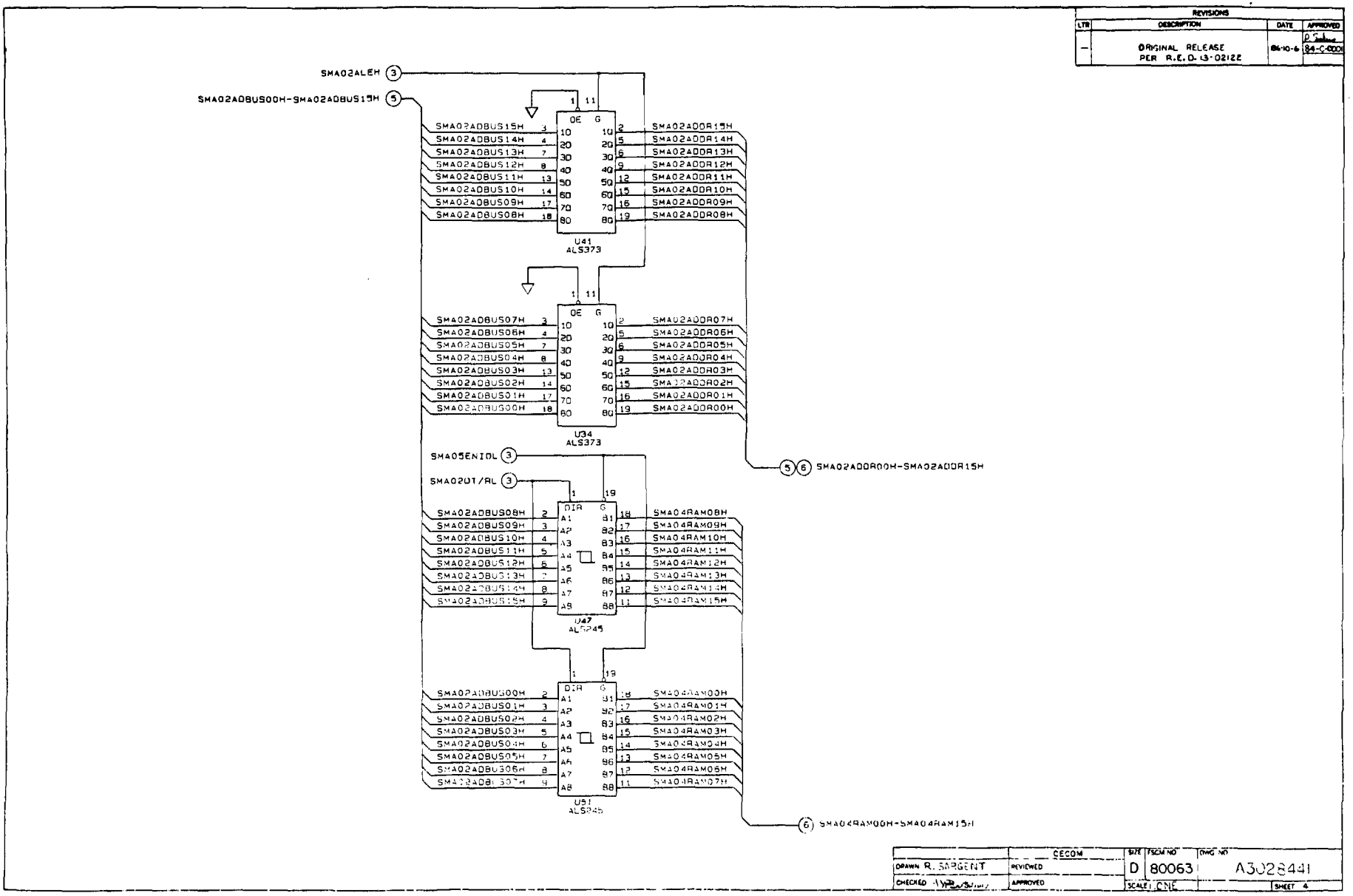
SHS SCHEMATIC
(Sheet 1 of 15)
I-109



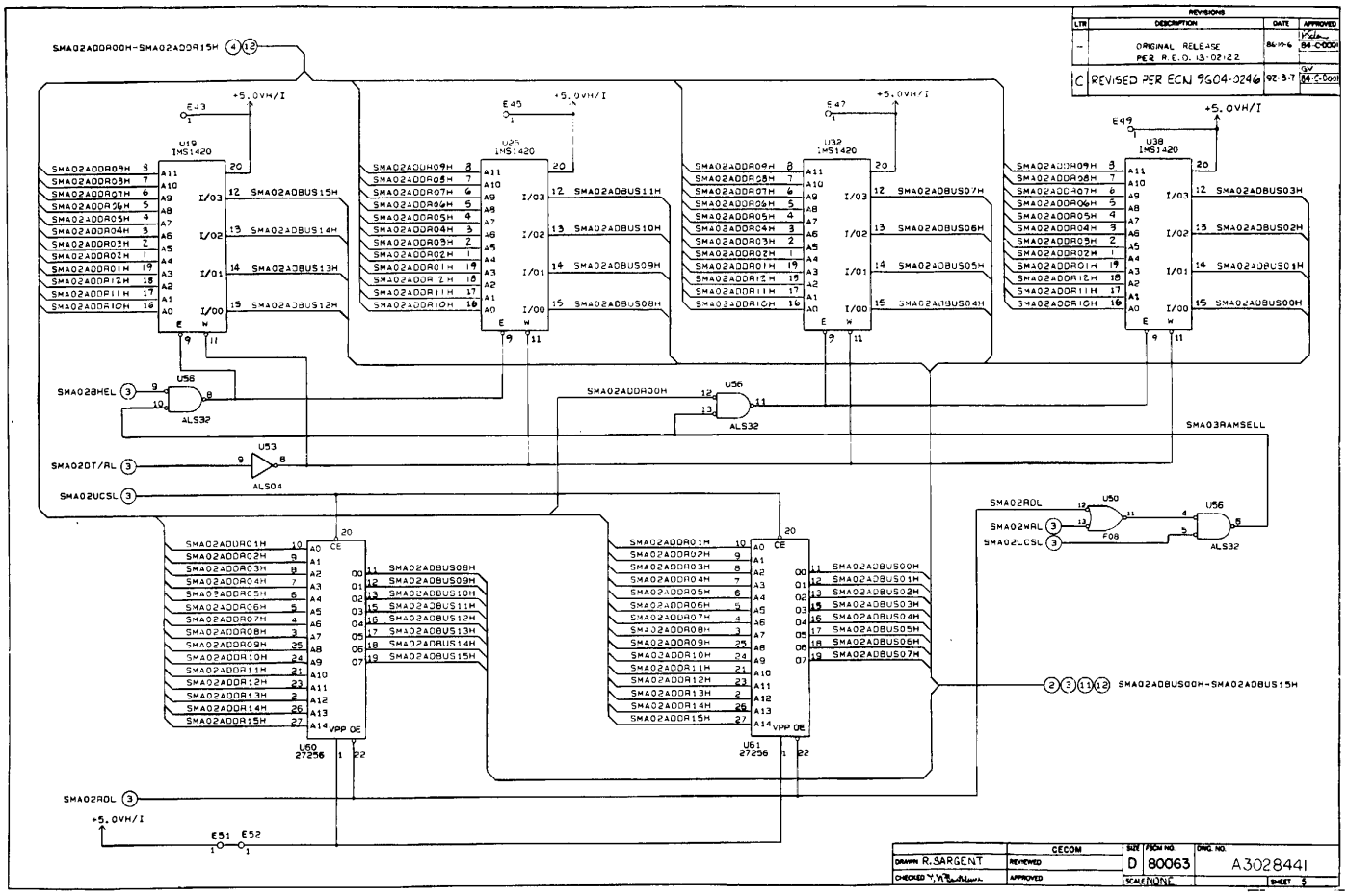
SMS SCHEMATIC
(Sheet 2 of 15)
I-110



SMS SCHEMATIC
(Sheet 3 of 15)
I-111

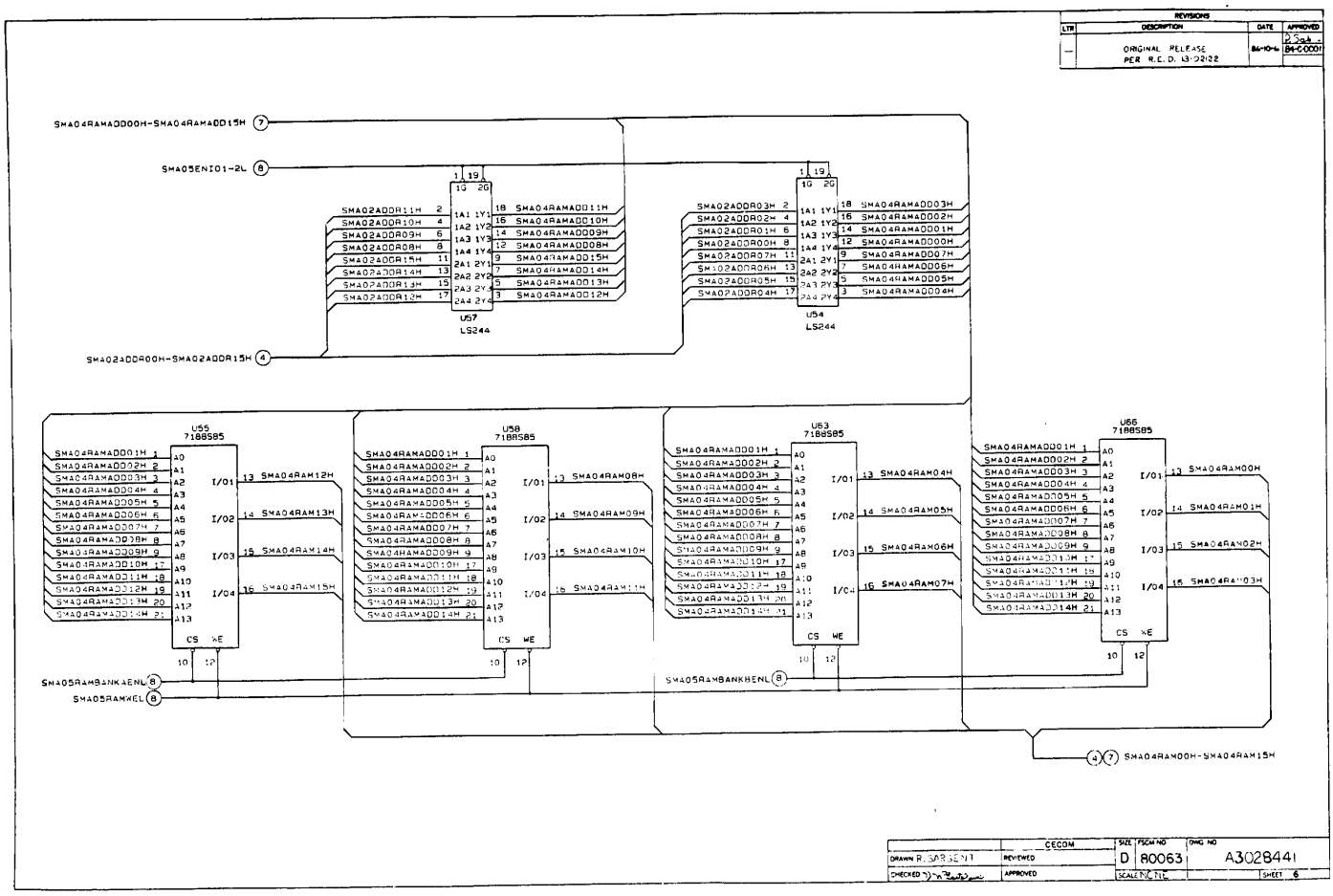


SMS SCHEMATIC
(Sheet 4 of 15)

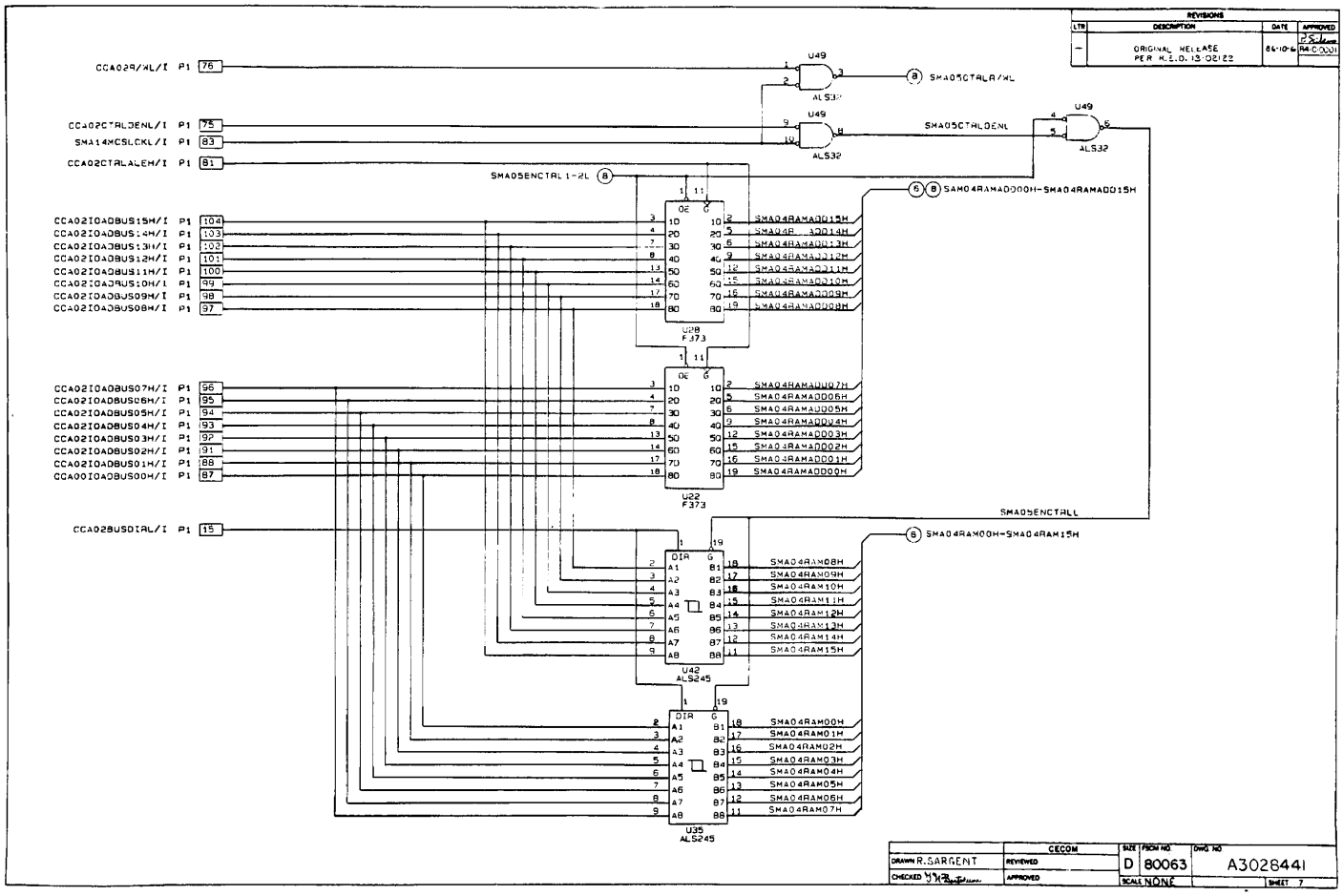


SMS SCHEMATIC

(Sheet 5 of 15)

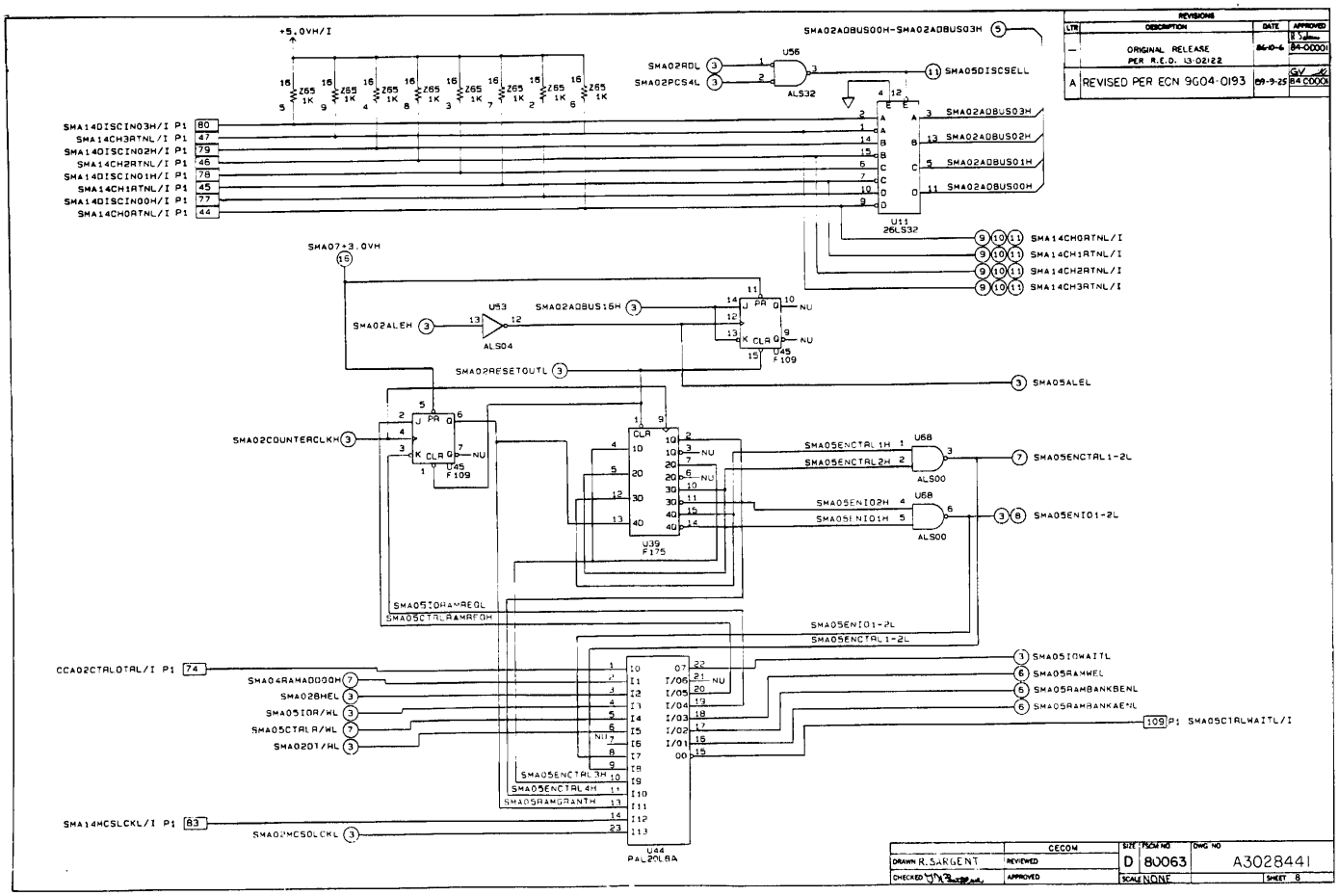


SMS SCHEMATIC
(Sheet 6 of 15)
I-114



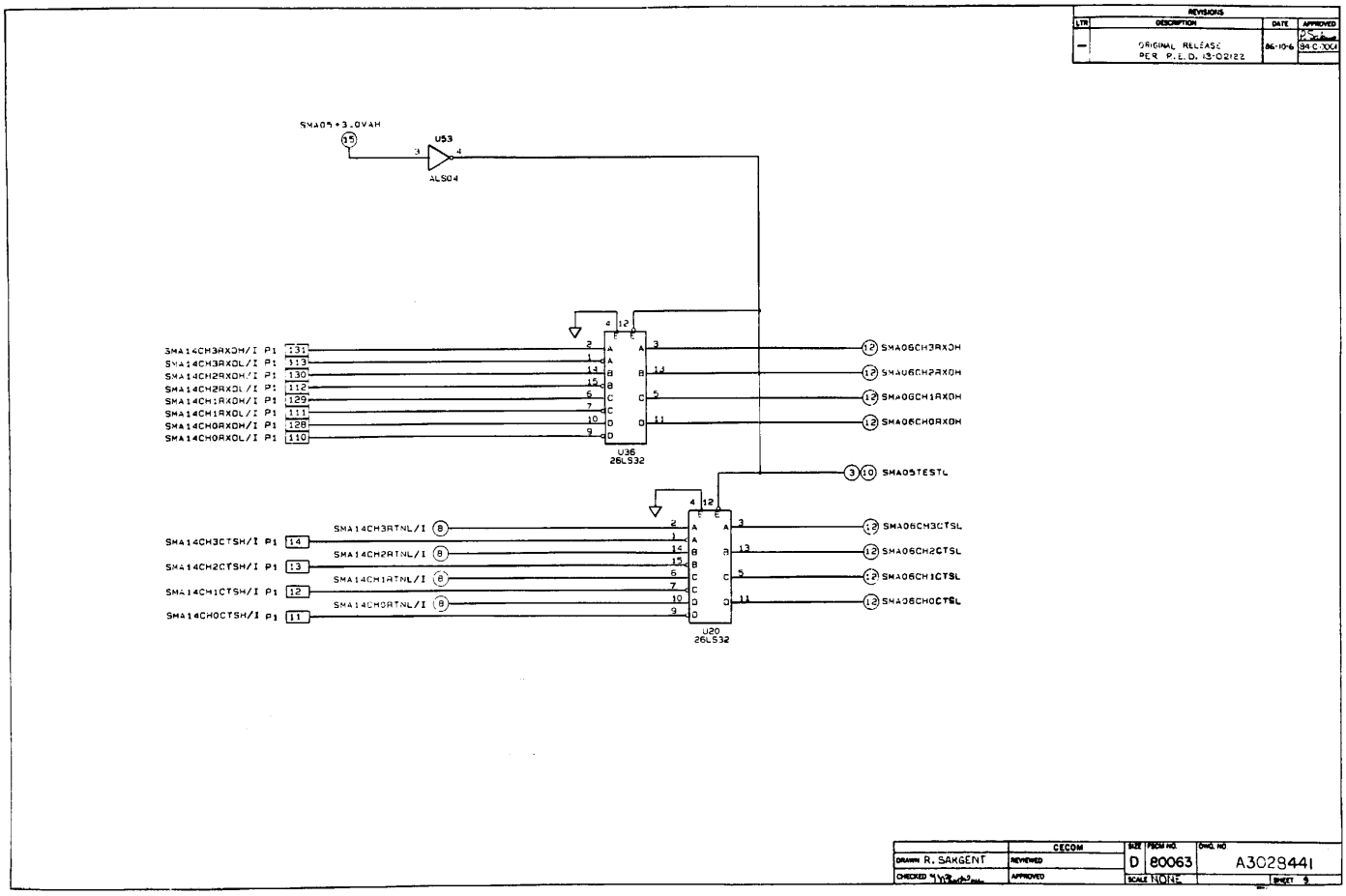
SMS SCHEMATIC

(Sheet 7 of 15)



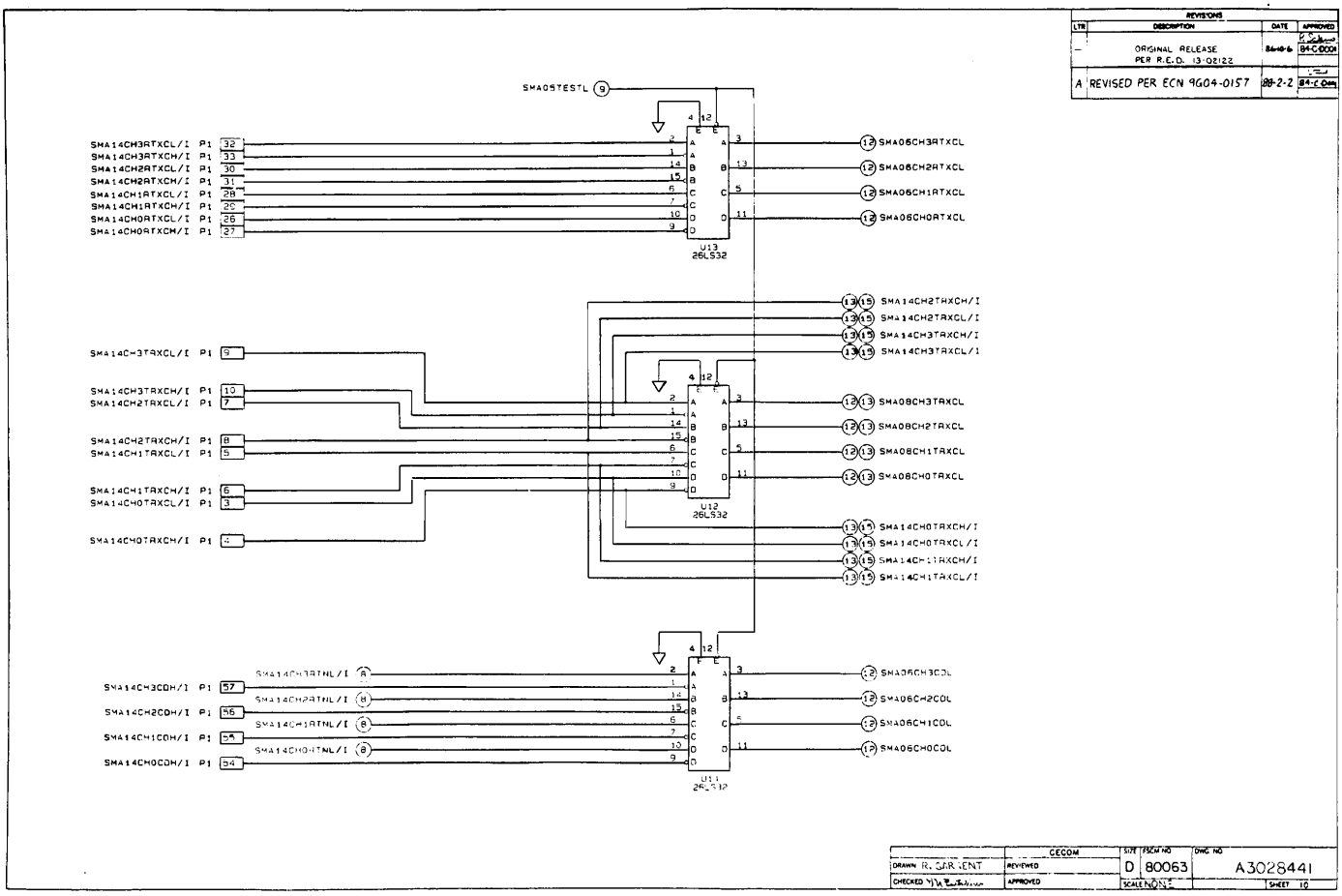
SMS SCHEMATIC

(Sheet 8 of 15)



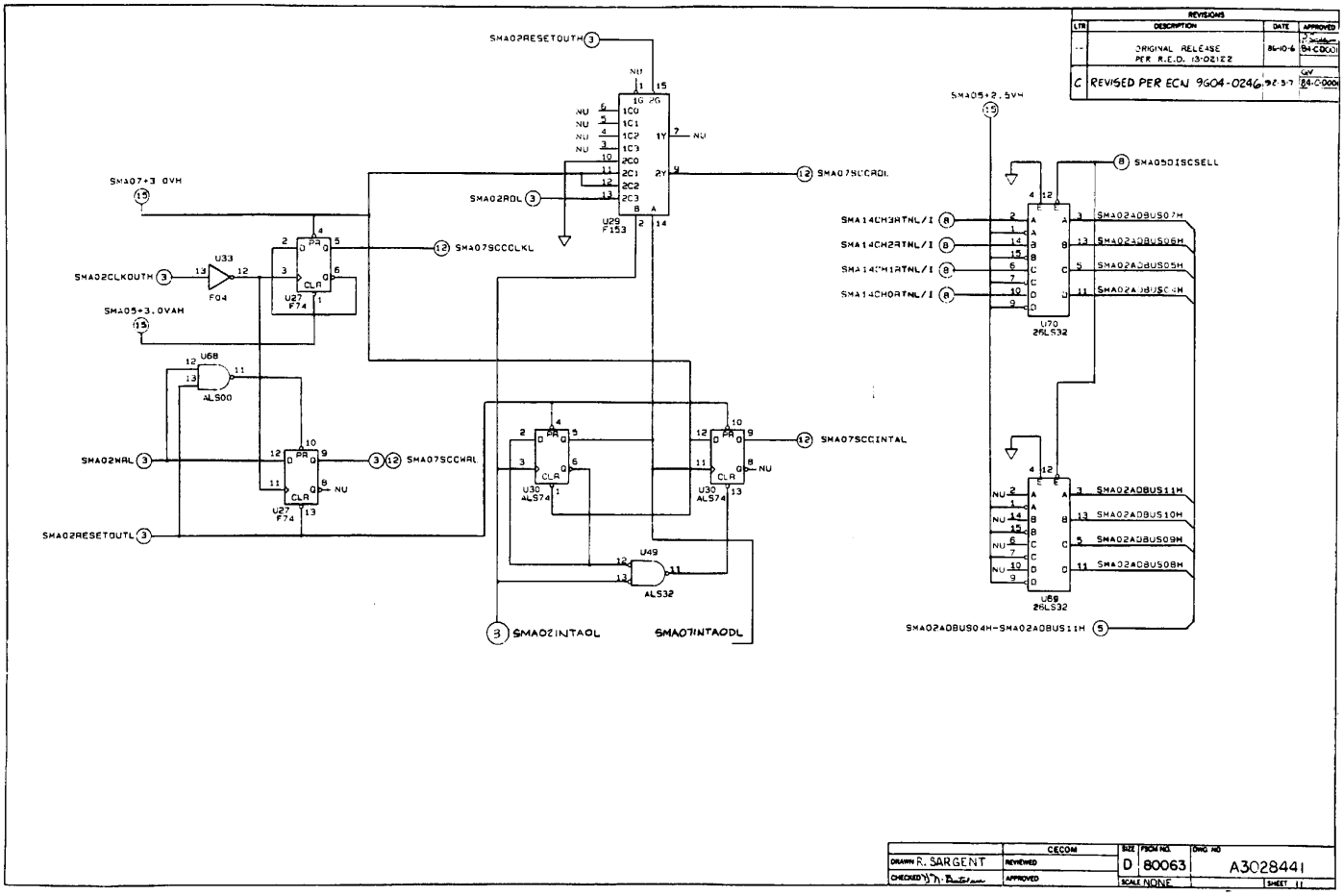
SMS SCHEMATIC

(Sheet 9 of 15)
I-117



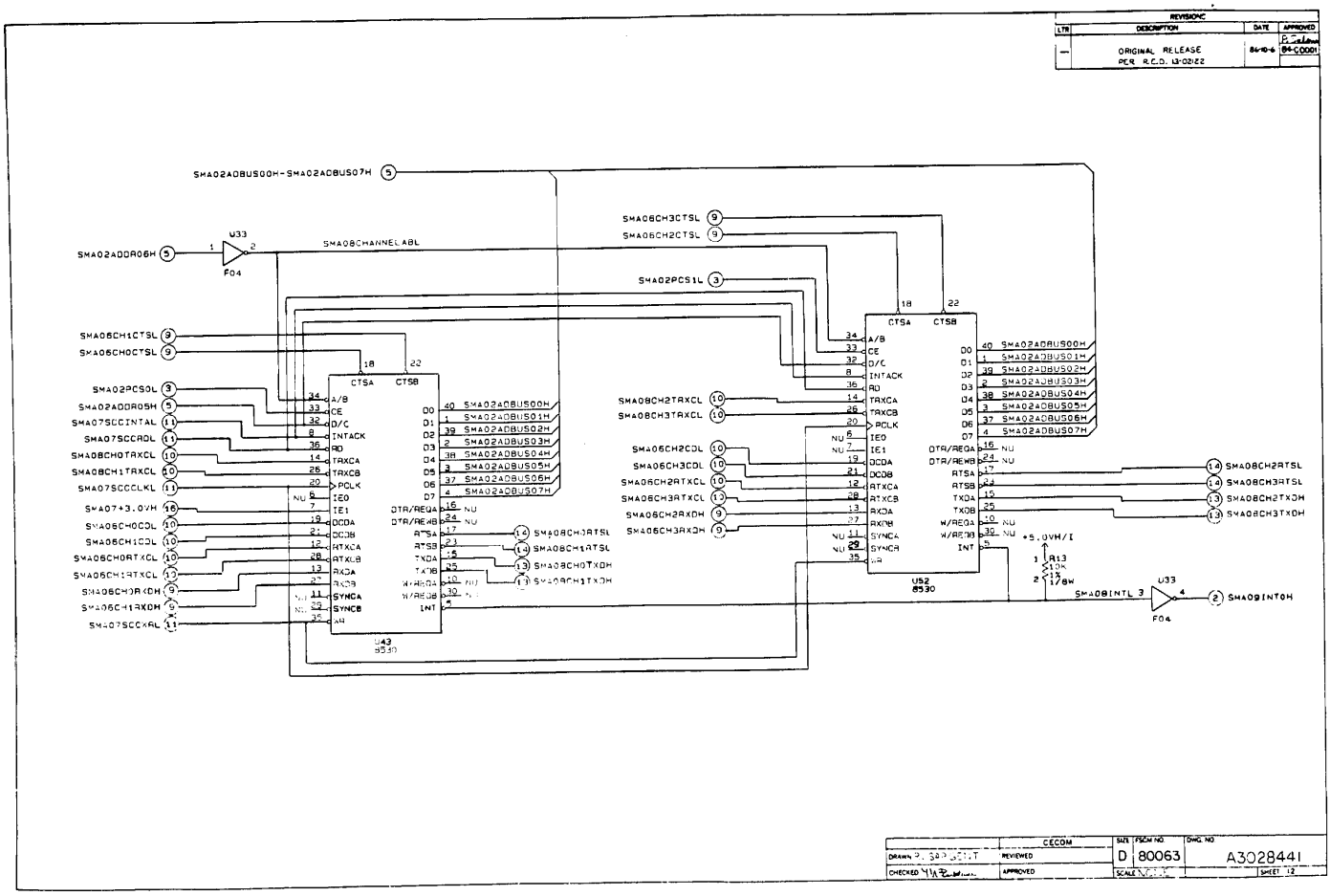
SMS SCHEMATIC

(Sheet 10 of 15)



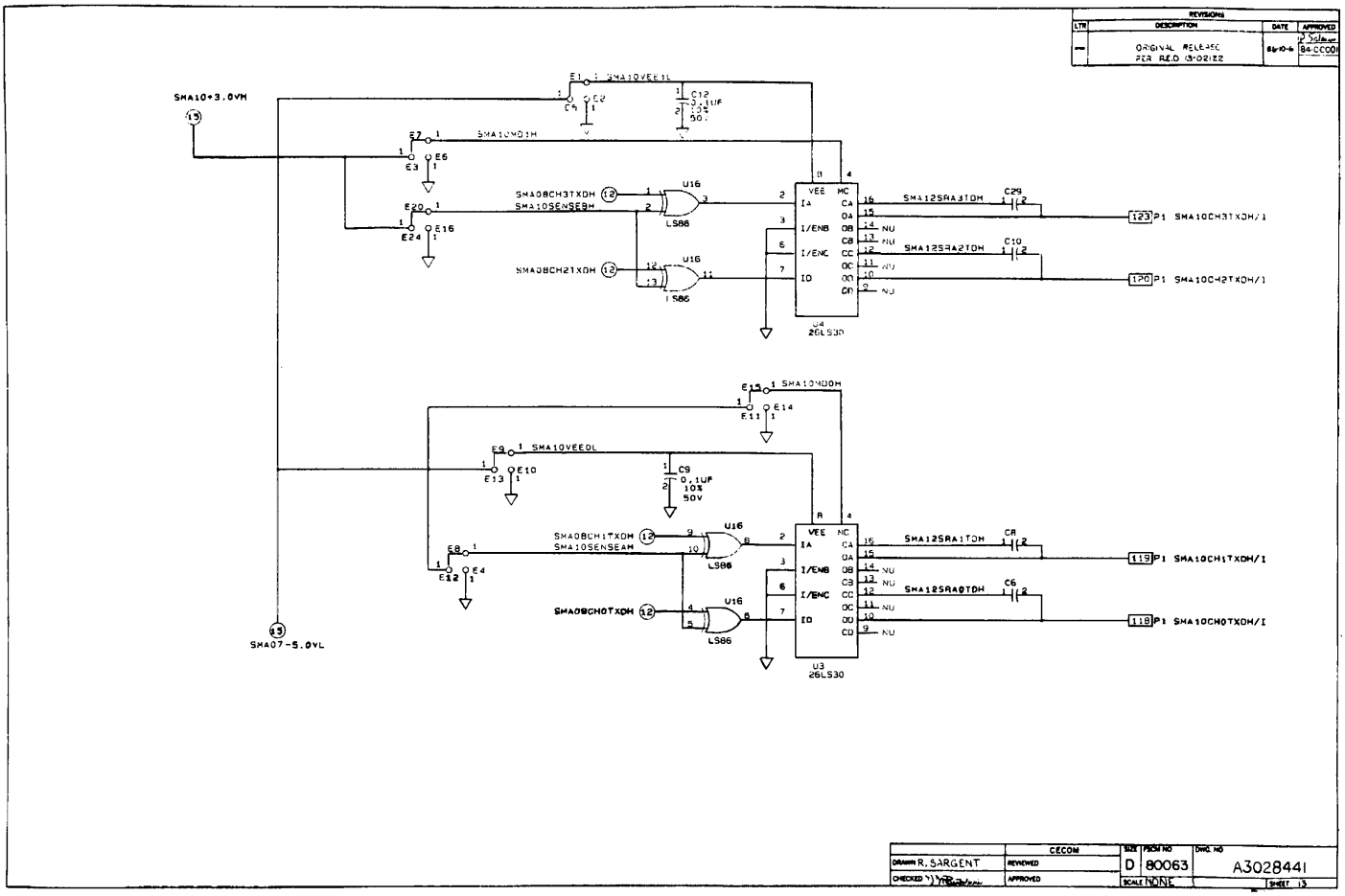
SMS SCHEMATIC

(Sheet 11 of 15)



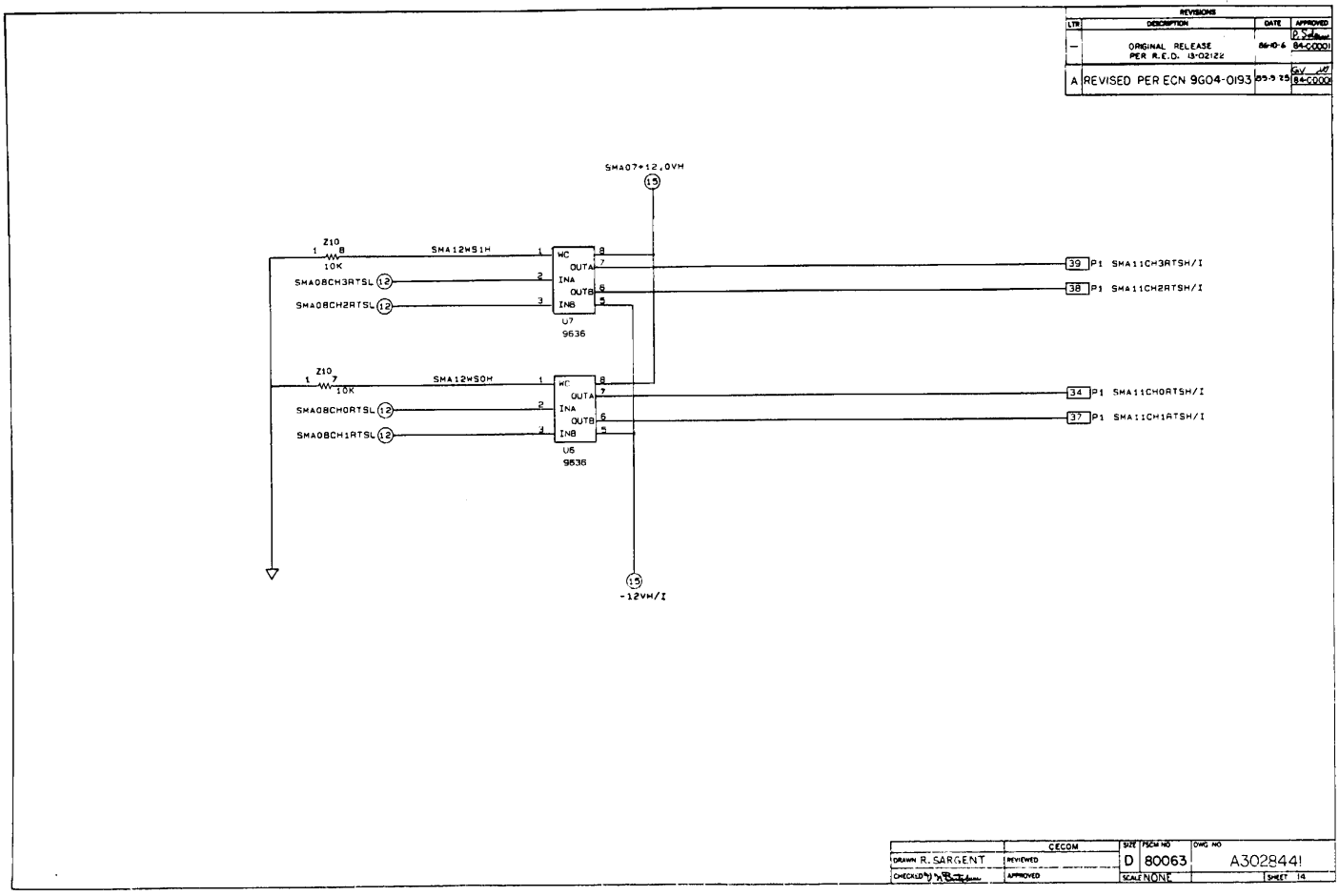
SMS SCHEMATIC

(Sheet 12 of 15)



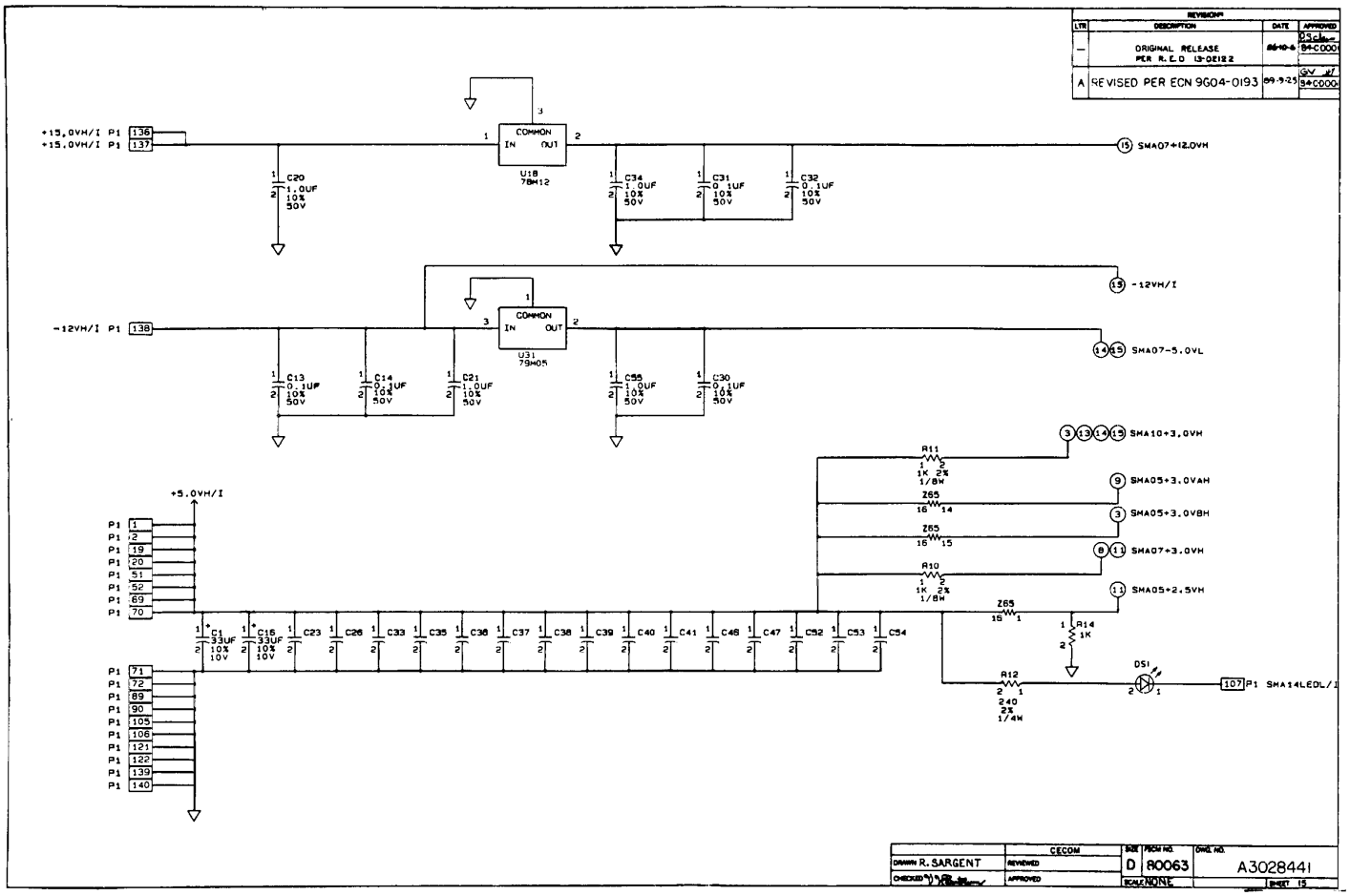
SMS SCHEMATIC

(Sheet 13 of 15)



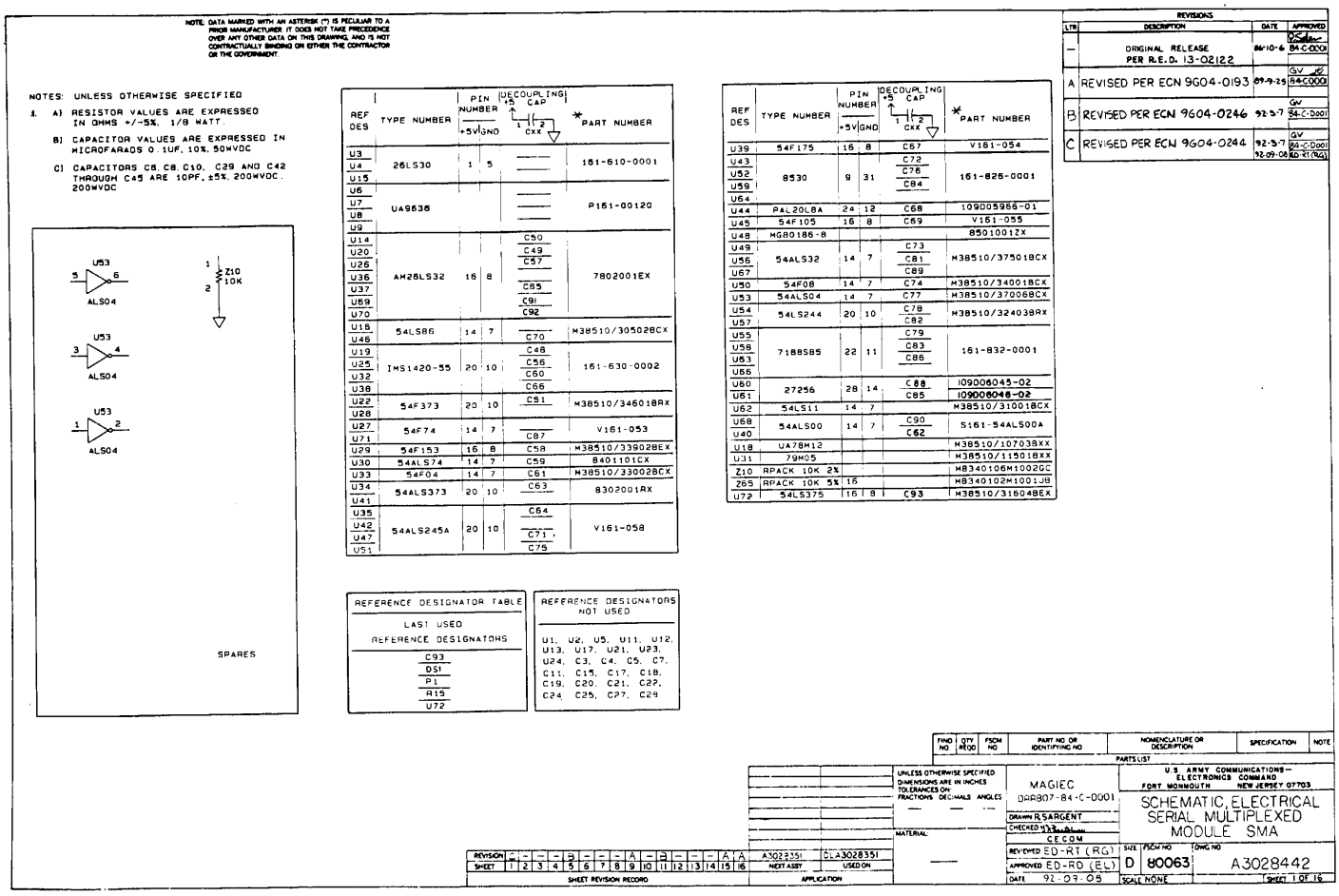
SMS SCHEMATIC

(Sheet 14 of 15)



SMS SCHEMATIC

(Sheet 15 of 15)

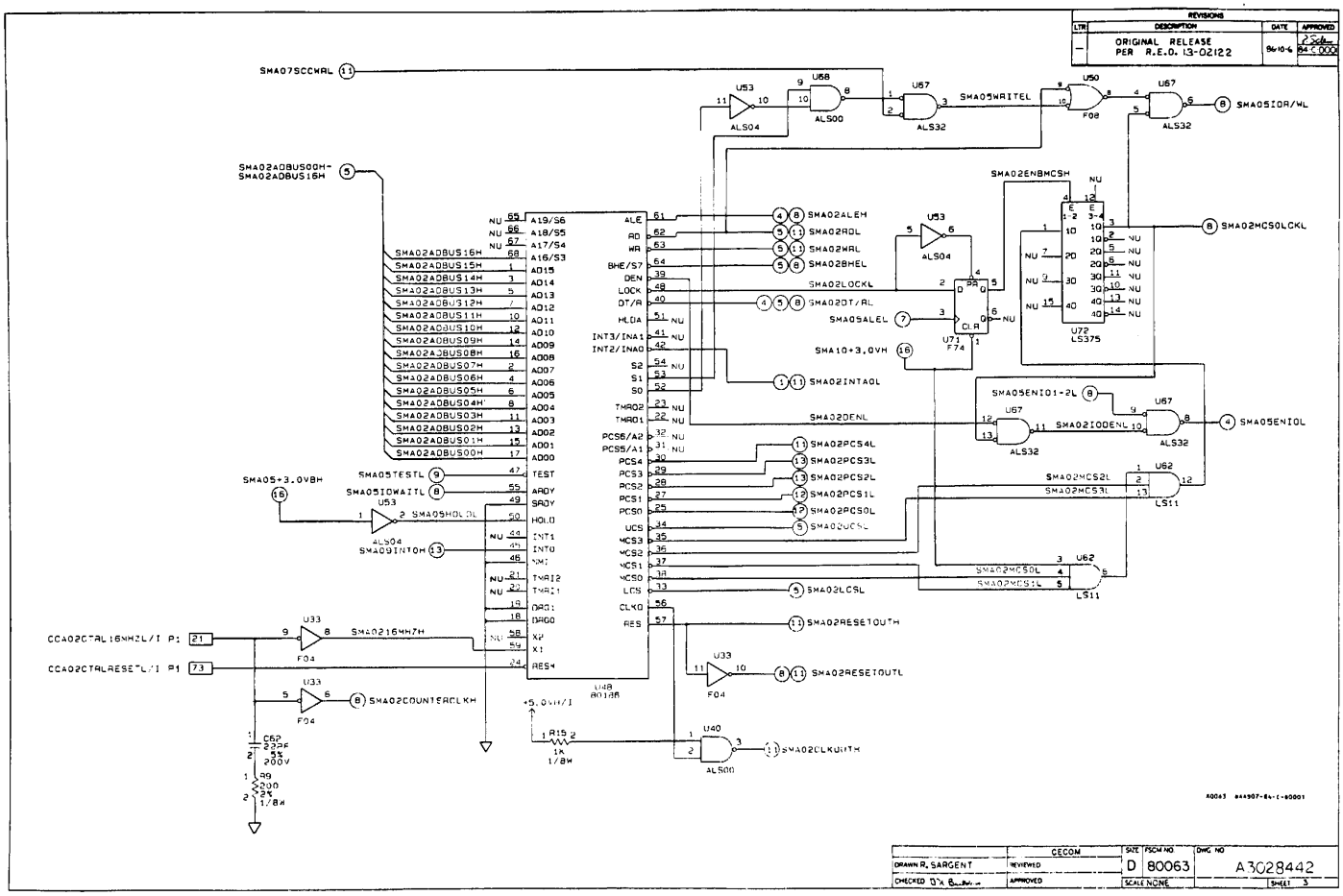


SMA SCHEMATIC

(Sheet 1 of 16)

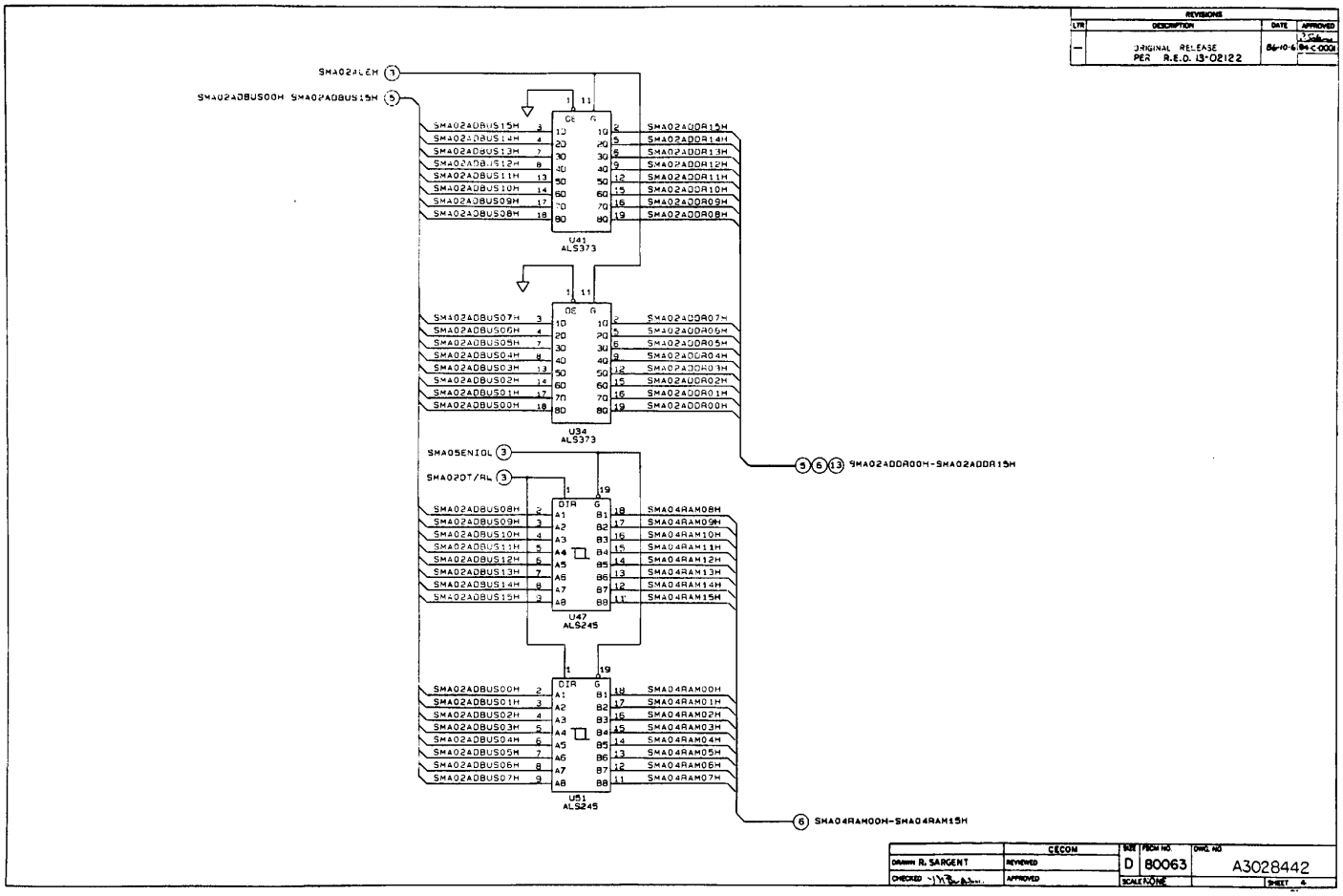
SMA SCHEMATIC

(Sheet 2 of 16)



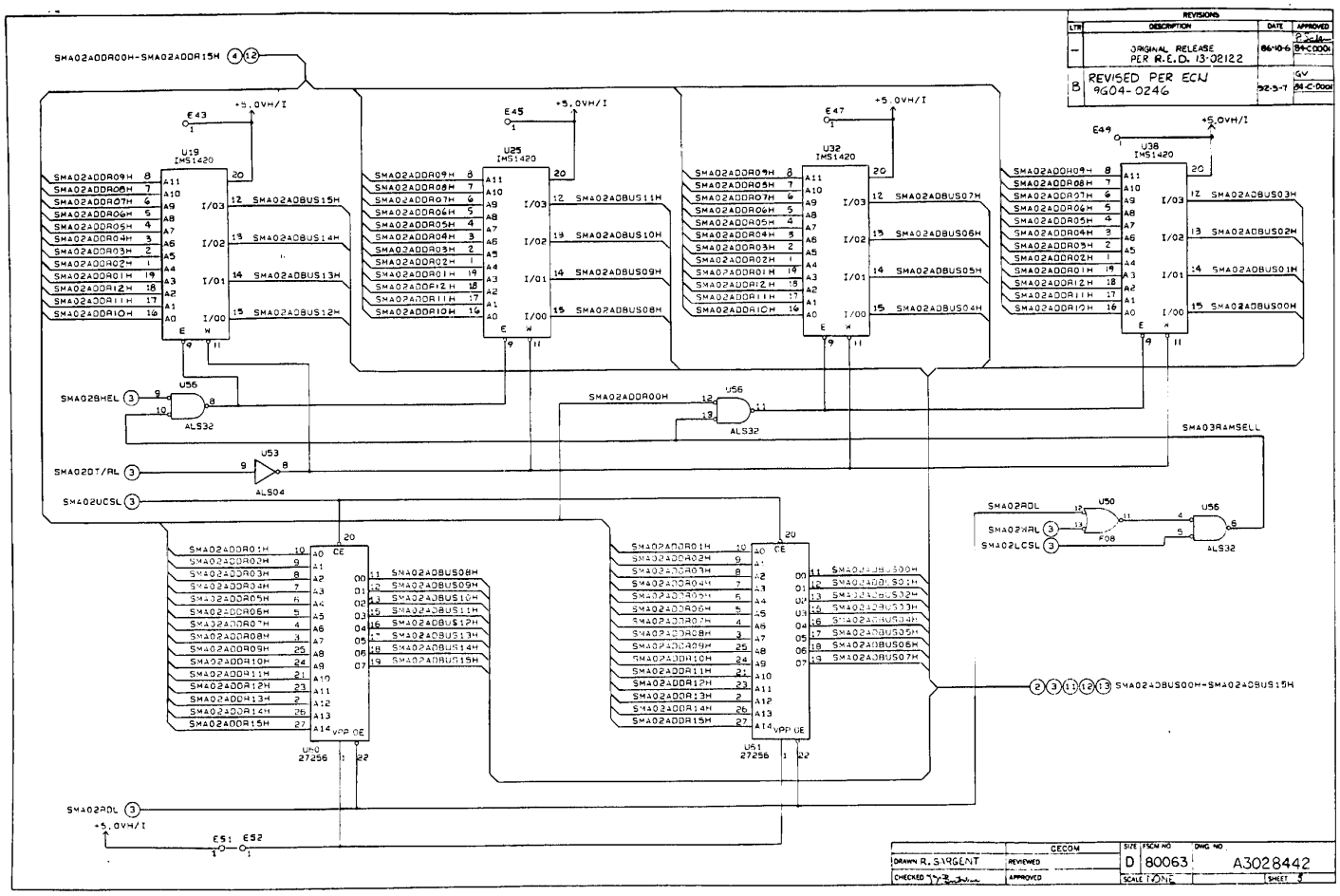
SMA SCHEMATIC

(Sheet 3 of 16)



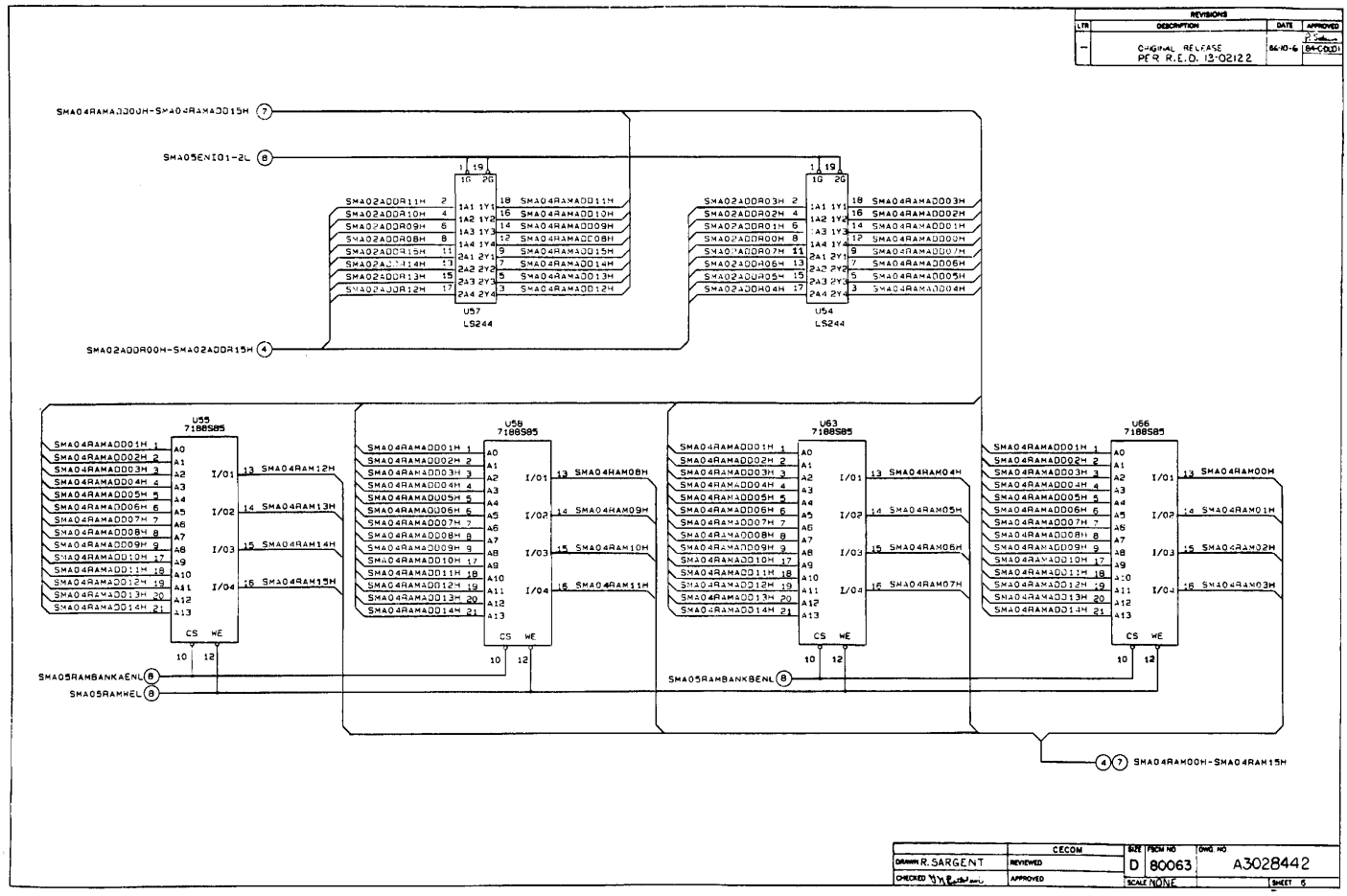
SMA SCHEMATIC

(Sheet 4 of 16)



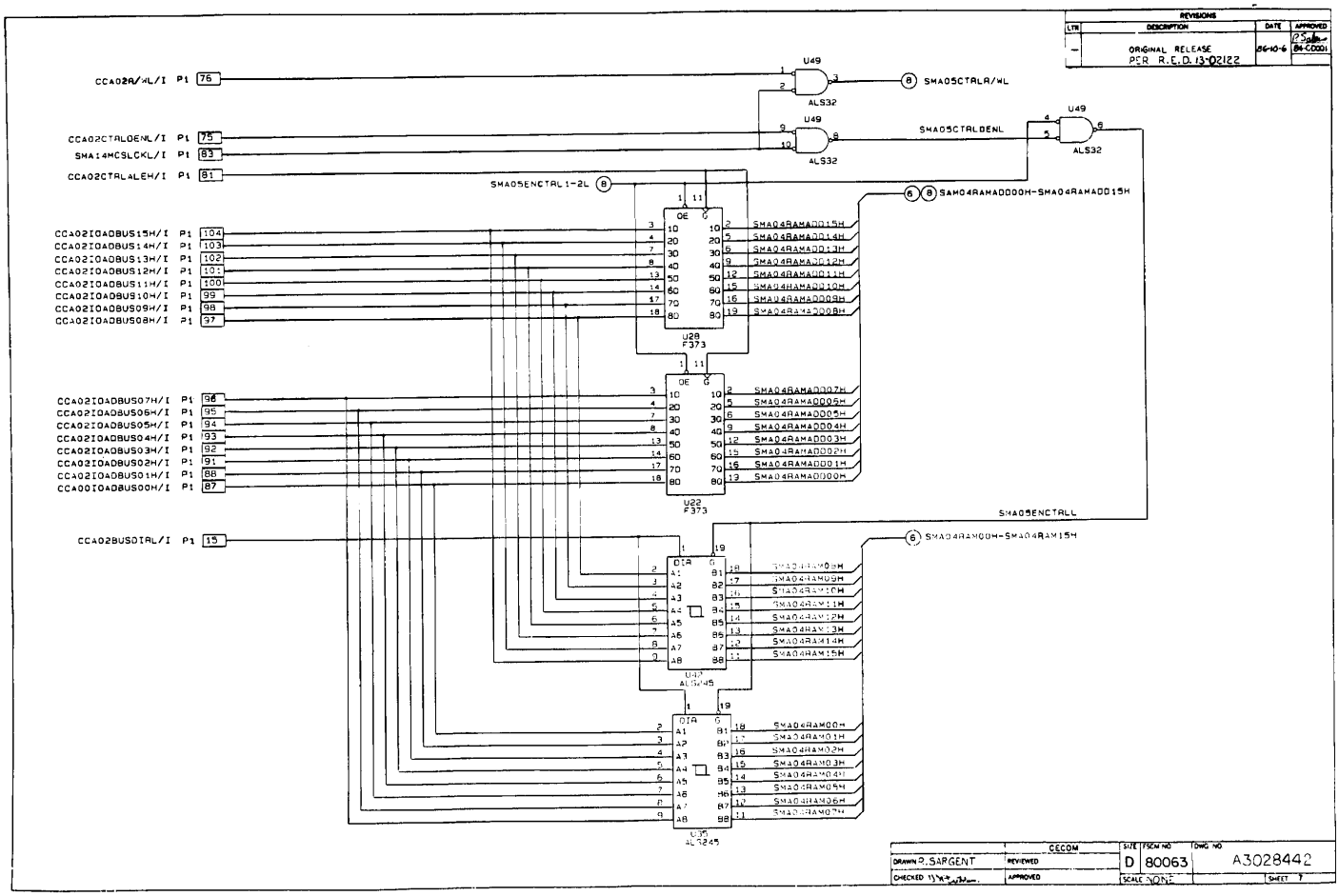
SMA SCHEMATIC

(Sheet 5 of 16)



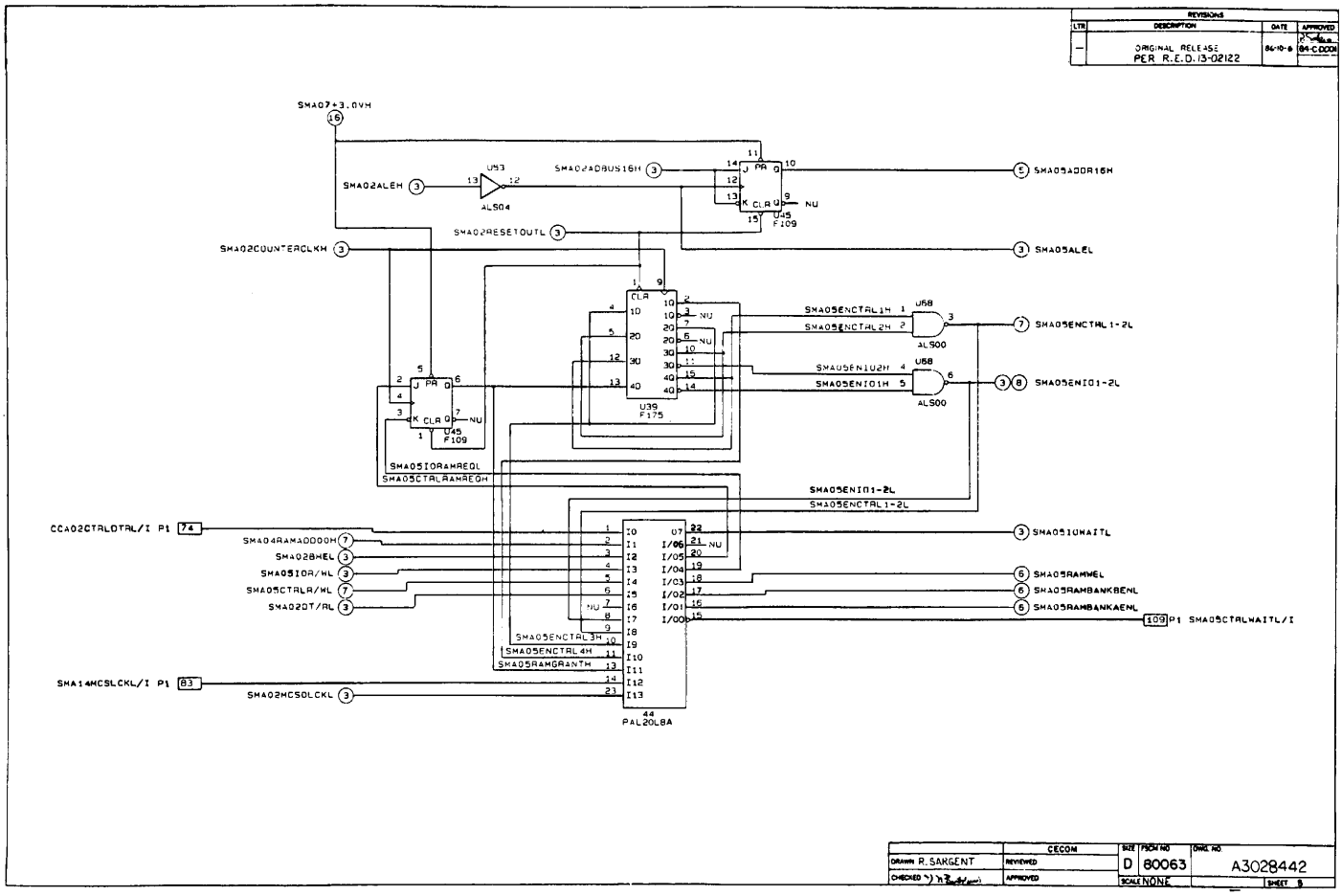
SMA SCHEMATIC

(Sheet 6 of 16)



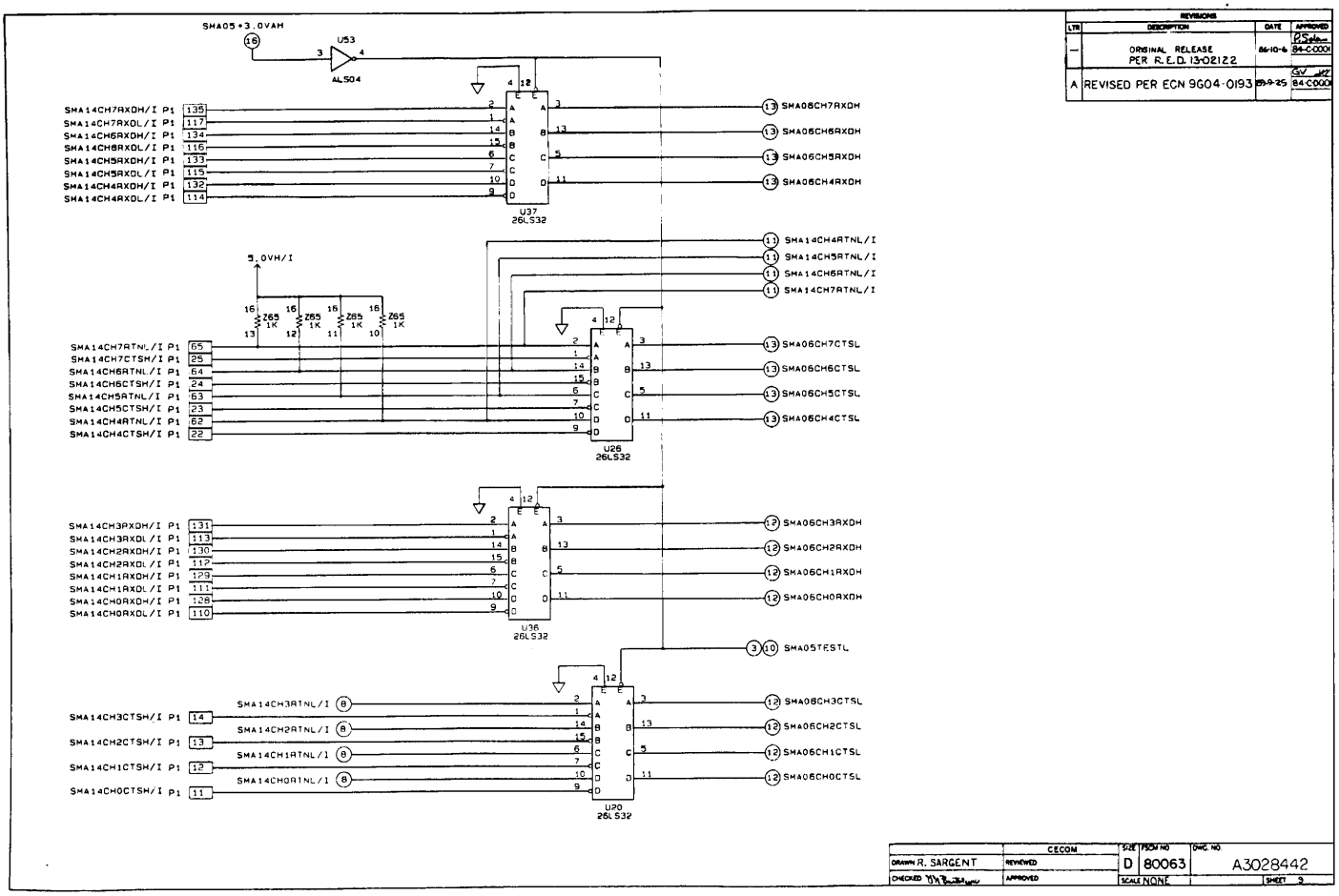
SMA SCHEMATIC

(Sheet 7 of 16)
I-130



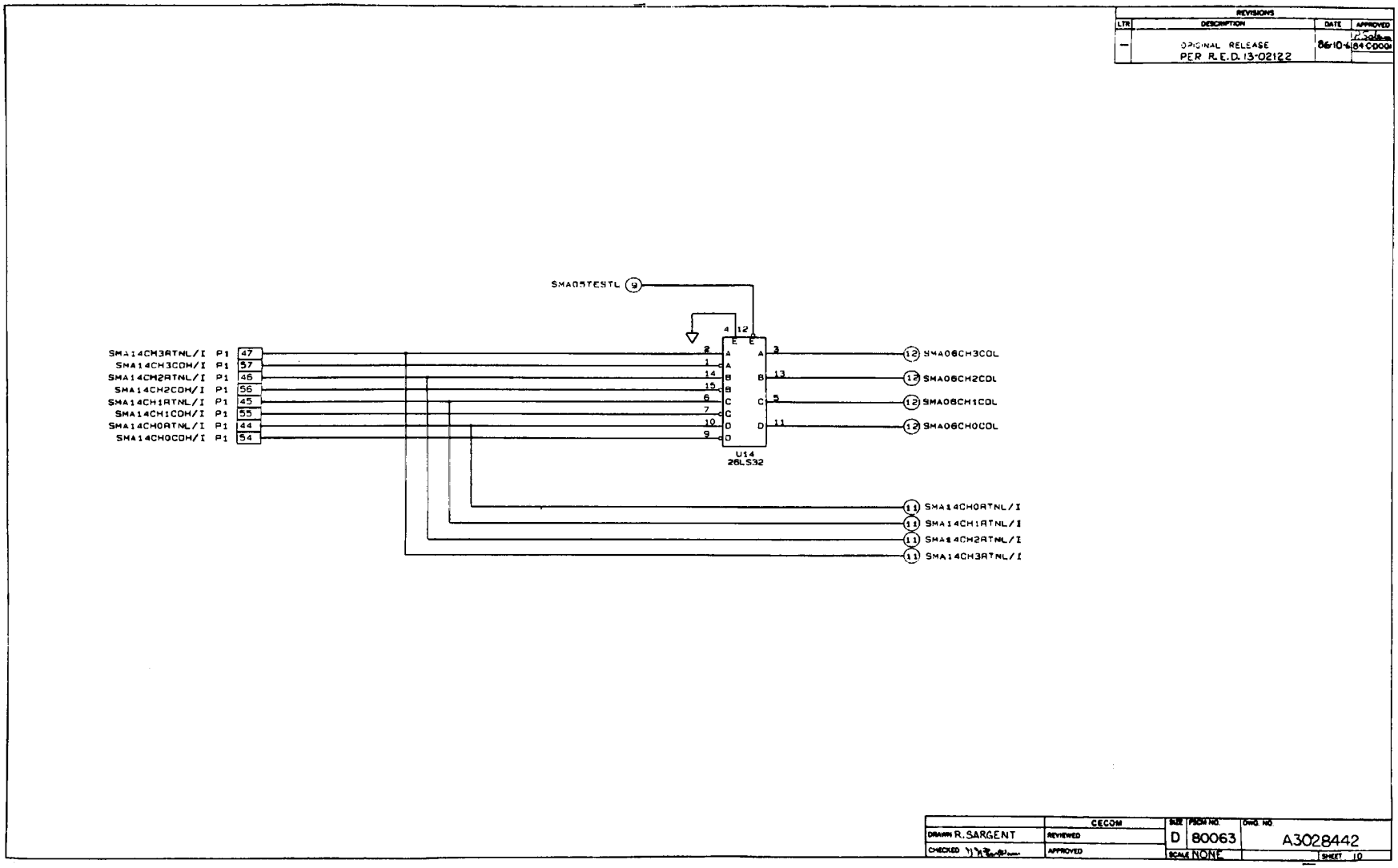
SMA SCHEMATIC

(Sheet 8 of 16)

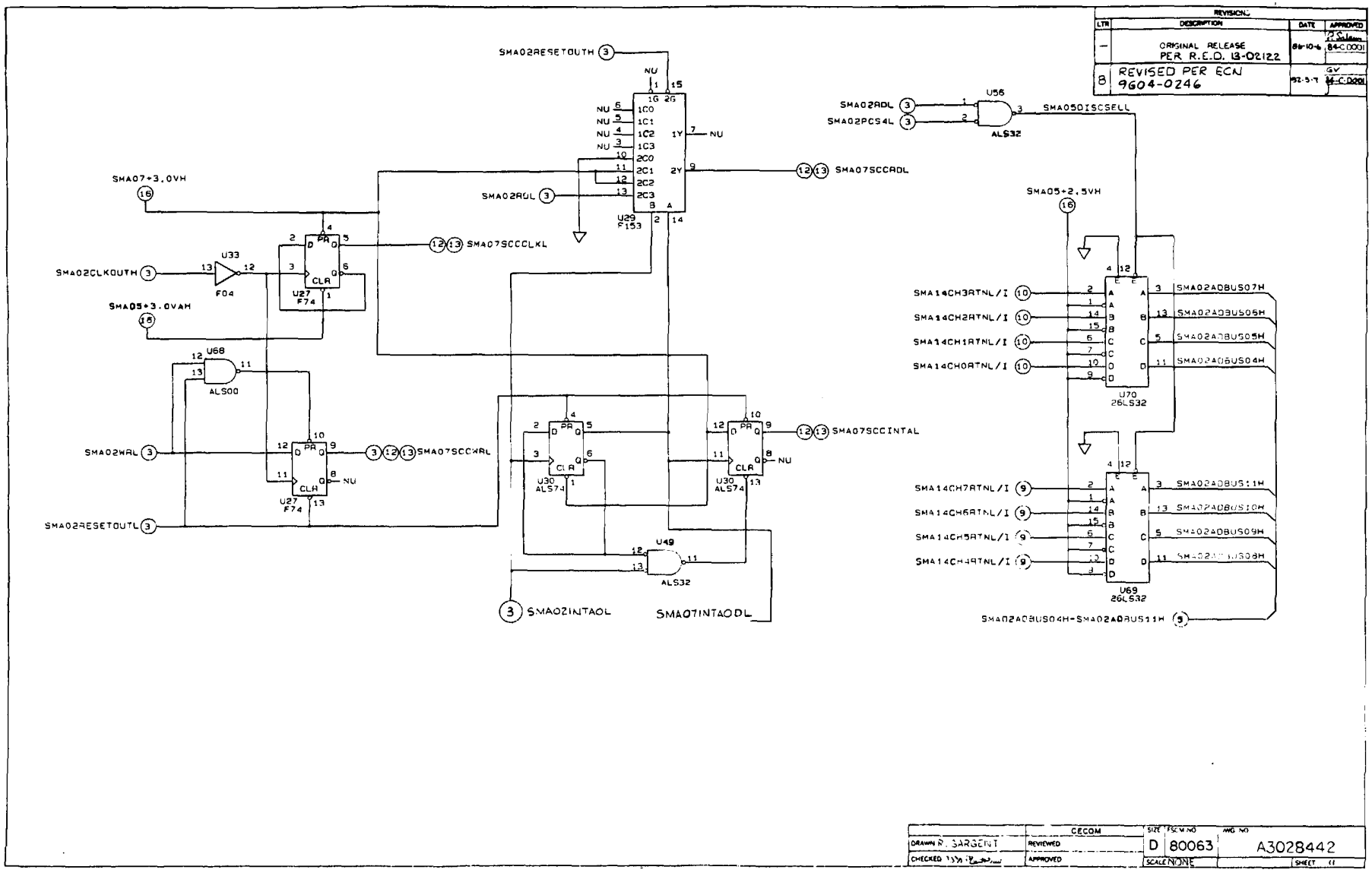


SMA SCHEMATIC

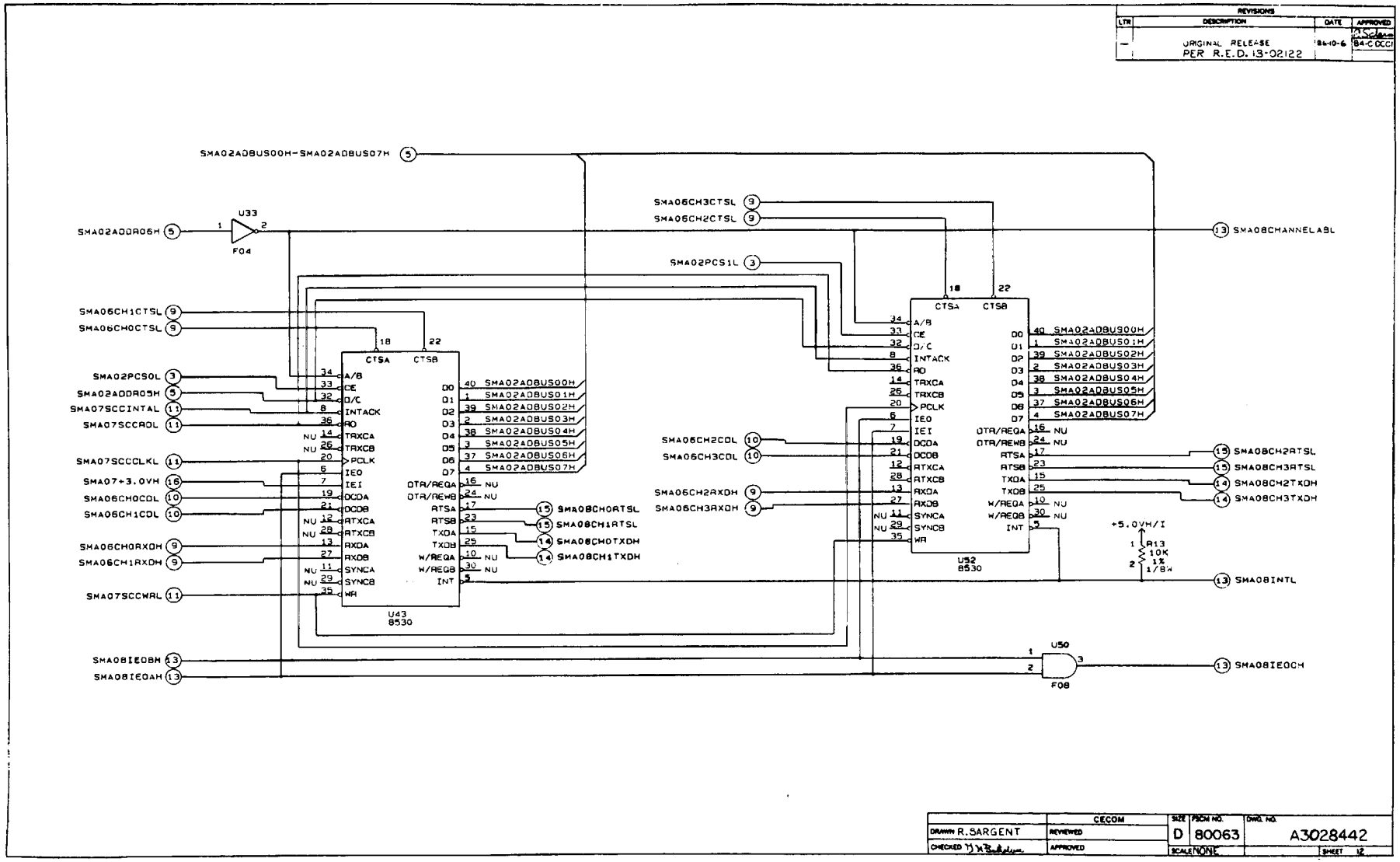
(Sheet 9 of 16)



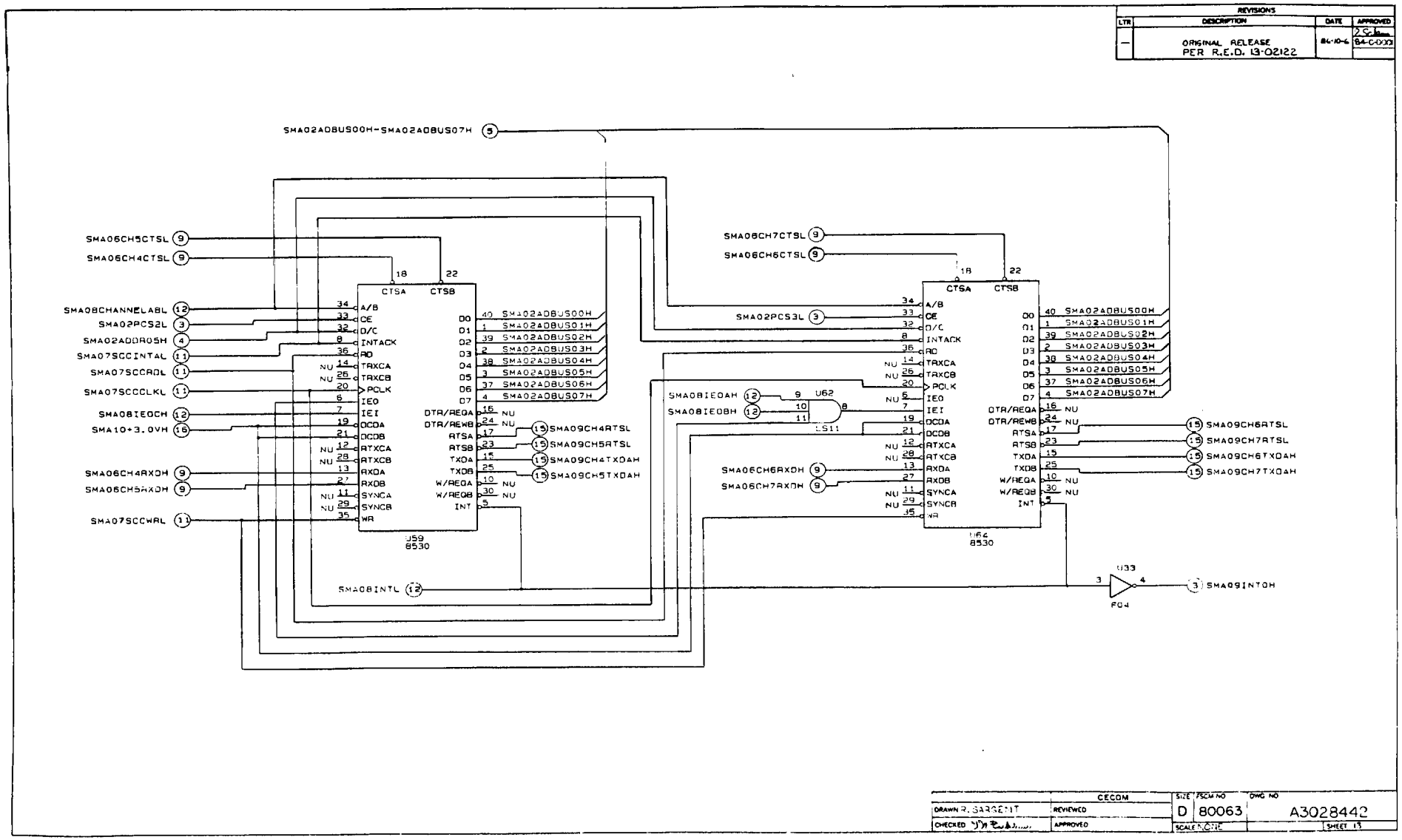
SMA SCHEMATIC
(Sheet 10 of 16)



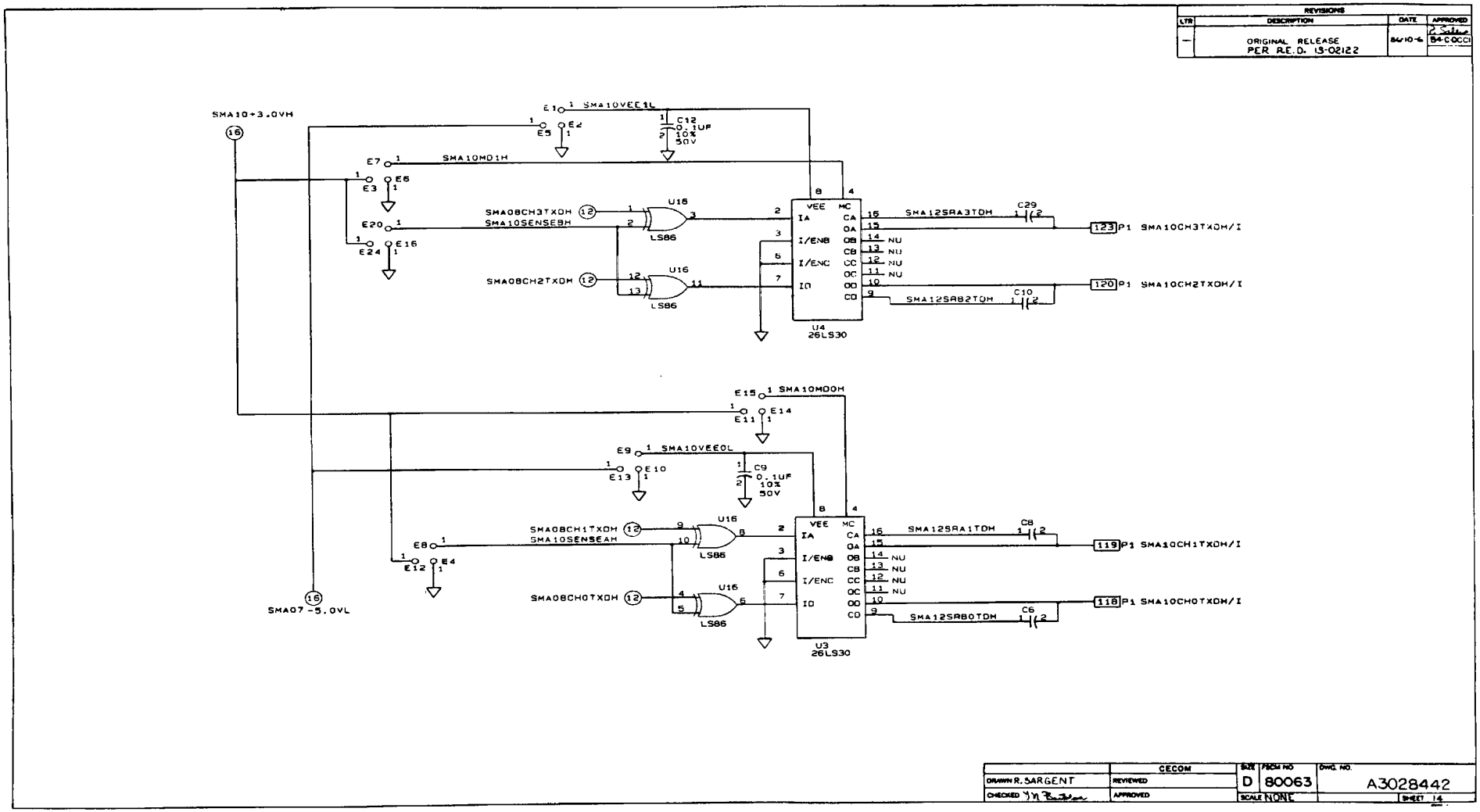
SMA SCHEMATIC
(Sheet 11 of 16)



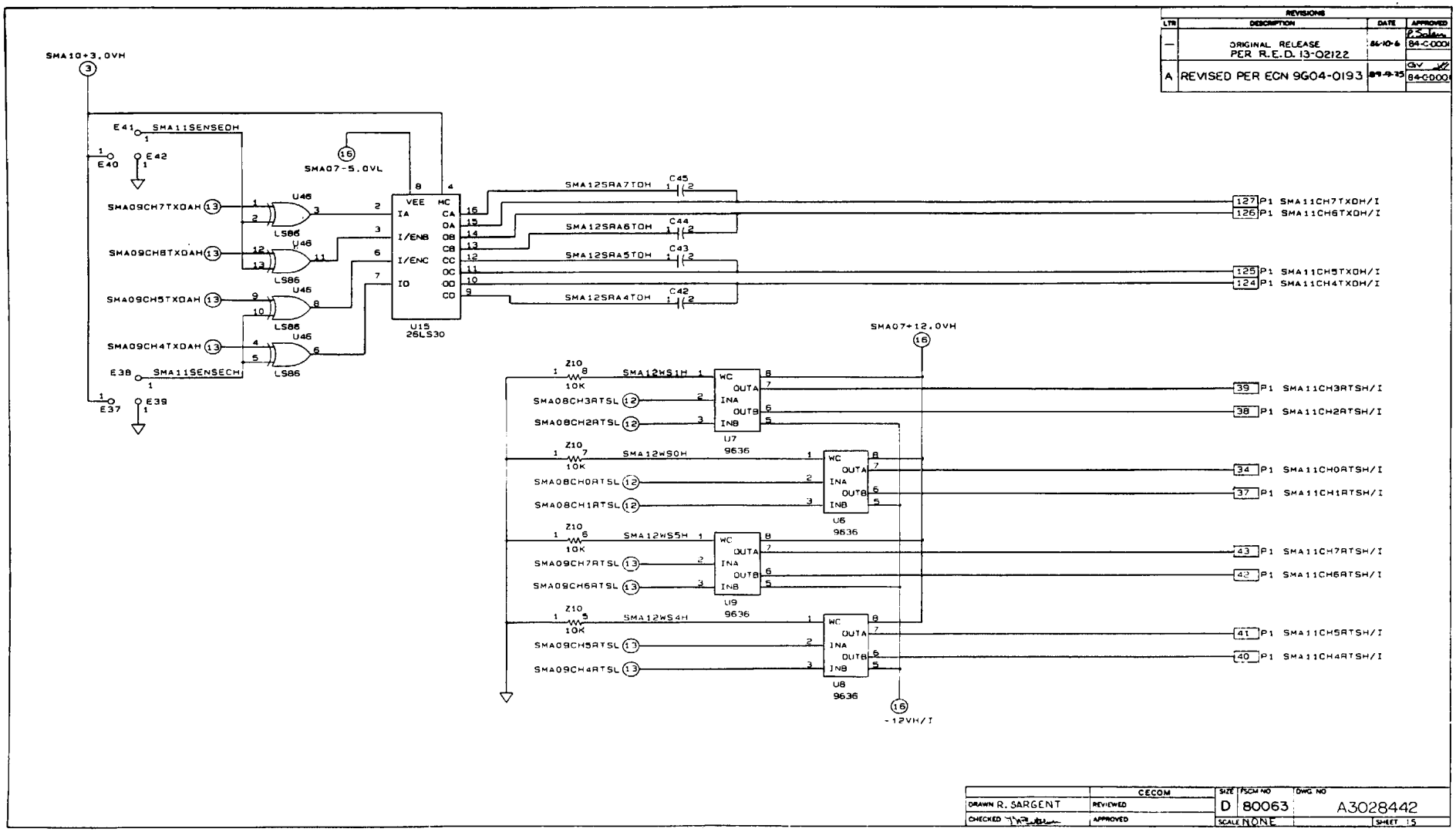
SMA SCHEMATIC
(Sheet 12 of 16)



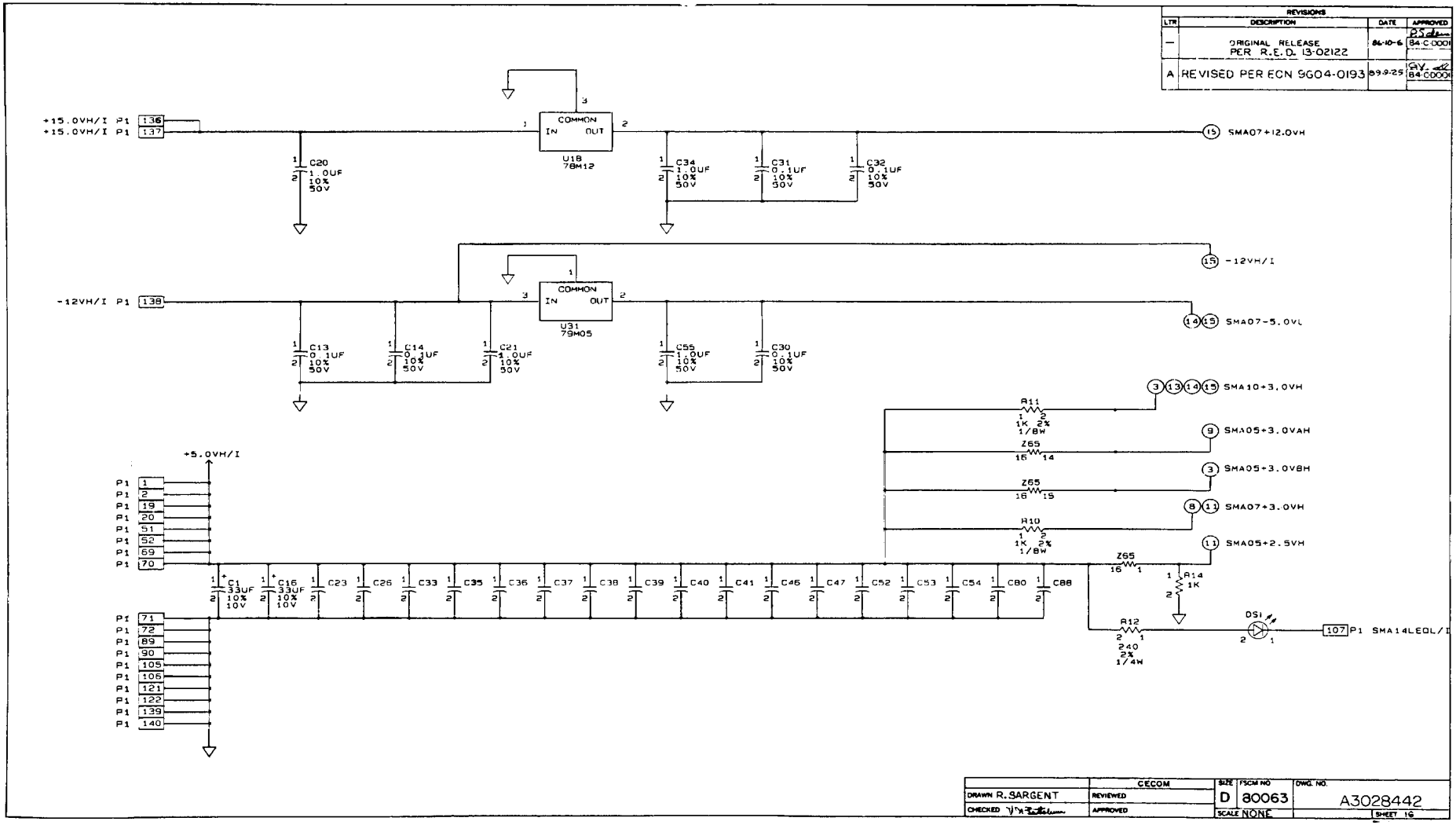
SMA SCHEMATIC
(Sheet 13 of 16)



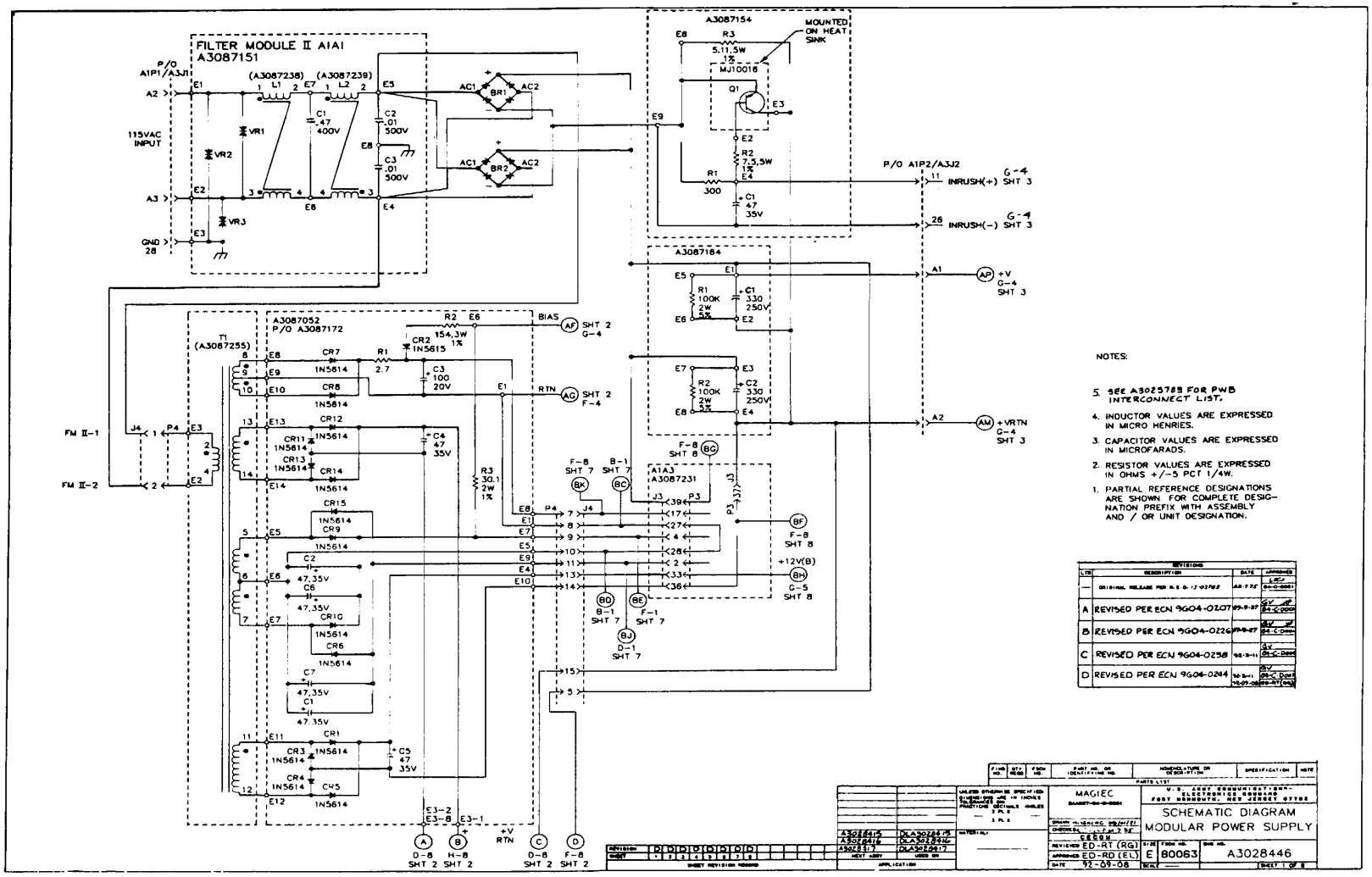
SMA SCHEMATIC
(Sheet 14 of 16)



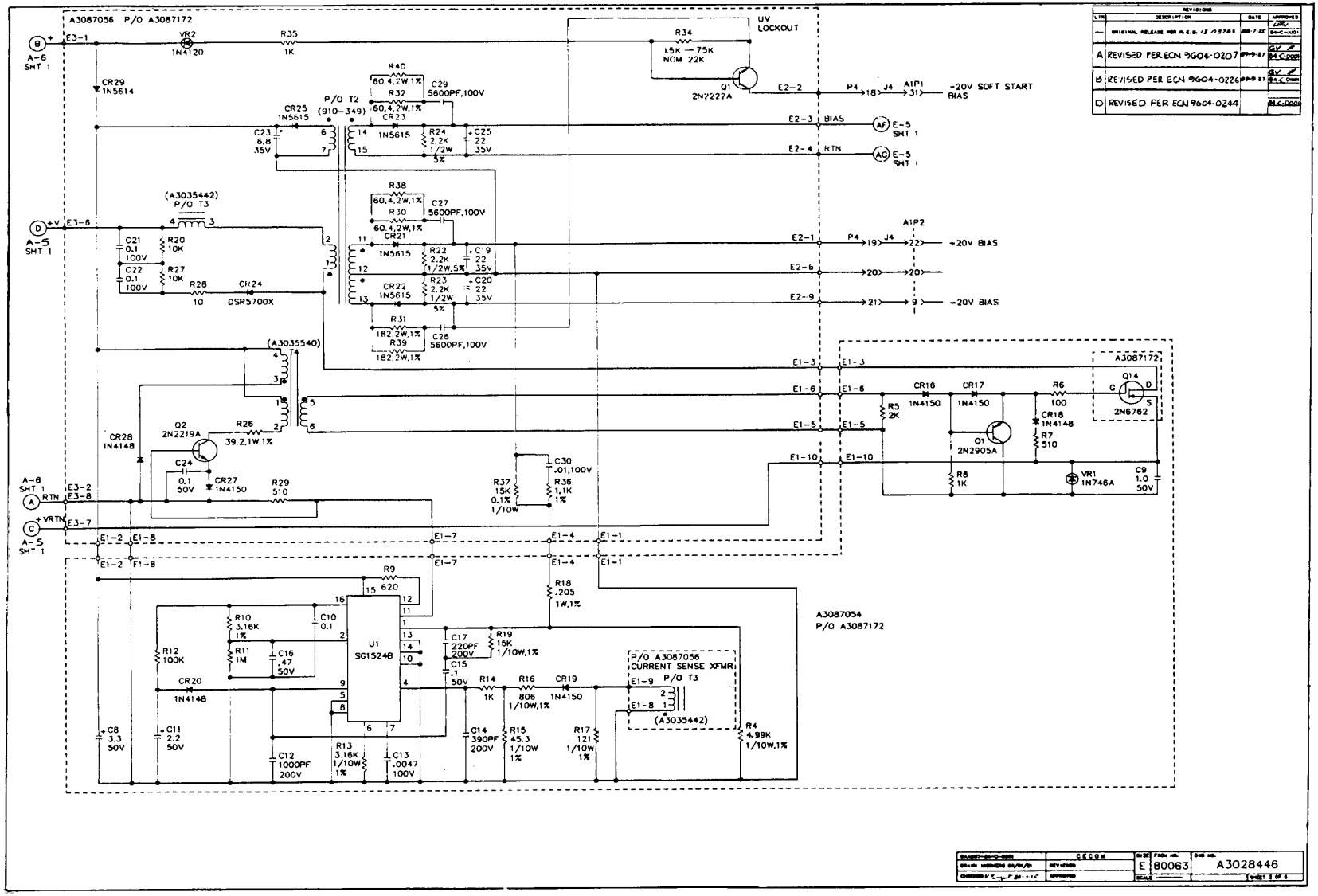
SMA SCHEMATIC
(Sheet 15 of 16)



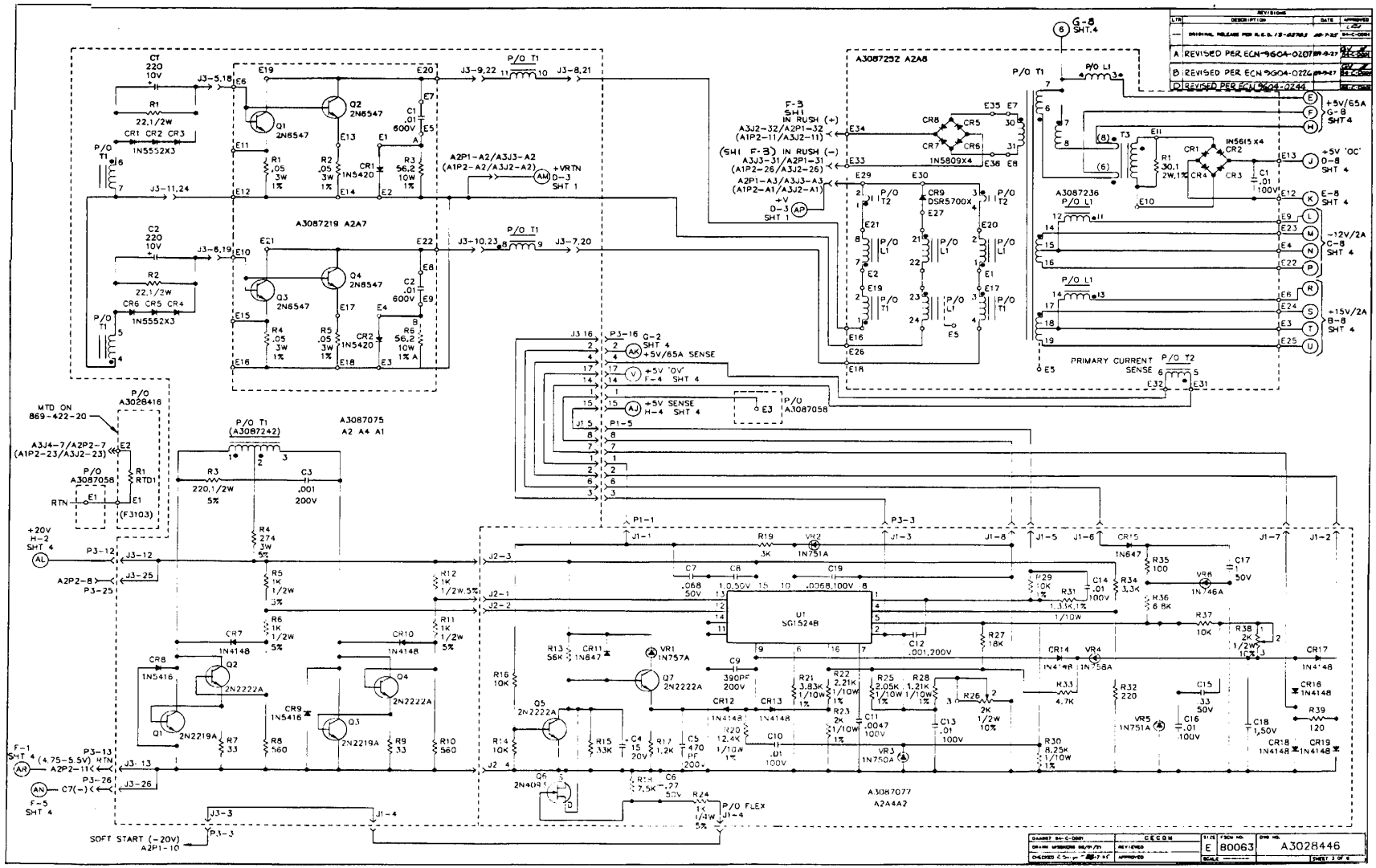
SMA SCHEMATIC
(Sheet 16 of 16)



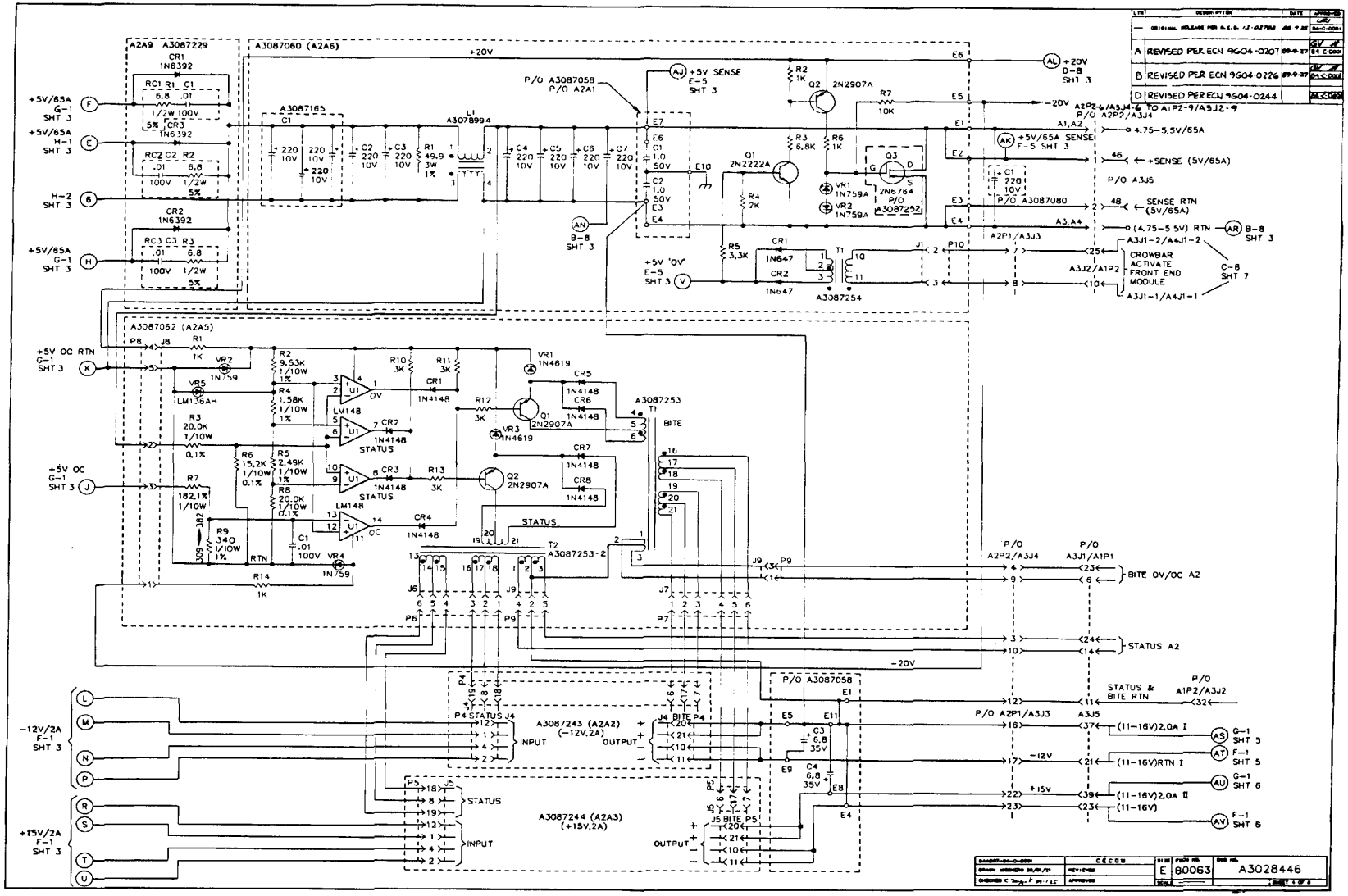
POWER SUPPLY SCHEMATIC
(Sheet 1 of 8)



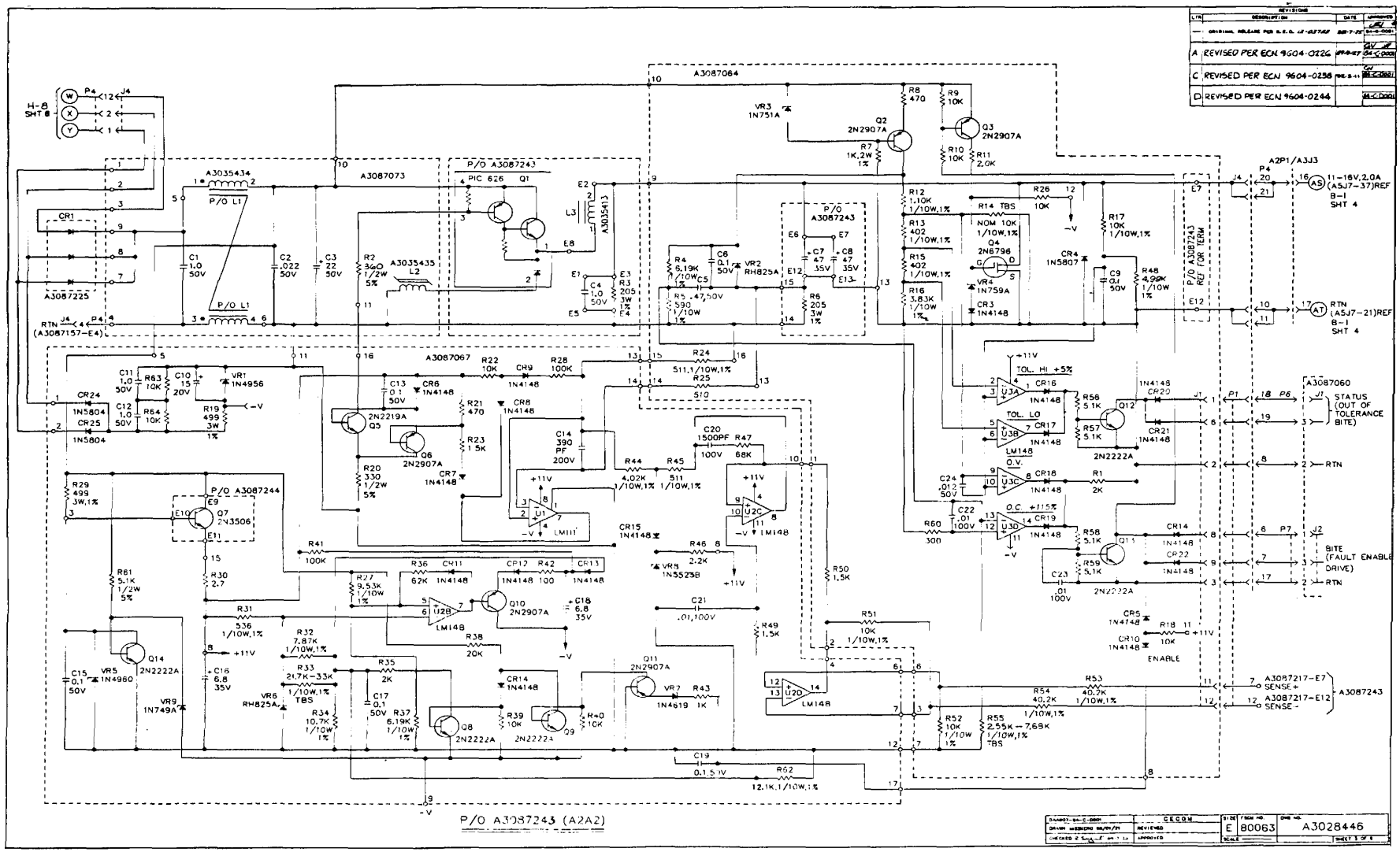
POWER SUPPLY SCHEMATIC
(Sheet 2 of 8)



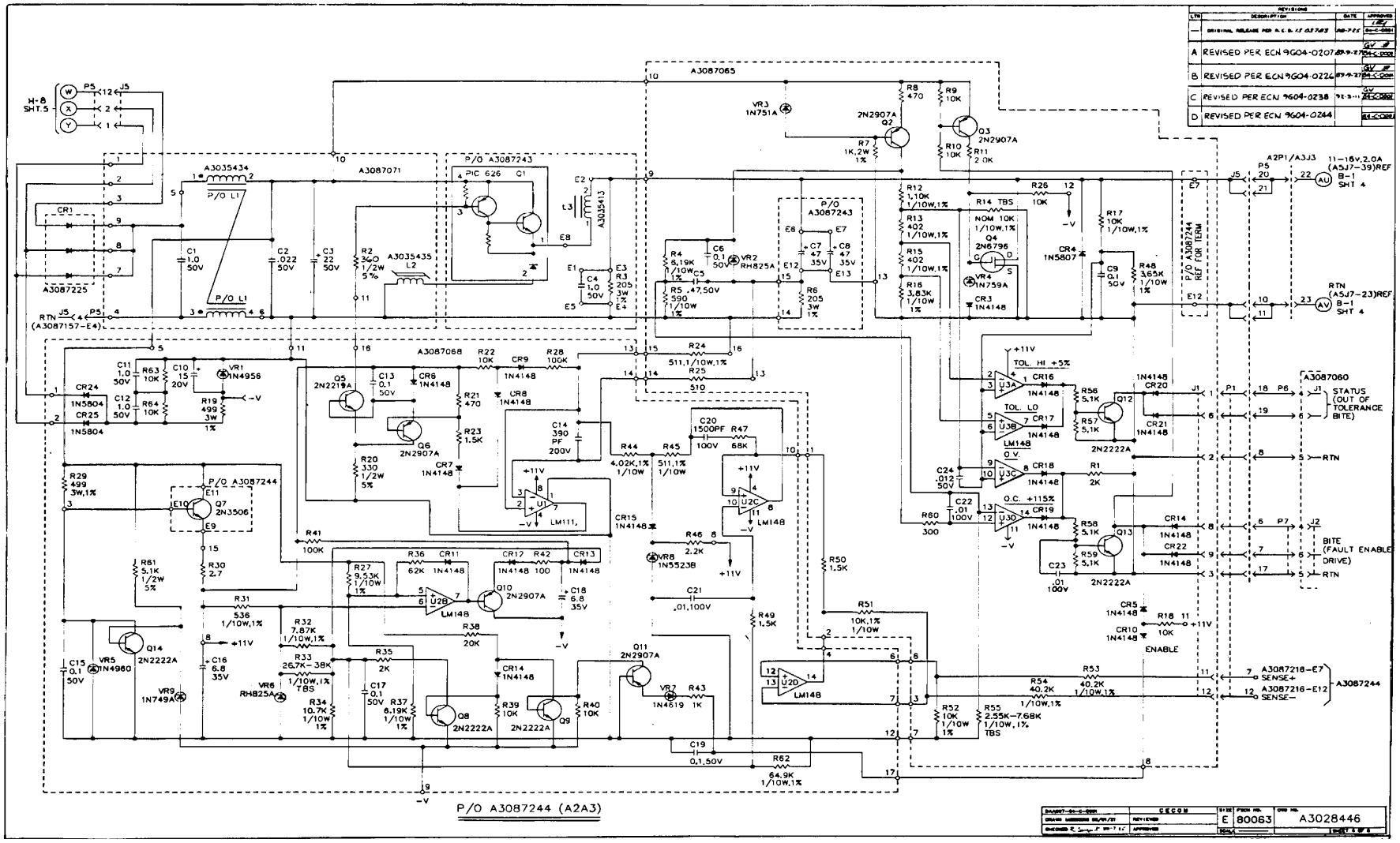
POWER SUPPLY SCHEMATIC
(Sheet 3 of 8)



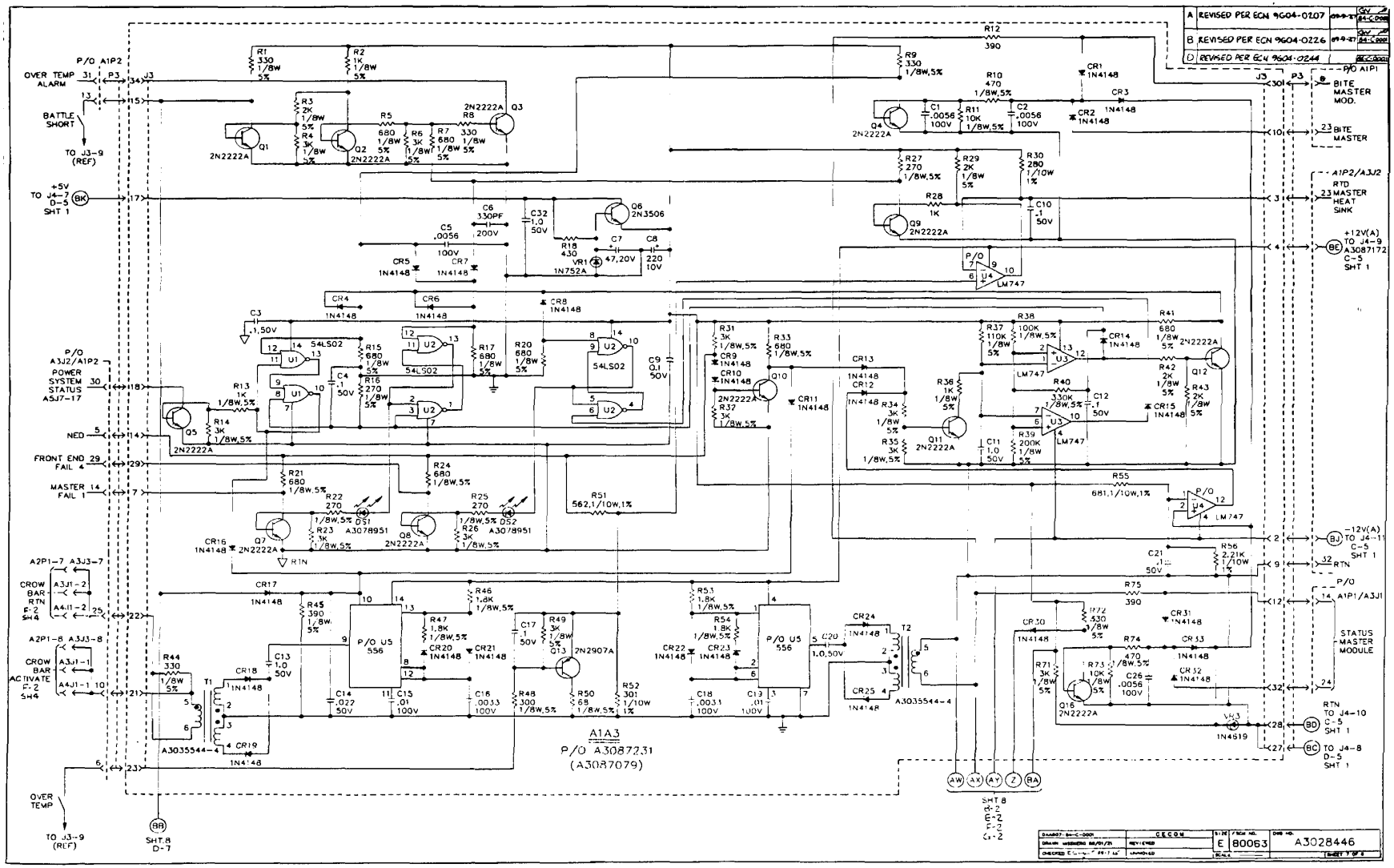
POWER SUPPLY SCHEMATIC
(Sheet 4 of 8)



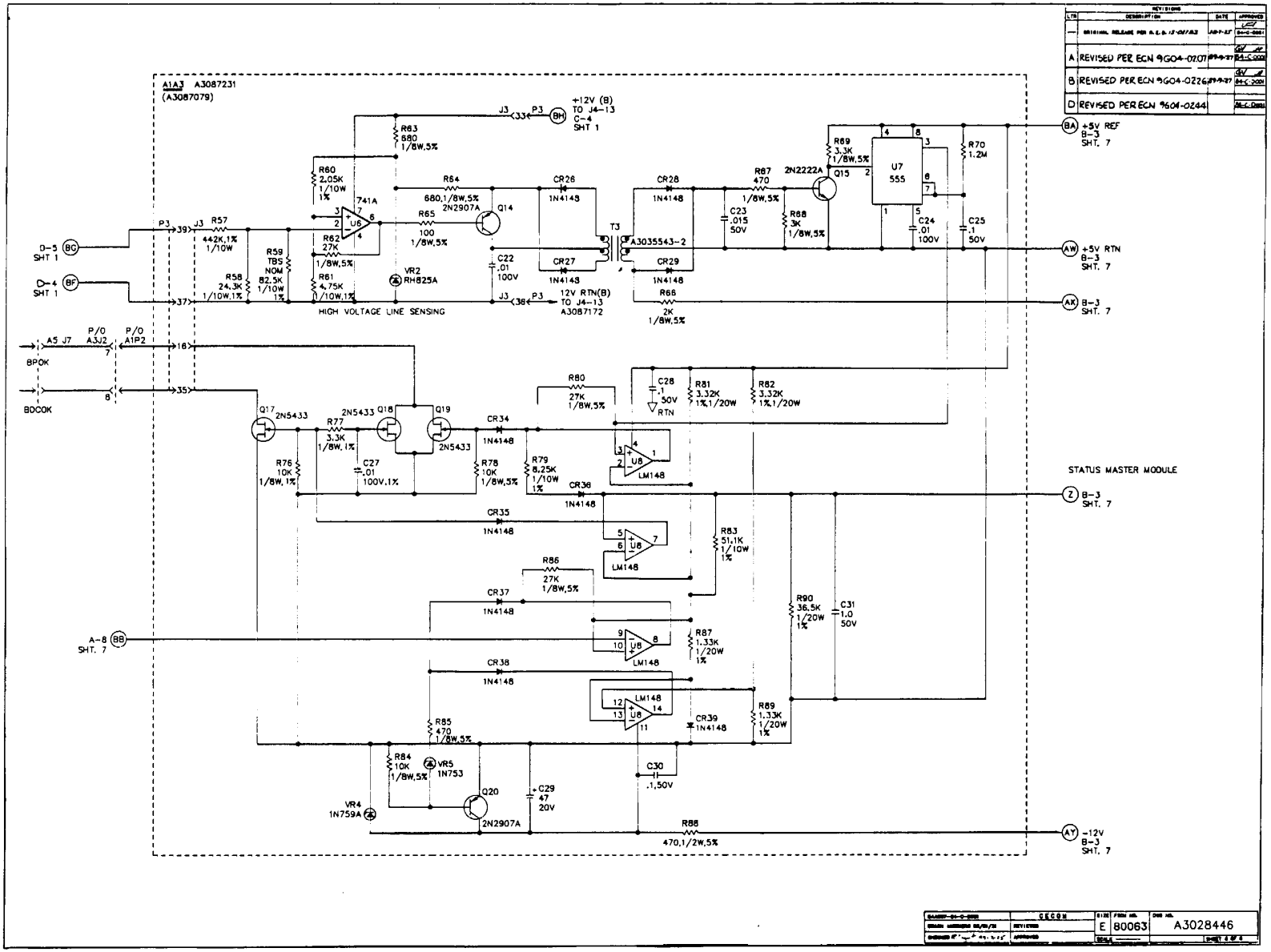
POWER SUPPLY SCHEMATIC
(Sheet 5 of 8)



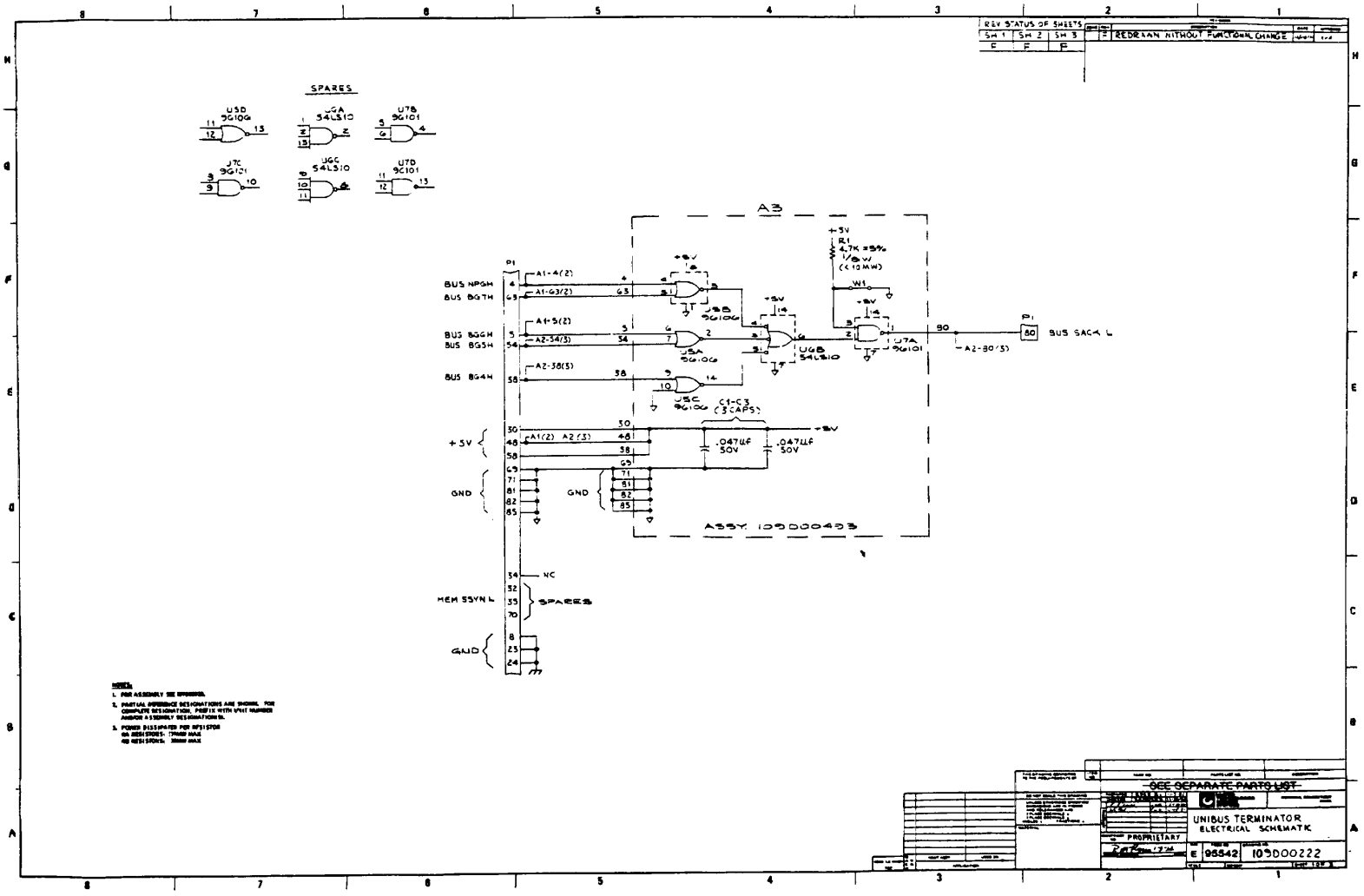
POWER SUPPLY SCHEMATIC
(Sheet 6 of 8)



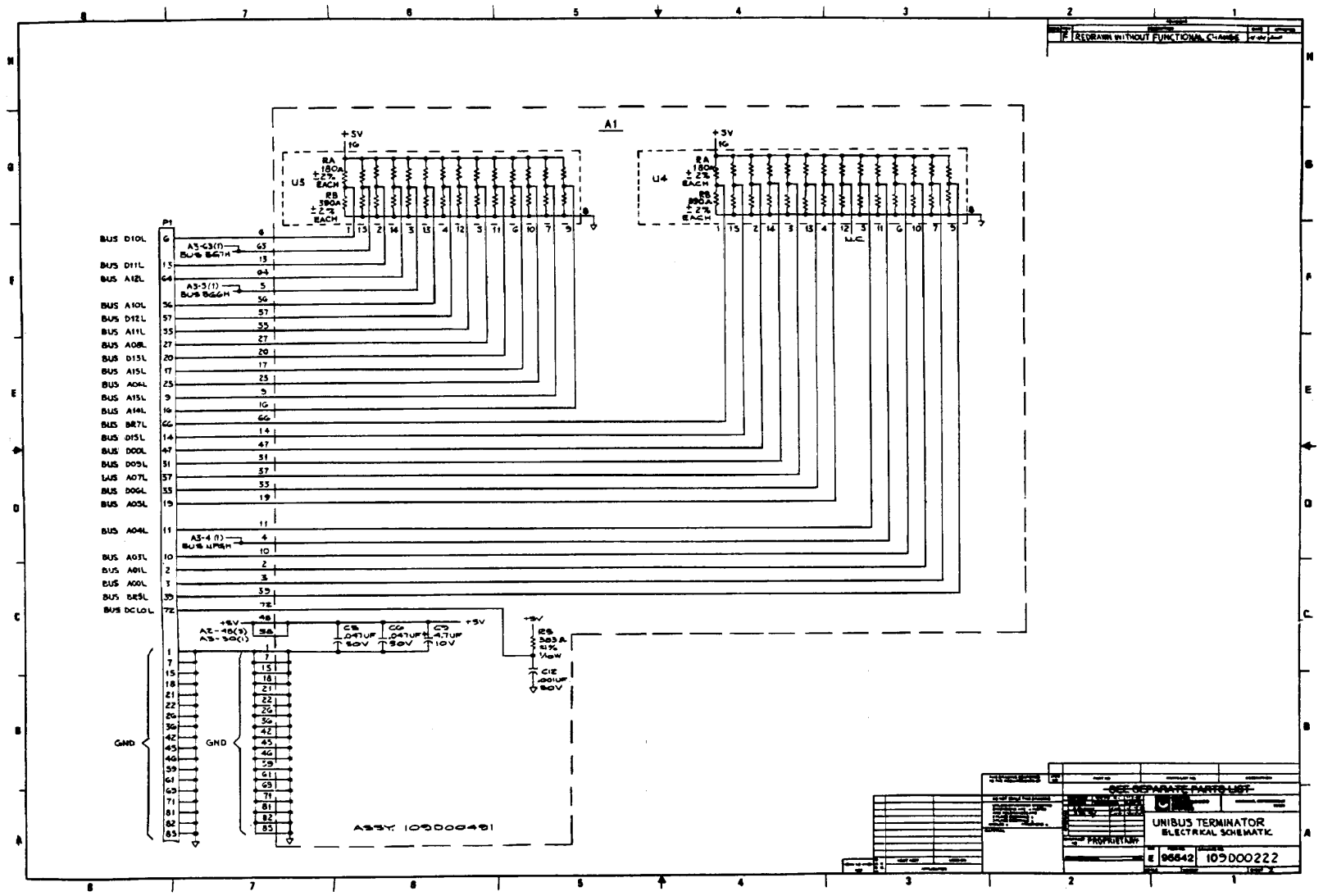
POWER SUPPLY SCHEMATIC
{Sheet 7 of 8)



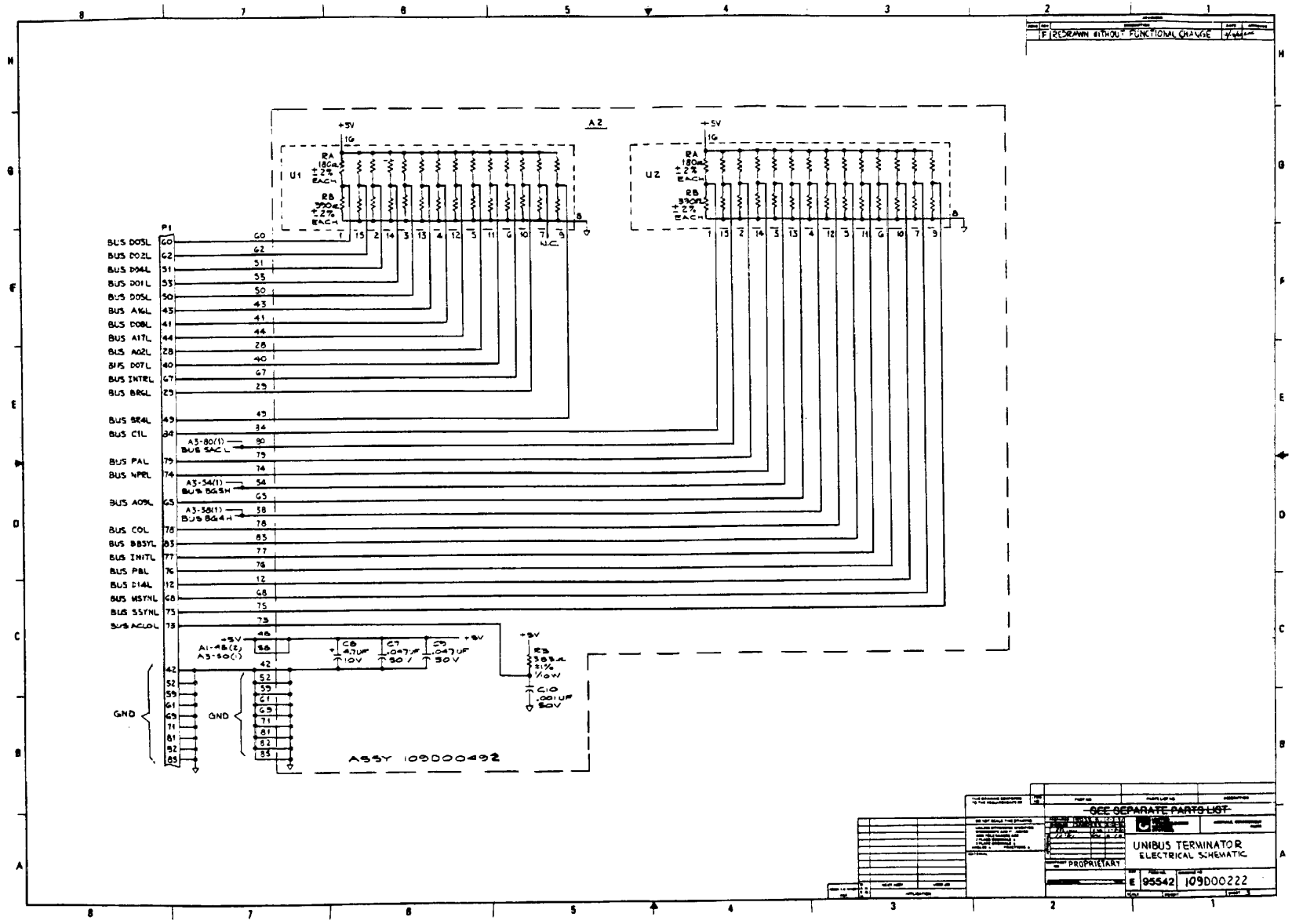
POWER SUPPLY SCHEMATIC
(Sheet 8 of 8)



UNIBUS TERMINATOR SCHEMATIC
(Shoot 1 of 3)



UNIBUS TERMINATOR SCHEMATIC
(Sheet 2 of 3)

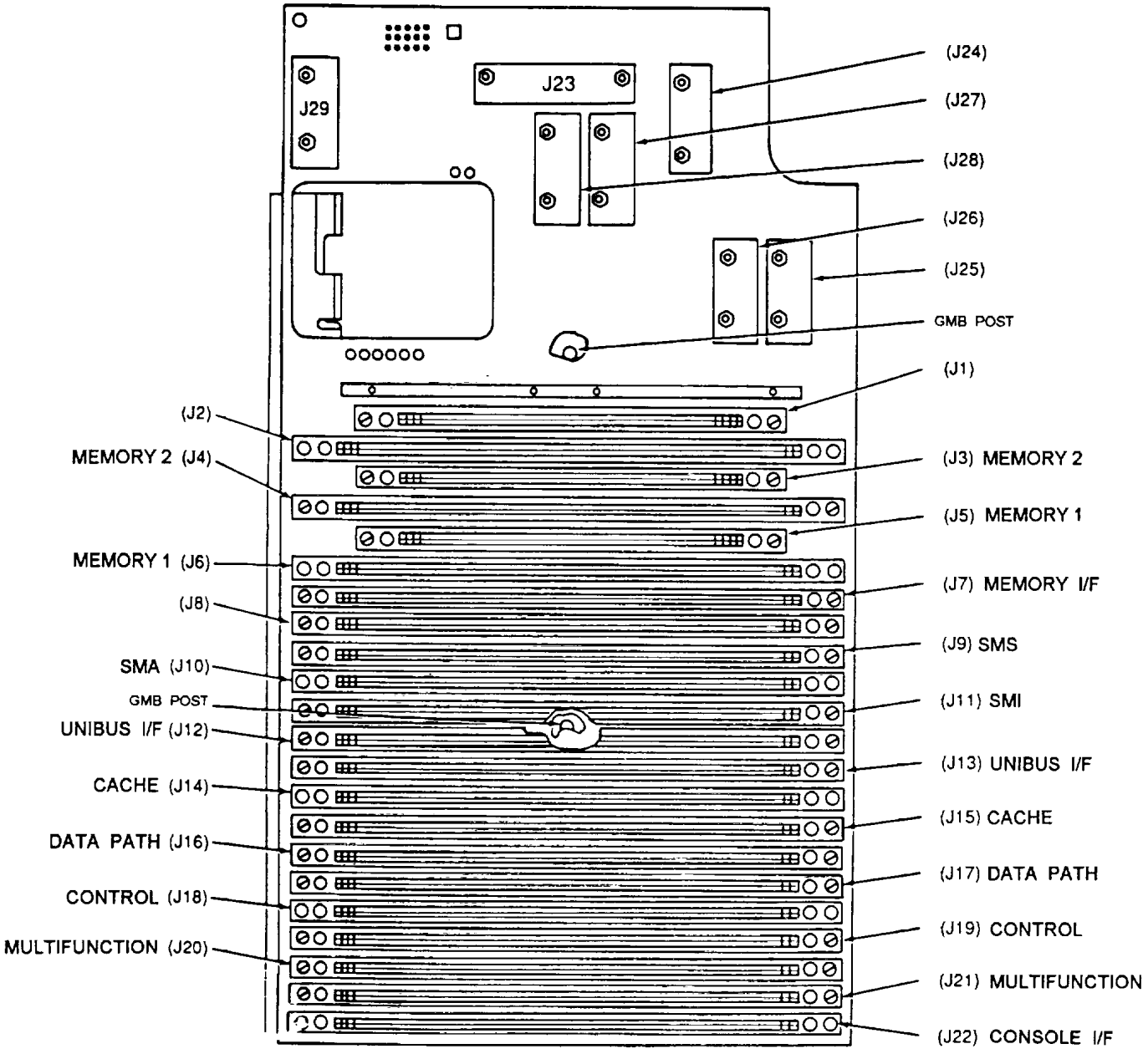


UNIBUS TERMINATOR SCHEMATIC
(Sheet 3 of 3)

APPENDIX J

Interconnect List For
Grandmother Board A3028354/A3086887

SUBJECT **PAGE**



GMB Connector Locations

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
E 1	BUS DCLO L
E 2	BUS ACLO L
E 3	+15V
E 4	+15V
E 5	+15V
E 6	-12V
E 7	-12V
E 8	-12V
E 9	MEMLCK 1
E10	MEMLCK 2
E11	MEMLCK 3
E12	MEMLCK 4
E13	MEMLCK 5
E14	MEMLCK 6
E15	MEMLCK 7
E16	MEMLCK 8
E17	MEMLCK 9
E18	MEMLCK 10
E19	MEMLCK 11
E20	MEMLCK 12
E21	+5V
E22	GND
301- 1	GND
J01- 2	GND
J01- 3	A01 H
J01- 4	DATA 01 H
J01- 5	A02 H
J01- 6	DATA 00 H
J01- 7	A03 H
J01- 8	DATA 03 H
J01- 9	A04 H
J01- 10	DATA 02 H
J01- 11	A05 H
J01- 12	DATA 05 H
J301- 13	A06 H
J301- 14	DATA 04 H
J01- 15	A14 H
J01- 16	DATA 00 H
J01- 17	DATA 07 H
J01- 18	DATA 04 H
J01- 21	DATA RDY (3) L
J01- 22	GND
J01- 23	REF SYNC H
J01- 24	A17 H
J01- 25	DATA 06 H
J01- 26	PARITY LSB H
J01- 28	DATA 07 H
J01- 29	DATA 06 H
J01- 30	DATA 03 H
J01- 31	DATA 05 H
J01- 32	GND
J01- 33	LSB BYTE CONTROL H
J01- 34	DATA 02 H
J01- 35	CYCLE INIT H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J01- 36	GND
J01- 38	DATA 01 H
J01- 40	DATA OUT CONT (3)L
J01- 41	PARITY LSB H
J01- 42	GND
J01- 43	MSB BYTE CONTROL H
J01- 44	GND
J01- 45	BOOT ENAB L
J01- 46	MEMORY ENABLE (3) L
J01- 47	+5V
J01- 48	+5V
J01- 49	+5V
J01- 50	+5V
J01- 51	A18 H
J01- 54	GND
J01- 56	MEMORY BUSY (3) H
J01- 58	GND
J01- 59	DATA 15 H
J01- 60	DATA 13 H
J01- 61	BUS DCLO L
J01- 62	DATA 14 H
J01- 63	PARITY MSB H
J01- 64	A16 H
J01- 65	DATA 12 H
J01- 66	DATA 09 H
J01- 68	DATA 10 H
J01- 70	DATA 08 H
J01- 71	DATA 11 H
J01- 72	CSR CLEAR L
J01- 73	CSR INITIATE H
J01- 74	GND
J01- 75	BUS ACLO L
J01- 76	A07 H
J01- 79	DATA 08 H
J01- 80	DATA 09 H
J01- 81	DATA 10 H
J01- 82	DATA 11 H
J01- 83	A08 H
J01- 84	DATA 12 H
J01- 85	A09 H
J01- 86	DATA 13 H
J01- 87	A12 H
J01- 88	DATA 14 H
J01- 89	A13 H
J01- 90	DATA 15 H
J01- 91	All H
J01- 92	PARITY MSB H
J01- 93	A10 H
J01- 94	A15 H
J01- 95	GND
J01- 96	GND
J02-1	+5V
J02-2	+5V
J02- 19	+5V

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J02- 20	+5V
J02- 35	GND
J02- 36	GND
J02- 40	MEMLCK 1
J02- 41	MEMLCK 2
J02- 42	MEMLCK 3
J02- 43	MEMLCK 4
J02- 51	+5V
J02- 52	+5V
J02- 69	+5V
J02- 70	+5V
J02- 71	GND
J02- 72	GND
J02- 73	+5VBB
J02- 74	+5VBB
J02- 75	+5VBB
J02- 76	+5VBB
J02- 87	+5VBB
J02- 88	+5VBB
J02- 89	GND
J02- 90	GND
J02- 91	+5VBB
J02- 92	+5VBB
J02-105	GND
J02-106	GND
J02-119	+5VBB
J02-120	+5VBB
J02-121	GND
J02-122	GND
J02-123	+5VBB
J02-124	+5VBB
J02-132	+5VBB
J02-133	+5VBB
J02-134	+5VBB
J02-135	+5VBB
J02-139	GND
J02-140	GND
J03-1	GND
J03-2	GND
J03-3	AO1 H
J03-4	DATA 01 H
J03-5	A02 H
J03-6	DATA 00 H
J03-7	A03 H
J03-8	DATA 03 H
J03-9	A04 H
J03- 10	DATA 02 H
J03- 11	A05 H
J03- 12	DATA 05 H
J03- 13	A06 H
J03- 14	DATA 04 H
J03- 15	A14 H
J03- 16	DATA 00 H
J03- 17	DATA 07 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J03- 18	DATA 04 H
J03- 21	DATA RDY (2) L
J03- 22	GND
J03- 23	REF SYNC H
J03- 24	A17 H
J03- 25	DATA 06 H
J03- 26	PARITY LSB H
J03- 28	DATA 07 H
J03- 29	DATA 06 H
J03- 30	DATA 03 H
J03- 31	DATA 05 H
J03- 32	GND
J03- 33	LSB BYTE CONTROL H
J03- 34	DATA 02 H
J03- 35	CYCLE INIT H
J03- 36	GND
J03- 38	DATA 01 H
J03- 40	DATA OUT CONT (2)L
J03- 41	PARITY LSB H
J03- 42	GND
J03- 43	MSB BYTE CONTROL H
J03- 44	GND
J03- 45	BOOT ENAB L
J03- 46	MEMORY ENABLE (2) L
J03- 47	+5V
J03- 48	+5V
J03- 49	+5V
J03- 50	+5V
J03- 51	A18 H
J03- 54	GND
J03- 56	MEMORY BUSY (2) H
J03- 58	GND
J03- 59	DATA 15 H
J03- 60	DATA 13 H
J03- 61	BUS DCLO L
J03- 62	DATA 14 H
J03- 63	PARITY MSB H
J03- 64	A16 H
J03- 65	DATA 12 H
J03- 66	DATA 09 H
J03- 68	DATA 10 H
J03- 70	DATA 08 H
J03- 71	DATA 11 H
J03- 72	CSR CLEAR L
J03- 73	CSR INITIATE H
J03- 74	GND
J03- 75	BUS ACLO L
J03- 76	A07 H
J03- 79	DATA 08 H
J03- 80	DATA 09 H
J03- 81	DATA 10 H
J03- 82	DATA 11 H
J03- 83	A08 H
J03- 84	DATA 12 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J03- 85	A09 H
J03- 86	DATA 13 H
J03- 87	A12 H
J03- 88	DATA 14 H
J03- 89	A13 H
J03- 90	DATA 15 H
J03- 91	All H
J03- 92	PARITY MSB H
JC3- 93	A10 H
J03- 94	A15 H
J03- 95	GND
J03- 96	GND
J04-1	+5V
J04-2	+5V
J04- 19	+5V
J04- 20	+5V
J04- 35	GND
J04- 36	GND
J04- 40	MEMLCK 5
J04- 41	MEMLCK 6
J04- 42	MEMLCK 7
J04- 43	MEMLCK 8
J04- 51	+5V
J04- 52	+5V
J04- 69	+5V
J04- 70	+5V
J04- 71	GND
J04- 72	GND
J04- 73	+5VBB
J04- 74	+5VBB
J04- 75	+5VBB
J04- 76	+5VBB
J04- 87	+5VBB
J04- 88	+5VBB
J04- 89	GND
J04- 90	GND
J04- 91	+5VBB
J04- 92	+SVBB
J04-105	GND
J04-106	GND
J04-119	+5VBB
J04-120	+SVBB
J04-121	GND
J04-122	GND
J04-123	+5VBB
J04-124	+5VBB
J04-132	+5VBB
J04-133	+5VBB
J04-134	+5VBB
J04-135	+5VBB SENSE
J04-139	+5VBB SENSE RTN
J04-140	GND
J05-1	GND
J05-2	GND

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J05-3	A01 H
J05-4	DATA 01 H
J05-5	A02 H
J05-6	DATA 00 H
J05-7	A03 H
J05-8	DATA 03 H
J05-9	A04 H
J05- 10	DATA 02 H
J05- 11	A05 H
J05- 12	DATA 05 H
J05- 13	A06 H
J05- 14	DATA 04 H
J05- 15	A14 H
J05- 16	DATA 00 H
J05- 17	DATA 07 H
J05- 18	DATA 04 H
J05- 21	DATA RDY (1) L
J05- 22	GND
J05- 23	REF SYNC H
J05- 24	A17 H
J05- 25	DATA 06 H
J05- 26	PARITY LSB H
J05- 28	DATA 07 H
J05- 29	DATA 06 H
J05- 30	DATA 03 H
J05- 31	DATA 05 H
J05- 32	GND
J05- 33	LSB BYTE CONTROL H
J05- 34	DATA 02 H
J05- 35	CYCLE INIT H
J05- 36	GND
J05- 38	DATA 01 H
J05- 40	DATA OUT CONT (1)L
J05- 41	PARITY LSB H
J05- 42	GND
J05- 43	MSB BYTE CONTROL H-
J05- 44	GND
J05- 45	BOOT ENAB L
J05- 46	MEMORY ENABLE (1) L
J05- 47	+5V
J05- 48	+5V
J05- 49	+5V
J05- 50	+5V
J05- 51	A18 H
J05- 54	GND
J05- 56	MEMORY BUSY (1) H
J05- 58	GND
J05- 59	DATA 15 H
J05- 60	DATA 13 H
J05- 61	BUS DCLO L
J05- 62	DATA 14 H
J05- 63	PARITY MSB H
J05- 64	A16 H
J05- 65	DATA 12 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J05- 66	DATA 09 H
J05- 68	DATA 10 H
J05- 70	DATA 08 H
J05- 71	DATA 11 H
J05- 72	CSR CLEAR L
J05- 73	CSR INITIATE H
J05- 74	GND
J05- 75	BUS ACLO L
J05- 76	A07 H
J05- 79	DATA 08 H
J05- 80	DATA 09 H
J05- 81	DATA 10 H
J05- 82	DATA 11 H
J05- 83	A08 H
J05- 84	DATA 12 H
J05- 85	A09 H
J05- 86	DATA 13 H
J05- 87	A12 H
J05- 88	DATA 14 H
J05- 89	A13 H
J05- 90	DATA 15 H
J05- 91	AII H
J05- 92	PARITY MSB H
J05- 93	A10 H
J05- 94	A15 H
J05- 95	GND
J05- 96	GND
J06-1	+5V
J06-2	+5V
J06- 19	+5V
J06- 20	+5V
J06- 35	GND
J06- 36	GND
J06- 40	MEMLCK 9
J06- 41	MEMLCK 10
J06- 42	MEMLCK 11
J06- 43	MEMLCK 12
J06- 51	+5V
J06- 52	+5V
J06- 69	+5V
J06- 70	+5V
J06- 71	GND
J06- 72	GND
J06- 73	+5VBB
J06- 74	+5VBB
J06- 75	+5VBB
J06- 76	+5VBB
J06- 87	+5VBB
J06- 88	+5VBB
J06- 89	GND
J06- 90	GND
J06- 91	+5VBB
J06- 92	+5VBB
J06-105	GND

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J06-106	**GND**
J06-119	**+5VBB**
J06-120	**+5VBB**
J06-121	**GND**
J06-122	**GND**
J06-123	**+5VBB**
J06-124	**+5VBB**
J06-132	**+5VBB**
J06-133	**+5VBB**
J06-134	**+5VBB**
J06-135	**+5VBB SENSE**
J06-139	**+SVBB SENSE RTN**
J06-140	**GND**
J07-1	**+5V**
J07-2	**+5V**
J07-3	**EUB A18 L**
J07-4	**EUB A19 L**
J07-5	**EUB A20 L**
J07-6	**EUB A21 L**
J07- 15	**A19 H**
J07- 16	**EUB INIT L**
J07- 18	**BUS DCLO L**
J07- 19	**+5V**
J07- 20	**+5V**
J07- 21	**CSR CLEAR L**
J07- 23	**EUB AOO L**
J07- 24	**EUB A01 L**
J07- 25	**EUB A02 L**
J07- 26	**EUB A03 L**
J07- 27	**EUB A04 L**
J07- 28	**EUB A05 L**
J07- 29	**EUB A06 L**
J07- 30	**EUB A07 L**
J07- 31	**EUB A08 L**
J07- 32	**EU3 A09 L**
J07- 33	**EUB A10 L**
J07- 34	**EUB AII L**
J07- 35	**GND**
J07- 36	**GND**
J07- 37	**EUB A12 L**
J07- 38	**EUB A13 L**
J07- 39	**EUB A14 L**
J07- 40	**EUB A15 L**
J07- 41	**EUB A16 L**
J07- 42	**EUB A17 L**
J07- 43	**EUB CO L**
J07- 44	**EUB C1 L**
J07- 45	**EUB MSYN L**
J07- 48	**BUS PB L**
J07- 50	**EUB SSYN L**
J07- 51	**+5V**
J07- 52	**+5V**
J07- 53	**BUS DOO L**
J07- 54	**BUS D01 L**

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J07- 55	BUS D02 L
J07- 56	BUS D03 L
J07- 57	BUS D04 L
J07- 58	BUS D05 L
J07- 59	BUS D06 L
J07- 60	BUS D07 L
J07- 61	BUS D08 L
J07- 62	BUS D09 L
J07- 63	BUS D10 L
J07- 64	BUS DIl L
J07- 65	BUS D12 L
J07- 66	BUS D13 L
J07- 67	BUS D14 L
J07- 68	BUS D15 L
J07- 69	+5V
J07- 70	+5V
J07- 71	GND
J07- 72	GND
J07- 73	MEMORY BUSY (2) H
J07- 74	MEMORY BUSY (3) H
J07- 77	DATA RDY (1) L
J07- 78	DATA RDY (2) L
J07- 79	DATA RDY (3) L
J07- 81	DATA 00 H
J07- 83	A01 H
J07- 84	A02 H
J07- 85	A03 H
J07- 86	A04 H
J07- 87	A05 H
J07- 88	A06 H
J07- 89	GND
J07- 90	GND
J07- 91	A14 H
J07- 92	DATA 04 H
J07- 93	DATA 07 H
J07- 94	DATA 06 H
J07- 96	DATA 03 H
J07- 97	DATA 05 H
J07- 98	LSB BYTE CONTROL H
J07- 99	CYCLE INIT H
J07-100	DATA 01 H
J07-101	DATA 02 H
J07-102	PARITY LSB H
J07-103	MSB BYTE CONTROL H
J07-104	MEMORY ENABLE (1) L
J07-105	GND
J07-106	GND
J07-107	DATA OUT CONT (1)L
J07-108	CSR INITIATE H
J07-109	BUS DCLO L
J07-110	DATA 13 H
J07-111	DATA 15 H
J07-112	DATA 14 H
J07-113	PARITY MSB H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J07-114	DATA 12 H
J07-115	MEMORY BUSY (1) H
J07-116	DATA 10 H
J07-117	DATA 11 H
J07-118	DATA 08 H
J07-119	A07 H
J07-120	DATA 09 H
J07-121	GND
J07-122	GND
J07-123	A08 H
J07-124	A09 H
J07-125	A12 H
J07-126	A13 H
J07-127	All H
J07-128	A10 H
J07-129	A15 H
J07-130	A16 H
J07-131	A18 H
J07-132	A17 H
J07-134	MEMORY ENABLE 3) L
J07-135	MEMORY ENABLE 2) L
J07-137	DATA OUT CONT 3)L
J07-138	DATA OUT CONT 2 L
J07-139	GND
J07-140	GND
J08-1	+5V
J08-2	+5V
J08- 19	+5V
J08- 20	+5V
J08- 35	GND
J08- 36	GND
J08- 51	+5V
J08- 52	+5V
J08- 69	+5V
J08- 70	+5V
J08- 71	GND
J08- 72	GND
J08- 89	GND
J08- 90	GND
J08-105	GND
J08-106	GND
J08-121	GND
J08-122	GND
J08-136	+15V
J08-137	+15V
J08-138	-12V
J08-139	GND
J08-140	GND
J09-1	+5V
J09-2	+5V
J09-3	CHO TRXC L
J09-4	CHO TRXC H
J09-5	CH1 TRXC L
J09-6	CH1 TRXC H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J09-7	CH2 TRXC L
J09-8	CH2 TRXC H
J09-9	CH3 TRXC L
J09- 10	CH3 TRXC H
J09- 11	CHO CTS H
J09- 12	CH1 CTS H
J09- 13	CH2 CTS H
J09- 14	CH3 CTS H
J09- 15	BUS DIR
J09- 19	+5V
J09- 20	+5V
J09- 21	CTRL 16 MHZ
J09- 26	CHO RTXC L
J09- 27	CHO RTXC H
J09- 28	CH1 RTXC L
J09- 29	CH1 RTXC H
J09- 30	CH2 RTXC L
J09- 31	CH2 RTXC H
J309- 32	CH3 RTXC L
J09- 33	CH3 RTXC H
J09- 34	CHO RTS H
J09- 35	GND
J09- 36	GND
J09- 37	CH1 RTS H
J09- 38	CH2 RTS H
J09- 39	CH3 RTS H
J09- 44	CHO RTN
J09- 45	CH1 RTN
J09- 46	CH2 RTN
J09- 47	CH3 RTN
J09- 51	+5V
J09- 52	+5V
J09- 54	CHO CD H
J09- 55	CH1 CD H
J09- 56	CH2 CD
J09- 57	CH3 CD
JO9- 69	+5V
J09- 70	+5V
J09- 71	GND
J09- 72	GND
J09- 73	CTRL RESET
J09- 74	CTRL DTR
J09- 75	CTRL DEN
J09- 76	R/W
J09- 77	SMA14 DISC IN 0
J09- 78	SMA14 DISC IN 1
J09- 79	SMA14 DISC IN 2
J09- 80	SMA14 DISC IN 3
J09- 81	CTRL ALE
J09- 83	MCS 1 LCK
J09- 87	IOADBUS 00
J09- 88	IOADBUS 01
J09- 89	GND
J09- 90	GND

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J09- 91	IOADBUS 02
J09- 92	IOADBUS 03
J09- 93	IOADBUS 04
J09- 94	IOADBUS 05
J09- 95	IOADBUS 06
J09- 96	IOADBUS 07
J09- 97	IOADBUS 08
J09- 98	IOADBUS 09
J09- 99	IOADBUS 10
J09-100	IOADBUS 11
J09-101	IOADBUS 12
J09-102	IOADBUS 13
J09-103	IOADBUS 14
J09-104	IOADBUS 15
J09-105	GND
J09-106	GND
J09-107	LED 1
J09-109	CTRL WAIT 1
J09-110	CHO RXD L
J09-111	CH1 RXD L
J09-112	CH2 RXD L
J09-113	CH3 RXD L
J09-118	CHO TXD H
J09-119	CH1 TXD H
J09-120	CH2 TXD H
J09-121	GND
J09-122	GND
J09-123	CH3 TXD H
J09-128	CHO RXD H
J09-129	CH1 RXD H
J09-130	CH2 RXD H
J09-131	CH3 RXD H
J09-136	+15V
J09-137	+15V
J09-138	-12V
J09-139	GND
J09-140	GND
J10-1	+5V
J10-2	+5V
J10- 11	CTS-0
J10- 12	CTS-1
J10- 13	CTS-2
J10- 14	CTS-3
J10- 15	BUS DIR
J10- 19	+5V
J10- 20	+5V
J10- 21	CTRL 16 MHZ
J10- 22	CTS-4
J10- 23	CTS-5
J10- 24	CTS-6
J10- 25	CTS-7
J10- 34	RTS-0
J10- 35	GND
J10- 36	GND

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J10- 37	RTS-1
J10- 38	RTS-2
J10- 39	RTS-3
J10- 40	RTS-4
J10- 41	RTS-5
J10- 42	RTS-6
J10- 43	RTS-7
J10- 44	RTN-0
J10- 45	RTN-1
J10- 46	RTN-2
J10- 47	RTN-3
J10- 51	+5V
J10- 52	+5V
J10- 62	RTN-4
J10- 63	RTN-5
J10- 64	RTN-6
J10- 65	RTN-7
J10- 69	+5V
J10- 70	+5V
J10- 71	GND
J10- 72	GND
J10- 73	CTRL RESET
J10- 74	CTRL DTR
J10- 75	CTRL DEN
J10- 76	R/W
J10- 81	CTRL ALE
J10- 83	MCS 0 LCK
J10- 87	IOADBUS 00
J10- 88	IOADBUS 01
J10- 89	GND
J10- 90	GND
J10- 91	IOADBUS 02
J10- 92	IOADBUS 03
J10- 93	IOADBUS 04
J10- 94	IOADBUS 05
J10- 95	IOADBUS 06
J10- 96	IOADBUS 07
J10- 97	IOADBUS 08
J10- 98	IOADBUS 09
J10- 99	IOADBUS 10
J10-100	IOADBUS 11
J10-101	IOADBUS 12
J10-102	IOADBUS 13
J10-103	IOADBUS 14
J10-104	IOADBUS 15
J10-105	GND
J10-106	GND
J10-107	LED 0
J10-109	CTRL WAIT 0
J10-110	RXD-0
J10-111	RXD-1
J10-112	RXD-2
J10-113	RXD-3
J10-114	RXD-4

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J10-115	RXD-5
J10-116	RXD-6
J10-117	RXD-7
J10-118	TXD-O
J10-119	TXD-1
J10-120	TXD-2
J10-121	GND
J10-122	GND
J10-123	TXD-3
J10-124	TXD-4
J10-125	TXD-5
J10-126	TXD-6
J10-127	TXD-7
J10-128	RXDH-0
J10-129	RXDH-1
J10-130	RXDH-2
J10-131	RXDH-3
J10-132	RXDH-4
J10-133	RXDH-5
J10-134	RXDH-6
J10-135	RXDH-7
J10-136	+15V
J10-137	+15V
J10-138	-12V
J10-139	GND
J10-140	GND
Jll-1	+5V
J11-2	+5V
J11-3	BUS BR4 L
J11-4	BUS BR5 L
J11-5	BUS BR6 L
J11-6	BUS BR7 L
J11-7	BUS BG4 H (1)
J11-8	BUS BG5 H (1)
J11-9	BUS BG6 H (1)
J11- 10	BUS BG7 H (1)
J11- 11	BUS NPR L
J11- 12	BUS NPG H (1)
J11- 13	BUS SACK L
J11- 14	BUS BBSY L
J11- 15	BUS DIR
J11- 16	BUS INIT L
311- 17	BUS ACLO L
J11- 18	BUS DCLO L
J11- 19	+5V
J11- 20	+5V
J11- 21	CTRL 16 MHZ
J11- 23	BUS AOO L
J11- 24	BUS A01 L
J11- 25	BUS A02 L
J11- 26	BUS A03 L
J11- 27	BUS A04 L
J11- 28	BUS A05 L
J11- 29	BUS A06 L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J11- 30	BUS A07 L
J11- 31	BUS A08 L
J11- 32	BUS A09 L
J11- 33	BUS A10 L
J11- 34	BUS AII L
J11- 35	GND
J11- 36	GND
J11- 37	BUS A12 L
J11- 38	BUS A13 L
J11- 39	BUS A14 L
J11- 40	BUS A15 L
J11- 41	BUS A16 L
J11- 42	BUS A17 L
J11- 43	BUS CO L
J11- 44	BUS C1 L
J11- 45	BUS MSYN L
J11- 46	BUS SSYN L
J11- 47	BUS PA L
J11- 48	BUS PB L
J11- 49	BUS INTR L
J11- 50	CCA10 DISC 07 OUT
J11- 51	+5v
J11- 52	+5V
J11- 53	BUS DOO L
J11- 54	BUS D01 L
J11- 55	BUS D02 L
J11- 56	BUS D03 L
J11- 57	BUS D04 L
J11- 58	BUS D05 L
J11- 59	BUS D06 L
J11- 60	BUS D07 L
J11- 61	BUS D08 L
J11- 62	BUS D09 L
J11- 63	BUS D10 L
J11- 64	BUS D11 L
J11- 65	BUS D12 L
J11- 66	BUS D13 L
J11- 67	BUS D14 L
J11- 68	BUS D15 L
J11- 69	+5V
J11- 70	+5V
J11- 71	GND
J11- 72	GND
J11- 73	CTRL RESET
J11- 74	CTRL DTR
J11- 75	CTRL DEN
J11- 76	R/W
J11- 77	BUS BG4 H (2)
J11- 78	BUS BG5 H (2)
J11- 79	BUS BG6 H (2
J11- 80	BUS BG7 H (2 ---
J11- 81	CTRL ALE
J11- 82	BUS NPG H (2)
J11- 83	MCS 0 LCK

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J11- 84	MCS 1 LCK
J11- 87	IOADBUS 00
J11- 88	IOADBUS 01
J11- 89	GND
J11- 90	GND
J11- 91	IOADBUS 02
J11- 92	IOADBUS 03
J11- 93	IOADBUS 04
J11- 94	IOADBUS 05
J11- 95	IOADBUS 06
J11- 96	IOADBUS 07
J11- 97	IOADBUS 08
J11- 98	IOADBUS 09
J11- 99	IOADBUS 10
JI1-100	IOADBUS 11
J11 101	IOADBUS 12
J11-102	IOADBUS 13
J11-103	IOADBUS 14
J11-104	IOADBUS 15
J11-105	GND
J11-106	GND
J11-108	GND
JI1-109	GND
J11-110	GND
JI1-111	LED 0
J11-112	LED 1
J11-115	CTRL WAIT 0
J11-116	CTRL WAIT 1
JI1-119	DISCOUT 0
J11-121	GND
J11-122	GND
J11-123	DISCOUT 2
J11-124	DISCOUT 3
J11-125	CCA10 DISC 04 OUT
J11-126	CCA10 DISC 05 OUT
J11-127	DISCIN-0
J11-128	DISCIN-1
JI1-129	DISCIN-2
J11-130	DISCIN-3
JI1-135	CCA10 DISC 06 OUT
JI1-136	+15V
JI1-137	+15V
J11-138	-12V
J11-139	GND
J11-140	GND
J12-1	+5V
J12-2	+5V
J12-4	CPU DATO L
J12-6	BYTE H
J12-7	UBI BG4 H
J12-8	BUS BG5 H (1)
J12-9	UBI BG6 H
J12- 10	BUS BG7 H (1)
J12- 11	BUS NPR L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J12- 12	BUS NPG H (1)
J12- 13	BUS SACK L
J12- 14	BUS BBSY L
J12- 15	PFAIL BR PEND H
J12- 16	INHIBIT L
J12- 17	CPU HLT RQST L
J12- 18	RESET (1) H
J12- 19	+5V
J12- 20	+5V
J12- 21	EXT CLK C L
J12- 22	PROC INIT L
J12- 23	BUS AOO L
J12- 24	BUS A01 L
J12- 25	BUS A02 L
J12- 26	BUS A03 L
J12- 27	BUS A04 L
J12- 28	BUS A05 L
J12- 29	BUS A06 L
J12- 30	BUS A07 L
J12- 31	BUS A08 L
J12- 32	BUS A09 L
J12- 33	BUS A10 L
J12- 34	BUS All L
J12- 35	GND
J12- 36	GND
J12- 37	BUS A12 L
J12- 38	BUS A13 L
J12- 39	START RESET H
J12- 40	TAKE BUS H
J12- 41	MFM CLK INH L
J12- 42	CPU MSYN (1) H
J12- 43	BUS CO L
J12- 44	BUS Cl L
J12- 45	BUS MSYN L
J12- 46	BUS SSYN L
J12- 47	BUS PA L
J12- 48	BUS PB L
J12- 49	BUS INTR L
J12- 50	EXT TAP 30 H
J12- 51	+5v
J12- 52	+5V
J12- 53	CACHE PE INTR L
J12- 54	RST INST H
J12- 55	CACHE GATE H
J12- 56	UPPER 128K L
J12- 57	RCD INIT L
J12- 58	STROBE CACHE H
J12- 59	CACHE RESTART L
J12- 60	START TRAN L
J12- 61	ENAB ADRS H
J12- 62	UBUS CO (1) H
J12- 63	UBUS Cl (1) H
J12- 64	PSW 05 (1) H
J12- 65	PSW 06 (1) H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J12- 66	PSW 07 (1) H
J12- 67	P1A 1 H
J12- 68	P1A 2 H
J12- 69	+5V
J12- 70	+SV
J12- 71	GND
J12- 72	GND
J12- 73	PAX AOO H
J12- 74	PAX AO1 H
J12- 75	PAX A02 H
J12- 76	PAX A03 H
J12- 77	PAX A04 H
J12- 78	PAX A05 H
J12- 79	PAX A06 H
J12- 80	PAX A07 H
J12- 81	PAX A08 H
J12- 82	PAX A09 H
J12- 83	PAX A10 H
J12- 84	PAX All H
J12- 85	PAX A12 H
J12- 86	PAX A13 H
J12- 87	PAX CO H
J12- 88	PAX Cl H
J12- 89	GND
J12- 90	GND
J12- 91	BUF C1 (1) H
J12- 92	BUF CO (1) H
J12- 93	EUB AOO L
J12- 94	EUB A01 L
J12- 95	EUB A02 L
J12- 96	EUB A03 L
J12- 97	EUB A04 L
J12- 98	EUB A05 L
J12- 99	EUB A06 L
J12-100	EUB A07 L
J12-101	EUB A08 L
J12-102	EUB A09 L
J12-103	EUB A10 L
J12-104	EUB All L
J12-105	GND
J12-106	GND
J12-107	EUB A12 L
J12-108	EUB A13 L
J12-109	KT FAULT L
J12-110	START TRAN H
J12-111	CIS ENAB L
J12-112	BUF DATA TRAN (1) H
J12-113	EUB CO L
J12-114	EUB C1 L
J12-115	EUB MSYN L
J12-116	EUB SSYN L
J12-117	PAX SSYN L
J12-118	KTE (1) H
J12-119	PAX INTR L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J12-120	PFAIL H
J12-121	GND
J12-122	GND
J12-124	CLR MPC L
J12-125	FAULT H
J12-126	ALLOW MSYN H
J12-127	CPU HLT (1) H
J12-128	PE (1) H
J12-129	PFAIL (1) H
J12-130	PE+BG+PIRQ+HLT+PFAIL H
J12-131	HLT GRANT H
J12-132	PIRQ GRANT L
J12-133	BUT SERVICE (1) H
J12-134	BE (1) H
J12-135	P1A 0 H
J12-136	SET BE L
J12-137	ENAB GRANTS H
J12-138	DISABLE MSYN L
J12-139	GND
J12-140	GND
J13-1	+5V
J13-2	+5V
J13-3	BUS BR4 L
J13-4	BUS BR5 L
J13-5	BUS BR6 L
J13-6	BUS BR7 L
J13- 11	ABORT H
J13- 19	+5V
J13- 20	+5V
J13- 22	FREE BUS H
J13- 23	DISABLE W BIT L
J13- 25	FORCE BUS DATA L
J13- 27	MFM HLT RQST L
J13- 29	TO (1) L
J13- 33	EMAP H
J13- 35	GND
J13- 36	GND
J13- 39	BUS A14 L
J13- 40	BUS A15 L
J13- 41	BUS A16 L
J13- 42	BUS A17 L
J13- 43	END TRAN TO MFM L
J13- 44	BA17 H
J13- 50	BUS STATUS ENAB L
J13- 51	+5V
J13- 52	+5V
J13- 53	BUS DOO L
J13- 54	BUS DO1 L
J13- 55	BUS D02 L
J13- 56	BUS D03 L
J13- 57	BUS D04 L
J13- 58	BUS D05 L
J13- 59	BUS D06 L
J13- 60	BUS D07 L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J13- 61	BUS D08 L
J13- 62	BUS D09 L
J13- 63	BUS D10 L
J13- 64	BUS D11 L
J13- 65	BUS D12 L
J13- 66	BUS D13 L
J13- 67	BUS D14 L
J13- 68	BUS D15 L
J13- 69	+5V
J13- 70	+5V
J13- 71	GND
J13- 72	GND
J13- 73	EUB A18 L
J13- 74	EUB A19 L
J13- 75	EUB A20 L
J13- 76	EUB A21 L
J13- 77	PAX A14 H
J13- 78	PAX A15 H
J13- 79	PAX A16 H
J13- 80	PAX A17 H
J13- 81	PAX A18 H
J13- 82	PAX A19 H
J13- 83	PAX A20 H
J13- 84	PAX A21 H
J13- 89	GND
J13- 90	GND
J13- 93	EUB AOO L
J13- 94	EUB A01 L
J13- 95	EUB A02 L
J13- 96	EUB A03 L
J13- 97	EUB A04 L
J13- 98	EUB A05 L
J13- 99	EUB A06 L
J13-100	EUB A07 L
J13-101	EUB A08 L
J13-102	EUB A09 L
J13-103	EUB A10 L
J13-104	EUB All L
J13-105	GND
J13-106	GND
J13-107	EUB A12 L
J13-108	EUB A13 L
J13-109	EUB A14 L
J13-110	EUB A15 L
J13-111	EUB A16 L
J13-112	EUB A17 L
J13-113	EUB CO L
J13-114	EUB C1 L
J13-121	GND
J13-122	GND
J13-123	PAX DOO H
J13-124	PAX DO1 H
J13-125	PAX D02 H
J13-126	PAX D03 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J13-127	PAX D04 H
J13-128	PAX D05 H
J13-129	PAX D06 H
J13-130	PAX D07 H
J13-131	PAX D08 H
J13-132	PAX D09 H
J13-133	PAX D10 H
J13-134	PAX D11 H
J13-135	PAX D12 H
J13-136	PAX D13 H
J13-137	PAX D14 H
J13-138	PAX D15 H
J13-139	GND
J13-140	GND
J14-1	+5V
J14-2	+5V
J14- 19	+5V
J14- 20	+5V
J14- 22	PROC INIT L
J14- 35	GND
J14- 36	GND
J14- 51	+5V
J14- 52	+5V
J14- 58	STROBE CACHE H
J14- 59	CACHE RESTART L
J14- 61	ENAB ADRS H
J14- 69	+5V
J14- 70	+5V
J14- 71	GND
J14- 72	GND
J14- 86	ENAB MAINT (1) H
J14- 89	GND
J14- 90	GND
J14-101	CACHE GR TP2
J14-103	CACHE GR TP1
J14-105	GND
J14-106	GND
J14-121	GND
J14-122	GND
J14-125	FAULT H
J14-139	GND
J14-140	GND
J15-1	+5V
J15-2	+5V
J15-3	PAX AOO H
J15-4	PAX A01 H
J15-5	PAX A02 H
J15-6	PAX A03 H
J15-7	PAX A04 H
J15-8	PAX A05 H
J15-9	PAX A06 H
J15- 10	PAX A07 H
J15- 11	PAX A08 H
J15- 12	PAX A09 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J15- 13	PAX A10 H
J15- 14	PAX AII H
J15- 15	PAX A12 H
J15- 16	PAX A13 H
J15- 17	CPU HLT RQST L
J15- 18	FORCE CACHE DATA L
J15- 19	+5V
J15- 20	+5V
J15- 30	EXT CLK A L
J15- 31	MAN CLK ENAB L
J15- 35	GND
J15- 36	GND
J15- 48	BUS PB L
J15- 51	+5v
J15- 52	+5V
J15- 53	CACHE PE INTR L
J15- 55	CACHE GATE H
J15- 56	UPPER 128K L
J15- 58	STROBE CACHE H
J15- 60	START TRAN L
J15- 61	ENAB ADRS H
J15- 64	CACHE MATCH L (TP)
J15- 69	+SV
J15- 70	+5V
J15- 71	GND
J15- 72	GND
J15- 73	EUB A18 L
J15- 74	EUB A19 L
J15- 75	EUB A20 L
J15- 76	EUB A21 L
J15- 77	PAX A14 H
J15- 78	PAX A15 H
J15- 79	PAX A16 H
J15- 80	PAX A17 H
J15- 81	PAX A18 H
J15- 82	PAX A19 H
J15- 83	PAX A20 H
J15- 84	PAX A21 H
J15- 85	CACHE BYPASS L
J15- 89	GND
J15- 90	GND
J15- 91	BUF C1 (1) H
J15- 92	FREE BUS H
J15- 93	EUB AOO L
J15- 94	EUB A01 L
J15- 95	EUB A02 L
J15- 96	EUB A03 L
J15- 97	EUB A04 L
J15- 98	EUB A05 L
J15- 99	EUB A06 L
J15-100	EUB A07 L
J15-101	EUB A08 L
J15-102	EUB A09 L
J15-103	EUB A10 L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J15-104	EUB All L
J15-105	GND
J15-106	GND
J15-107	EUB A12 L
J15-108	EUB A13 L
J15-109	EUB A14 L
J15-110	EUB A15 L
J15-111	EUB A16 L
J15-112	EUB A17 L
J15-113	EUB CO L
J15-114	EUB C1 L
J15-115	EUB MSYN L
J15-116	EUB SSYN L
J15-117	PAX SSYN L
J15-121	GND
J15-122	GND
J15-123	PAX DOO H
J15-124	PAX D01 H
J15-125	PAX D02 H
J15-126	PAX D03 H
J15-127	PAX D04 H
J15-128	PAX D05 H
J15-129	PAX D06 H
J15-130	PAX D07 H
J15-131	PAX D08 H
J15-132	PAX D09 H
J15-133	PAX D10 H
J15-134	PAX D11 H
J15-135	PAX D12 H
J15-136	PAX D13 H
J15-137	PAX D14 H
J15-138	PAX D15 H
J15-139	GND
J15-140	GND
J16-1	+5V
J16-2	+5V
J16-3	LOAD PARH L (TP)
J16-4	LOAD PARL L (TP)
J16-5	LOAD PDRH L (TP)
J16-6	LOAD PDRL L (TP)
J16-7	PAX' A14 H
J16-8	PAX A15 H
J16-9	PAX A16 H
J16- 10	PAX A17 H
J16- 11	PAX A18 H
J16- 12	PAX A19 H
J16- 13	PAX A20 H
J16- 14	PAX A21 H
J16- 15	CACHE BYPASS L
J16- 16	ENAB MAINT (1) H
J16- 17	KT MUX SO L (TP)
J16- 19	+5V
J16- 20	+5V
J16- 23	DISABLE W BIT L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J16- 27	LOAD SROH L (TP)
J16- 30	ENAB INT REG L
J16- 31	STATUS REG SO L
J16- 32	TRAN TO MFM L
J16- 33	STATUS REG S1 L
J16- 34	LOAD BAR H
J16- 35	GND
J16- 36	GND
J16- 37	INTR H
J16- 38	LOAD VBA H
J16- 39	RELOCATE H
J16- 40	MODE 00 H
J16- 41	READ SR2 L (TP)
J16- 42	CPU MSYN (1) H
J16- 43	END TRAN TO MFM L
J16- 44	EXT CLK B3 L
J16- 46	INT SSYN L (TP)
J16- 47	LOAD SR3 L
J16- 50	ENAB KT MUX L (TP)
J16- 51	+5v
J16- 52	+5V
J16- 53	MODE 01 H
J16- 54	PAR+PDR L (TP)
J16- 57	RCD INIT L
J16- 62	UBUS CO (1) H
J16- 63	UBUS CI (1) H
J16- 67	ERROR H
J16- 69	+5V
J16- 70	+5V
J16- 71	GND
J16- 72	GND
J16- 73	PAX AOO H
J16- 74	PAX A01 H
J16- 75	PAX A02 H
J16- 76	PAX A03 H
J16- 77	PAX A04 H
J16- 78	PAX A05 H
J16- 79	PAX A06 H
J16- 80	PAX A07 H
J16- 81	PAX A08 H
J16- 82	PAX A09 H
J16- 83	PAX A10O H
J16- 84	PAX AII H
J16- 85	PAX A12 H
J16- 86	PAX A13 H
J16- 87	PAX CO H
J16- 88	PAX CI H
J16- 89	GND
J16- 90	GND
J16- 97	SR SEL L
J16-100	PAGE FAULT H
J16-103	UPPER 128K L
J16-104	KT DISABLE MSYN L
J16-105	GND

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J16-106	GND
J16-109	KT FAULT L
J16-110	E22 BITS H
J16-111	FORCE KERNEL (1) H
J16-112	BUF DATA TRAN (1) H
J16-113	CLEAR ERROR L
J16-117	PAX SSYN L
J16-121	GND
J16-122	GND
J16-125	VBA 00 (1) H
J16-131	D SPACE H
J16-135	PREVIOUS MODE (1) L
J16-137	LOAD PIRH L
J16-139	GND
J16-140	GND
J17-1	+5V
J17-2	+5V
J17-3	CC CODE 01 H
J17-4	CPU DATO L
J17-5	V BIT (1) H
J17-6	LOAD CC L
J17-7	Z BIT (1) H
J17-8	N BIT (1 H
J17-9	P.C. USER H
J17- 10	BREG 15 (1) H
J17- 11	BREG 14 (1) H
J17- 12	C BIT (1) H
J17- 13	CC CODE 02 H
J17- 14	MPC 01 L
J17- 15	BYTE L
J17- 16	TRI STATE AMUX L
J17- 17	ENAB OVX L
J17- 19	+5V
J17- 20	+5V
J17- 21	UPPER BYTE L
J17- 22	PROC INIT L
J17- 23	PSW 15 (1) H
J17- 24	PSW 14 (1) H
J17- 25	EXT CLK B1 L
J17- 26	AMUX 00 H
J17- 27	AMUX 01 H
J17- 28	AMUX 02 H
J17- 29	BUT Z BIT H
J17- 30	AMUX 03 H
J17- 31	AMUX 04 H
J17- 32	AMUX 05 H
J17- 33	AMUX S1 (1) L
J17- 35	GND
J17- 36	GND
J17- 37	AMUX 06 H
J17- 38	AMUX 07 H
J17- 39	AMUX 08 H
J17- 40	AMUX 09 H
J17- 41	SERIAL SHIFT H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J17- 42	FORCE CPU DATA L
J17- 43	FORCE SS DATA L
J17- 45	SPA 00 H
J17- 46	SPA 01 H
J17- 47	SPA 02 H
J17- 48	SPA 03 H
J17- 49	DP BLEG 00 H
J17- 50	DP BLEG 01 H
J17- 51	+5V
J17- 52	+5V
J17- 53	INT VECTOR L
J17- 54	C6 H
J17- 55	C1 H
J17- 56	C2 H
J17- 57	C3 H
J17- 58	C4 H
J17- 59	C5-C7 H
J17- 60	START TRAN L
J17- 61	BX REG 01(1) H
J17- 62	BX REG 00(1) H
J17- 63	UBUS CI (1) H
J17- 64	PSW 05 (1 H
J17- 65	PSW 06 (1 H
J17- 66	PSW 07 (1) H
J17- 68	B REG 00(1) H
J17- 69	+5V
J17- 70	+5V
J17- 71	GND
J17- 72	GND
J17- 73	LOAD IR L
J17- 74	BLEG 01 H
J17- 75	BLEG 00 H
J17- 76	DISABLE LOAD PSW H
J17- 77	ALU CIN L
J17- 78	ALU MODE H
J17- 79	B MODE 01 L
J17- 80	B MODE 00 L
J17- 81	BX MODE 00 L
J17- 82	BX MODE 01 L
J17- 83	SWAP H
J17- 84	SEX H
J17- 85	SHIFT MUX 00 L
J17- 87	CC CODE 00 H
J17- 88	LOAD PSW L
J17- 89	GND
J17- 90	GND
J17- 91	ROT C BIT (1) H
J17- 92	FREE BUS H
J17- 93	AMUX 10 H
J17- 94	AMUX 11 H
J17- 95	AMUX 12 H
J17- 96	AMUX 13 H
J17- 97	AMUX 14 H
J17- 98	AMUX 15 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J17- 99	ALU COUT H
J17-100	AUX CONTROL L
J17-101	PLUS ONE H
J17-102	AMUX SO (1) L
J17-103	SHIFT MUX 01 L
J17-104	8-15-0 L
J17-105	GND
J17-106	GND
J17-107	CC N H
J17-108	ALU SO H
J17-109	ALU S1 H
J17-110	T BIT (1) H
J17-111	FORCE KERNEL (1) H
J17-113	SP WRITE H
J17-114	EXT CLK B2 L
J17-115	DP BLEG 02 H
J17-116	DP BLEG 03 H
J17-118	ALU S2 H
J17-119	ALU S3 H
J17-120	EXT TAP 30 H
J17-121	GND
J17-122	GND
J17-123	PAX DOO H
J17-124	PAX DO1 H
J17-125	PAX D02 H
J17-126	PAX D03 H
J17-127	PAX D04 H
J17-128	PAX D05 H
J17-129	PAX D06 H
J17-130	PAX D07 H
J17-131	PAX D08 H
J17-132	PAX D09 H
J17-133	PAX D10 H
J17-134	PAX D11 H
J17-135	PAX D12 H
J17-136	PAX D13 H
J17-137	PAX D14 H
J17-138	PAX D15 H
J17-139	GND
J17-140	GND
J18-1	+5V
J18-2	+5V
J18-3	LOAD IR L
J18-4	BLEG 01 H
J18-5	BLEG 00 H
J18-6	BYTE H
J18-7	LOAD CC L
J18-8	SHIFT MUX 01 L
J18-9	ALU S2 H
J18- 10	MAN CLK L
J18- 11	B REG 00(1) H
J18- 12	C BIT (1) H
J18- 13	MPC 00 L
J18- 14	MPC 01 L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J18- 15	BYTE L
J18- 16	INHIBIT L
J18- 18	BUS DCLO L
J18- 19	+5V
J18- 20	+5v
J18- 21	EXT CLK C L
J18- 22	UPPER BYTE L
J18- 23	PSW 15 (1) H
J18- 24	PSW 14 (1) H
J18- 25	EXT CLK B1 L
J18- 26	MPC 08 L
J18- 27	MPC 09 L
J18- 28	MPC 10 L
J18- 29	BX REG 01(1) H
J18- 30	EXT CLK A L
J18- 31	MAN CLK ENAB L
J18- 32	TRAN TO MFM L
J18- 33	AMUX S1 (1) L
J18- 34	LOAD BAR H
J18- 35	GND
J18- 36	GND
J18- 37	INTR H
J18- 38	LOAD VBA H
J18- 39	RELOCATE H
J18- 40	MODE 00 H
J18- 41	SERIAL SHIFT H
J18- 42	T'BIT (1) H
J18- 43	EXT TAP 90 L
J18- 44	EXT CLK B3 L
J18- 45	SPA 00 H
J18- 46	SPA 01 H
J18- 47	SPA 02 H
J18- 48	SPA 03 H
J18- 49	PAX INTR L
J18- 50	EXT TAP 30 H
J18- 51	+5V
J18- 52	+5v
J18- 53	MODE 01 H
J18- 54	C6 H
J18- 56	C2 H
J18- 57	C3 H
J18- 58	C4 H
J18- 59	C5-C7 H
J18- 60	CACHE RESTART L
J18- 61	BUF CO (1) H
J18- 62	BUT Z BIT H
J18- 63	BUT SERVICE (1) H
J18- 64	BE (1) H
J18- 65	FORCE KERNEL (1) H
J18- 68	DISABLE MSYN L
J18- 69	+5V
J18- 70	+5V
J18- 71	GND
J18- 72	GND

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J18- 73	PAX AOO H
J18- 74	PAX AO1 H
J18- 75	PAX A02 H
J18- 76	PAX A03 H
J18- 77	ALU CIN L
J18- 78	ALU MODE H
J18- 79	B MODE 01 L
J18- 80	B MODE 00 L
J18- 81	BX MODE 00 L
J18- 82	BX MODE 01 L
J18- 83	SWAP H
J18- 84	SEX H
J18- 85	SHIFT MUX 00 L
J18- 86	ENAB MAINT (1) H
J18- 87	ENAB OVX L
J18- 88	LOAD PSW L
J18- 89	GND
J18- 90	GND
J18- 91	BUF CI (1) H
J18- 92	BX REG 00(1) H
J18- 93	MPC 02 L
J18- 94	MPC 03 L
J18- 95	MPC 04 L
J18- 96	MPC 05 L
J18- 97	MPC 06 L
J18- 98	MPC 07 L
J18- 99	ALU COUT H
J18-100	CI H
J18-101	PLUS ONE H
J18-102	AMUX SO (1) L
J18-104	KT DISABLE MSYN L
J18-105	GND
J18-106	GND
J18-107	CC N H
J18-108	ALU SO H
J18-109	ALU S1 H
J18-110	START TRAN H
J18-112	BUF DATA TRAN (1) H
J18-113	SP WRITE H
J18-114	EXT CLK B2 L
J18-115	DCLO H
J18-116	CLK TP
J18-117	CLK EB TP
J18-118	ABORT H
J18-119	ALU 53 H
J18-120	CLK OSC
J18-121	GND
J18-122	GND
J18-123	INT VECTOR L
J18-124	CLR MPC L
J18-125	VBA 00 (1) H --
J18-126	ALLOW MSYN H
J18-127	CPU HLT (1) H
J18-128	AUX CONTROL L

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J18-129	PFAIL (1) H
J18-131	D SPACE H
J18-132	PIRQ GRANT L
J18-135	PREVIOUS MODE (1) L
J18-136	SET BE L
J18-137	ENAB GRANTS H
J18-139	GND
J18-140	GND
J19-1	+5V
J19-2	+5V
J19-3	CC CODE 01 H
J19-5	V BIT (1) H
J19-6	BYTE H
J19-7	Z BIT (1) H
J19-8	N BIT (1) H
J19-9	P.C. USER H
J19- 10	BREG 15 (1) H
J19- 11	BREG 14 (1) H
J19- 12	C BIT (1) H
J19- 13	MPC 00 L
J19- 14	MPC 01 L
J19- 15	BYTE L
J19- 16	BUS INIT L
J19- 17	BUS ACLO L
J19- 18	RESET (1) H
J19- 19	+5V
J19- 20	+5V
J19- 21	ROT C BIT (1) H
J19- 22	PROC INIT L
J19- 23	PSW 15 (1) H
J19- 24	PSW 14 (1) H
J19- 25	EXIT CONSOLE L
J19- 26	LOAD PIRH L
J19- 27	PE+BG+PIRQ+HLT+PFAIL H
J19- 29	TO (1) L
J19- 30	ENAB INT REG L
J19- 31	STATUS REG SO L
J19- 32	TRAN TO MFM L
J19- 34	STATUS REG S1 L
J19- 35	GND
J19- 36	GND
J19- 37	INTR H
J19- 38	BUS STATUS ENAB L
J19- 39	START RESET H
J19- 40	TAKE BUS H
J19- 41	CIS ENAB L
J19- 42	CLEAR ERROR L
J19- 43	END TRAN TO MFM L
J19- 44	BA17 H
J19- 45	SPA 00 H
J19- 46	SPA 01 H
J19- 47	SPA 02 H
J19- 48	ABORT H
J19- 49	DP BLEG 00 H

Backplane Node List

Sorted by Connector Number

Connector Pin Number	Signal Name
J319- 50	DP BLEG 01 H
J19- 51	+5V
J19- 52	+5V
J19- 55	POWER FAILURE H
J19- 57	RCD INIT L
J19- 58	PE (1) H
J19- 59	CACHE RESTART L
J19- 61	MFM LOAD MPC L
J19- 63	FORCE CPU MPC L
J19- 64	BE (1) H
J19- 68	DISABLE MSYN L
J19- 69	+5V
J19- 70	+5V
J19- 71	GND
J19- 72	GND
J19- 73	LOAD IR L
J19- 74	BLEG 01 H
J19- 75	BLEG 00 H
J19- 76	DISABLE LOAD PSW H
J19- 77	ALU CIN L
J19- 78	ALU MODE H
J19- 80	DCLO H
J19- 82	BOOT H
J19- 83	CC CODE 02 H
J19- 84	FP11F ATTACHED L
J19- 85	CACHE BYPASS L
J19- 86	ENAB MAINT (1) H
J19- 87	CPU HLT RQST L
J19- 88	CC CODE 00 H
J19- 89	GND
J19- 90	GND
J19- 91	BUF CI (1) H
J19- 92	FREE BUS H
J19- 93	MPC 02 L
J19- 94	MPC 03 L
J19- 95	MPC 04 L
J19- 96	MPC 05 L
J19- 97	MPC 06 L
J19- 98	MPC 07 L
J19- 99	BOOT ENAB L
J19-100	PFAIL H
J19-103	UPPER 128K L
J19-104	8-15-0 L
J19-105	GND
J19-106	GND
J19-107	P1A 0 H
J19-108	P1A 1 H
J19-109	P1A 2 H
J19-110	E22 BITS H
J19-111	EUB INIT L --
J19-112	BUF DATA TRAN (1) H
J19-113	ERROR H
J19-114	EMAP H
J19-115	DP BLEG 02 H

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J19-116	DP BLEG 03 H
J19-117	LOAD SR3 L
J19-118	KTE (1) H
J19-119	ALU S3 H
J19-121	GND
J19-122	GND
J19-123	PAX D00 H
J19-124	PAX D01 H
319-125	PAX D02 H
J19-126	PAX D03 H
J19-127	PAX D04 H
J19-128	PAX D05 H
J19-129	PAX D06 H
J19-130	PAX D07 H
J19-131	PAX D08 H
J19-132	PAX D09 H
J19-133	PAX D10 H
J19-134	PAX D11 H
J19-135	PAX D12 H
J19-136	PAX D13 H
J19-137	PAX D14 H
J19-138	PAX D15 H
J19-139	GND
J19-140	GND
J20-1	+5v
J20-2	+5v
J20-3	BUS BR4 L
J20-5	BUS BR6 L
J20-6	PULLUP A
J20-7	PAX A14 H
J20-8	PAX A15 H
J20-9	PAX A16 H
J20- 10	PAX A17 H
J20- 11	PAX A18 H
J20- 12	PAX A19 H
J20- 13	PAX A20 H
J20- 14	PAX A21 H
J20- 15	UBI BG4 H
J20- 16	UBI BG6 H
J20- 17	BUS SACK L
J20- 18	FORCE CACHE DATA L
J20- 19	+5V
J20- 20	+5V
J20- 21	BUS INIT L
J20- 22	GR TEST
J20- 25	EXIT CONSOLE L
320- 32	CPU MSYN (1) H
J20- 33	HALT H
J20- 35	GND
J20- 36	GND
J20- 42	FORCE CPU DATA L
J20- 44	FORCE SS DATA L
J20- 49	FORCE BUS DATA L
J20- 50	BUS STATUS ENAB L

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J20- 51	+5V
J20- 52	+5V
J20- 55	BUS BG4 H (1)
J20- 56	BUS BG6 H (1)
J20- 61	MFM LOAD MPC L
J20- 63	FORCE CPU MPC L
J20- 64	FORCE CIS DATA L
J20- 65	FORCE CPC L
J20- 67	FORCE FPP DATA L
J20- 69	+5V
J20- 70	+5V
J20- 71	GND
J20- 72	GND
J20- 73	PAX A00 H
J20- 74	PAX A01 H
J20- 75	PAX A02 H
J20- 76	PAX A03 H
J20- 77	PAX A04 H
J20- 78	PAX A05 H
J20- 79	PAX A06 H
J20- 80	PAX A07 H
J20- 81	PAX A08 H
J20- 82	PAX A09 H
J20- 83	PAX A10 H
J20- 84	PAX A11 H
J20- 85	PAX A12 H
J20- 86	PAX A13 H
J20- 87	PAX C0 H
J20- 88	PAX C1 H
J20- 89	GND
J20- 90	GND
J20- 94	RUN H
J20-105	GND
J20-106	GND
J20-115	DCL0 H
J20-117	PAX SSYN L
J20-119	PAX INTR L
J20-120	EXT TAP 30 H
J20-121	GND
J20-122	GND
J20-123	PAX DOO H
J20-124	PAX D01 H
J20-125	PAX D02 H
J20-126	PAX D03 H
J20-127	PAX D04 H
J20-128	PAX D05 H
J20-129	PAX D06 H
J20-130	PAX D07 H
J20-131	PAX D08 H
J20-132	PAX D09 H
J20-133	PAX D10 H
J20-134	PAX D11 H
J20-135	PAX D12 H
J20-136	PAX D13 H

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J20-137	PAX D14 H
J20-138	PAX D15 H
J20-139	GND
J20-140	GND
J21-1	+5V
J21-2	+5V
J21-4	CPU DATO L
J21-6	PULLUP A
J21- 10	MAN CLK L
J21- 11	LTC
J21- 17	CPU HLT RQST L
J21- 19	+5V
J21- 20	+5V
J21- 22	PROC INIT L
J21- 23	614.4KHZ
J21- 27	MFM HLT RQST L
J21- 30	EXT CLK A L
J21- 31	MAN CLK ENAB L
J21- 32	TRAN TO MFM L
J21- 34	HALT H
J21- 35	GND
J21- 36	GND
J21- 41	MFM CLK INH L
J21- 43	END TRAN TO MFM L
J21- 51	+5V
J21- 52	+5V
J21- 60	EXIT CONSOLE L
J21- 61	CPU ENAB ADRS H
J21- 65	INHIBIT CONSOLE L
J21- 67	REMOTE H
J21- 68	WAIT (TP)
J21- 69	+5V
J21- 70	+5V
J21- 71	GND
J21- 72	GND
J21- 89	GND
J21- 90	GND
J21- 92	FREE BUS H
J21- 97	SR SEL L
J21-100	EXT CLK
J21-101	EXT CLK RET
J21-105	GND
J21-106	GND
J21-119	MFM SER OUT H
J21-121	GND
J21-122	GND
J21-129	MFM SER IN H
J21-131	HLT GRANT H
J21-133	BUT SERVICE (1) H
J21-139	GND
J21-140	GND
J22-1	+5V
J22-2	+5V
J22-4	+SVF

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J22-5	PAN BOOT H
J22-6	PAN HALT H
J22-7	REMOTE L
J22-8	RUN L
J22- 14	CLEAR ERROR L
J22- 16	BOOT H
J22- 17	BUS DCLO L
J22- 20	+5v
J22- 22	PROC INIT L
J22- 23	614.4KHZ
J22- 24	POWER FAILURE H
J22- 34	HALT H
J22- 35	GND
J22- 36	GND
J22- 43	GND
J22- 45	GND
J22- 51	+5V
J22- 52	+5V
J22- 63	LTC
J22- 65	INHIBIT CONSOLE L
J22- 66	+15V
J22- 67	REMOTE H
J22- 68	LTC TP
J22- 69	+5v
J22- 70	+5V
J22- 71	GND
J22- 72	GND
J22- 89	GND
J22- 90	GND
J22- 93	20MA REC+
J22- 94	RUN H
J22- 95	20MA REC-
J22- 97	20MA TRANSMIT+
J22- 98	20MA TRANSMIT-
J22-106	GND
J22-109	SEND COMMON
J22-110	SEND DATA
J22-111	TERMINAL READY
J22-112	GND
J22-113	RTS/DSR-1
J22-114	RTS/DSR-2
J22-115	RECEIVE COMMON
J22-116	RECEIVE DATA
J22-119	MFM SER OUT H
J22-121	GND
J22-122	GND
J22-129	MFM SER IN H
J22-136	+15V
J22-137	+15V
J22-138	-12V
J22-139	GND
J22-140	GND
J23-1	BUS BG4 H (2)
J23-2	BUS BG5 H (2)

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J23-3	BUS BG6 H (2)
J23-4	BUS BG7 H (2)
J23-5	BUS NPR L
J23-6	BUS SACK L
J23-7	BUS INIT L
J23-8	BUS ACLO L
J23-9	BUS AOO L
J23- 10	BUS A02 L
J23- 11	BUS A04 L
J23- 12	BUS A05 L
J23- 13	BUS A07 L
J23- 14	BUS A09 L
J23- 15	BUS A10 L
J23- 16	BUS A12 L
J23- 17	BUS A14 L
J23- 18	BUS A15 L
J23- 19	BUS A17 L
J23- 20	BUS CO L
J23- 21	BUS C1 L
J23- 22	BUS MSYN L
J23- 23	BUS BR7 L
J23- 24	BUS NPG H (2)
J23- 25	+5v
J23- 26	BUS BBSY L
J23- 27	BUS DCLO L
J23- 28	BUS A01 L
J23- 29	+5V
J23- 30	BUS A03 L
J23- 31	BUS A06 L
J23- 32	GND
J23- 33	BUS A08 L
J23- 34	BUS A11 L
J23- 35	BUS A13 L
J23- 36	GND
J23- 37	BUS A16 L
J23- 38	BUS SSYN L
J23- 39	GND
J23- 40	BUS BR4 L
J23- 41	BUS D15 L
J23- 42	BUS D13 L
J23- 43	GND
J23- 44	BUS D11 L
J23- 45	BUS D10 L
J23- 46	BUS D08 L
J23- 47	BUS D06 L
J23- 48	BUS D05 L
J23- 49	BUS D03 L
J23- 50	GND
J23- 51	BUS D02 L
J23- 52	BUS D00 L
J23- 53	BUS PB L
J23- 54	GND
J23- 55	BUS BR6 L
J23- 56	BUS BR5 L

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J23- 57	GND
J23- 58	BUS D14 L
J23- 59	GND
J23- 60	BUS D12 L
J23- 61	GND
J23- 62	BUS D09 L
J23- 63	BUS D07 L
J23- 64	GND
J23- 65	BUS D04 L
J23- 66	GND
J23- 67	BUS D01 L
J23- 68	GND
J23- 69	BUS INTR L
J23- 70	BUS PA L
J24-1	GND
J24-2	GND
J24-7	RECEIVE DATA
J24-9	SEND DATA
J24- 10	SEND COMMON
J24- 11	REMOTE L
J24- 13	PAN BOOT H
J24- 22	RUN L
J24- 23	+5VF
J24- 25	RECEIVE COMMON
J24- 26	20MA TRANSMIT+
J24- 37	TERMINAL READY
J24- 28	PAN HALT H
J24- 29	GND
J24- 32	GND
J24- 36	RTS/DSR-2
J24- 39	20MA REC-
J24- 40	20MA REC+
J24- 41	20MA TRANSMIT-
J24- 47	RTS/DSR-1
J25-1	GND
J25-2	RTS-2
J25-3	GND
J25-4	CTS-1
J25-5	RTN-1
J25-6	CTS-2
J25-7	RTN-2
J25-8	CTS-3
J25-9	RTN-3
J25- 10	GND
J25- 11	RTS-0
J25- 12	CTS-0
J25- 13	RTN-0
J25- 14	RTS-3
J25- 15	GND
J25- 16	RTS-1
J25- 17	GND
J25- 18	GND
J25- 24	GND
J25- 26	TXD-4

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J25- 28	RXD-4
J25- 29	RXDH-4
J25- 30	RXD-5
J25- 31	RXDH-5
J25- 32	TXD-5
J25- 34	TXD-6
J25- 35	GND
J25- 38	RXDH-0
J25- 39	RXD-0
J25- 41	TXD-0
J25- 46	TXD-1
J25- 47	RXD-1
J25- 48	RXDH-1
J25- 51	GND
J25- 52	TXD-2
J25- 53	RXD-2
J25- 54	RXDH-2
J25- 58	TXD-3
J25- 59	RXD-3
J25- 60	RXDH-3
J25- 66	GND
J26-1	GND
J26-2	RTS-4
J26-3	GND
J26-4	CTS-5
J26-5	RTN-5
J26-6	CTS-6
J26-7	RTN-6
J26-8	RTS-5
J26-9	GND
J26- 10	RTS-6
J26- 11	GND
J26- 12	RTS-7
J26- 13	GND
J26- 14	CTS-4
J26- 15	RTN-4
J26- 16	CTS-7
J26- 17	RTN-7
J26- 18	RXD-6
J26- 19	RXDH-6
J26- 23	TXD-7
J26- 24	RXD-7
J26- 25	RXDH-7
J26- 30	DISCOUT 3
J26- 34	DISCIN-0
J26- 35	DISCIN-1
J26- 36	DISCIN-2
J26- 37	DISCIN-3
J26- 41	GND
J26- 46	GND
J26- 51	GND
J26- 57	GND
J26- 59	DISCOUT 2
J26- 60	DISCOUT 0

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J26- 61	+5V
J26- 62	-12V
J26- 63	+15V
J26- 64	GND
J26- 66	GND
J27-1	GND
J27-4	CHO CD H
J27-5	CHO RTN
J27-8	CCA10 DISC 04 OUT
J27- 10	CHO TRXC H
J27- 11	CHO TRXC L
J27- 12	SMA14 DISC IN 0
J27- 13	CHO RTN
J27- 14	CHO RTXC H
J27- 15	CHO RTXC L
J27- 18	CH1 RTN
J27- 19	CH1 CD H
J27- 20	CH1 RTXC H
J27- 21	CH1 RTXC L
J27- 22	CH1 RTN
J27- 23	SMA14 DISC IN 1
J27- 24	CH1 TRXC H
J27- 25	CH1 TRXC L
J27- 26	CCA10 DISC 05 OUT
J27- 36	CHO RTS H
J27- 37	GND
J27- 38	CHO RXD H
J27- 39	CHO RXD L
J27- 40	CHO RTN
J27- 41	CHO CTS H
J27- 42	CHO TXD H
J27- 43	GND
J27- 44	CH1 RTS H
J27- 45	GND
J27- 48	GND
J27- 49	CH1 TXD H
J27- 50	CH1 RXD L
J27- 51	CH1 RXD H
J27- 52	CH1 CTS H
J27- 53	CH1 RTN
J27- 62	GND
J27- 63	GND
J27- 64	GND
J27- 65	GND
J27- 66	GND
J28-1	GND
J28-6	CH2 RTS H
J28-7	GND
J28-8	GND
J28-9	CH2 TXD H
J28- 10	CH2 RXD L
J28- 11	CH2 RXD H
J28- 12	CH2 CTS H
J28- 13	CH2 RTN

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
J28- 17	GND
J28- 20	CH3 TXD H
J28- 21	GND
J28- 22	CH3 RTS H
J28- 23	GND
J28- 25	CH3 TRXC H
J28- 26	CH3 CD
J28- 27	CH3 RTN
J28- 32	GND
J28- 33	GND
J28- 34	CH3 CTS H
J28- 35	CH3 RTN
J28- 40	CH2 CD
J28- 41	CH2 RTN
J28- 42	CH2 RTXC H
J28- 43	CH2 RTXC L
J28- 44	CH2 RTN
J28- 45	SMA14 DISC IN 2
J28- 46	CH2 TRXC H
J28- 47	CH2 TRXC L
J28- 48	CCA10 DISC 06 OUT
J28- 52	CH3 RXD H
J28- 53	CH3 RXD L
J28- 54	CH3 TRXC L
J28- 55	CCA10 DISC 07 OUT
J28- 56	SMA14 DISC IN 3
J28- 57	CH3 RTN
J28- 58	CH3 RTXC H
J28- 59	CH3 RTXC L
J28- 61	+5V
J28- 62	-12V
J28- 63	+15V
J28- 64	GND
J28- 66	GND
J29-1	+5VBB
J29-2	+SVBB
J29-5	GND
J29-6	GND
J29-9	+5v
J29- 10	+5V
J29- 15	+5VBB
J29- 16	+5VBB
J29- 19	GND
J29- 20	GND
J29- 23	+5v
J29- 24	+5v
J29- 29	+5VBB
J29- 30	+5VBB
J29- 33	GND
J29- 34	GND
J29- 37	+5V
J29- 38	+5V
J29- 59	+5VBB SENSE
J29- 60	+5VBB SENSE RTN

Backplane Node List
Sorted by Connector Number

Connector Pin Number	Signal Name
E 3	+15V
E 4	+15V
E 5	+15V
J08-136	+15v
J08-137	+15V
J09-136	+15V
J09-137	+15V
J10-136	+15v
J10-137	+15v
Jl1-136	+15V
J11-137	+15V
J22- 66	+15V
J22-136	+15V
J22-137	+15v
J26- 63	+15V
J28- 63	+15V
E21	+5V
J301- 47	+5V
J01- 48	+5v
J01- 49	+5V
J01- 50	+5V
J02-1	+5V
J02-2	+5V
J02- 19	+5V
J02- 20	+5V
J02- 51	+5V
J02- 52	+5V
J02- 69	+5V
J02- 70	+5V
J03- 47	+5V
J03- 48	+5V
J03- 49	+5V
J03- 50	+5V
J04-1	+5V
J04-2	+5V
J04- 19	+5V
J04- 20	+5V
J04- 51	+5V
J04- 52	+5V
J04- 69	+5V
J04- 70	+5V
J05- 47	+5V
J05- 48	+5V
J05- 49	+5V
J05- 50	+5V
J06-1	+5V
J06-2	+5V
J06- 19	+5V
J06- 20	+5V
J06- 51	+5v
J06- 52	+5V
J06- 69	+5V
J06- 70	+5V
J07-1	+5V

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J07-2	+5V
J07- 19	+5V
J07- 20	+5V
J07- 51	+5v
J07- 52	+5V
J07- 69	+5V
J07- 70	+5V
J08-1	+5V
J08-2	+5v
J08- 19	+5v
J08- 20	+5v
J08- 51	+5v
J08- 52	+5v
J08- 69	+5v
J08- 70	+5v
J09-1	+5v
J09-2	+5v
J09- 19	+5v
J09- 20	+5v
J09- 51	+5V
J09- 52	+5v
J09- 69	+5v
J09- 70	+5v
J10-1	+5v
J10-2	+5v
J10- 19	+5v
J10- 20	+5v
J10- 51	+5v
J10- 52	+5v
J10- 69	+5v
J10- 70	+5v
J11-1	+5v
J11-2	+5v
J11- 19	+5v
J11- 20	+5v
311- 51	+5v
J11- 52	+5v
J11- 69	+5v
J11- 70	+5v
J12-1	+5V
J12-2	+5v
J12- 19	+5v
J12- 20	+5v
J12- 51	+5v
J12- 52	+5v
J12- 69	+5v
J12- 70	+5V
J13-1	+5v
J13-2	+5V
J13- 19	+5V
J13- 20	+5v
J13- 51	+5v
J13- 52	+5v
J13- 69	+5v

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J13- 70	+5V
J14-1	+5V
J14-2	+5V
J14- 19	+5V
J14- 20	+5V
J14- 51	+5V
J14- 52	+5V
J14- 69	+5V
J14- 70	+5V
J15-1	+5V
J15-2	+5V
J15- 19	+5v
J15- 20	+5v
J15- 51	+5v
J15- 52	+5V
J15- 69	+5v
J15- 70	+5V
J16-1	+5V
J16-2	+5v
J16- 19	+5V
J16- 20	+5V
J16- 51	+5v
J16- 52	+5V
J16- 69	+5v
J16- 70	+5v
J17-1	+5V
J17-2	+5V
J17- 19	+5v
J17- 20	+5V
J17- 51	+5V
J17- 52	+5V
J17- 69	+5v
J17- 70	+5v
J18-1	+5V
J18-2	+5V
J18- 19	+5V
J18- 20	+5V
J18- 51	+5V
J18- 52	+5V
J18- 69	+5V
J18- 70	+5v
J19-1	+5V
J19-2	+5V
J19- 19	+5V
J19- 20	+5V
J19- 51	+5V
J19- 52	+5V
J19- 69	+5V
J19- 70	+5V
J20-1	+5V
J20-2	+5v
J20- 19	+5V
J20- 20	+5V
J20- 51	+5V

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J20- 52	+5V
J20- 69	+5V
J20- 70	+5V
J21-1	+5V
J21-2	+5V
J21- 19	+5v
J21- 20	+5v
J21- 51	+5V
J21- 52	+5v
J21- 69	+5V
J21- 70	+5V
J22-1	+5v
J22-2	+5v
J22- 20	+5v
J22- 51	+5v
J22- 52	+5v
J22- 69	+5v
J22- 70	+5V
J23- 25	+5v
J23- 29	+5V
J26- 61	+5V
J28- 61	+5V
J29-9	+5V
J29- 10	+5V
J29- 23	+5V
J29- 24	+5V
J29- 37	+5V
J29- 38	+5V
J02- 73	+5VBB
J02- 74	+5VBB
J02- 75	+5VBB
J02- 76	+5VBB
J02- 87	+5VBB
J02- 88	+5VBB
J02- 91	+5VBB
J02- 92	+5VBB
J02-119	+5VBB
J02-120	+5VBB
J02-123	+5VBB
J02-124	+5VBB
J02-132	+5VBB
J02-133	+5VBB
J02-134	+5VBB
J02-135	+5VBB
J04- 73	+5VBB
J04- 74	+5VBB
J04- 75	+5VBB
J04- 76	+5VBB
J04- 87	+5VBB
J04- 88	+5VBB
J04- 91	+5VBB
J04- 92	+5VBB
J04-119	+5VBB

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J04-120	+5VBB
J04-123	+5VBB
J04-124	+5VBB
J04-132	+5VBB
J04-133	+5VBB
J04-134	+5VBB
J06- 73	+5VBB
J06- 74	+5VBB
J06- 75	+5VBB
J06- 76	+5VBB
J06- 87	+5VBB
J06- 88	+5VBB
J06- 91	+5VBB
J06- 92	+5VBB
J06-119	+5VBB
J06-120	+5VBB
J06-123	+5VBB
J06-124	+5VBB
J06-132	+5VBB
J06-133	+5VBB
J06-134	+5VBB
J29-1	+5VBB
J29-2	+5VBB
J29- 15	+5VBB
J29- 16	+5VBB
J29- 29	+5VBB
J29- 30	+5VBB
J04-135	+5VBB SENSE
J06-135	+5VBB SENSE
J29- 59	+5VBB SENSE
J04-139	+5VBB SENSE RTN
J06-139	+5VBB SENSE RTN
J29- 60	+5VBB SENSE RTN
J22-4	+5VF
J24- 23	+5VF
E 6	-12V
E 7	-12V
E 8	-12V
J08-138	-12V
J09-138	-12V
J11-138	-12V
J22-138	-12V
J26- 62	-12V
J28- 62	-12V
J22- 93	20MA REC+
J24- 40	20MA REC+
J22- 95	20MA REC-
J24- 39	20MA REC-

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J22- 97	20MA TRANSMIT+
J24- 26	20MA TRANSMIT+
J22- 98	20MA TRANSMIT-
J24- 41	20MA TRANSMIT-
J21- 23	614.4KHZ
J22- 23	614.4KHZ
J17-104	8-15-0 L
J19-104	8-15-0 L
J01-3	A01 H
J03-3	A01 H
J05-3	A01 H
J07- 83	A01 H
J01-5	A02 H
J03-5	A02 H
J05-5	A02 H
J07- 84	A02 H
J01-7	A03 H
J03-7	A03 H
J05-7	A03 H
J07- 85	A03 H
J01-9	A04 H
J03-9	A04 H
J05-9	A04 H
J07- 86	A04 H
J01- 11	A05 H
J03- 11	A05 H
J05- 11	A05 H
J07- 87	A05 H
J01- 13	A06 H
J03- 13	A06 H
J05- 13	A06 H
J07- 88	A06 H
J01- 76	A07 H
J03- 76	A07 H
J05- 76	A07 H
J07-119	A07 H
J01- 83	A08 H
J03- 83	A08 H
J05- 83	A08 H
J07-123	A08 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J01- 85	A09 H
J03- 85	A09 H
J05- 85	A09 H
J07-124	A09 H
J01- 93	A10 H
J03- 93	A10 H
J05- 93	A10 H
J07-128	A10 H
J01- 91	A11 H
J03- 91	A11 H
J05- 91	A11 H
J07-127	A11 H
J01- 87	A12 H
J03- 87	A12 H
J05- 87	A12 H
J07-125	A12 H
J01- 89	A13 H
J03- 89	A13 H
J05- 89	A13 H
J07-126	A13 H
J01- 15	A14 H
J03- 15	A14 H
J05- 15	A14 H
J07- 91	A14 H
J01- 94	A15 H
J03- 94	A15 H
J05- 94	A15 H
J07-129	A15 H
J01- 64	A16 H
J03- 64	A16 H
J05- 64	A16 H
J07-130	A16 H
J01- 24	A17 H
J03- 24	A17 H
J05- 24	A17 H
J07-132	A17 H
J01- 51	A18 H
J03- 51	A18 H
J05- 51	A18 H
J07-131	A18 H
J07- 15	A19 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J13- 11	ABORT H
J18-118	ABORT H
J19- 48	ABORT H
J12-126	ALLOW MSYN H
J18-126	ALLOW MSYN H
J17- 77	ALU CIN L
J18- 77	ALU CIN L
J19- 77	ALU CIN L
J17- 99	ALU COUT H
J18- 99	ALU COUT H
J17- 78	ALU MODE H
J18- 78	ALU MODE H
J19- 78	ALU MODE H
J17-108	ALU S0 H
J18-108	ALU S0 H
J17-109	ALU S1 H
J18-109	ALU S1 H
J17-118	ALU S2 H
J18-9	ALU S2 H
J17-119	ALU S3 H
J18-119	ALU S3 H
J19-119	ALU S3 H
J17- 26	AMUX 00 H
J17- 27	AMUX 01 H
J17- 28	AMUX 02 H
J17- 30	AMUX 03 H
J17- 31	AMUX 04 H
J17- 32	AMUX 05 H
J17- 37	AMUX 06 H
J17- 38	AMUX 07 H
J17- 39	AMUX 08 H
J17- 40	AMUX 09 H
J17- 93	AMUX 10 H
J17- 94	AMUX 11 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J17- 95	AMUX 12 H
J17- 96	AMUX 13 H
J17- 97	AMUX 14 H
J17- 98	AMUX 15 H
J17-102	AMUX S0 11 LL
J18-102	AMUX S0 1 L
J17- 33	AMUX S1 (1) L
J18- 33	AMUX S1 (1) L
J17-100	AUX CONTROL L
J18-128	AUX CONTROL L
J17- 80	B MODE 00 L
J18- 80	B MODE 00 L
J17- 79	B MODE 01 L
J18- 79	B MODE 01 L
J17- 68	B REG 00(1) H
J18- 11	B REG 00(1) H
J13- 44	BA17 H
J19- 44	BA17 H
J12-134	BE (1) H
J18- 64	BE (1) H
J19- 64	BE (1) H
J17- 75	BLEG 00 H
J18-5	BLEG 00 H
J19- 75	BLEG 00 H
J17- 74	BLEG 01 H
J18-4	BLEG 01 H
J19- 74	BLEG 01 H
J01- 45	BOOT ENAB L
J03- 45	BOOT ENAB L
J05- 45	BOOT ENAB L
J19- 99	BOOT ENAB L
J19- 82	BOOT H
J22- 16	BOOT H
J17- 11	BREG 14 (1) H
J19- 11	BREG 14 (1) H
J17- 10	BREG 15 (1) H
J19- 10	BREG 15 (1) H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J12- 92	BUF CO (1) H
J18- 61	BUF CO(1) H
J12- 91	BUF C1 (1) H
J15- 91	BUF C1 (1) H
J18- 91	BUF C1 1 H
J19- 91	BUF C1 1 H
J12-112	BUF DATA TRAN (1) H
J16-112	BUF DATA TRAN (1) H
J18-112	BUF DATA TRAN (1) H
J19-112	BUF DATA TRAN (1) H
J11- 23	BUS A00 L
J12- 23	BUS A00 L
J23-9	BUS A00 L
J11- 24	BUS A01 L
J12- 24	BUS A01 L
J23- 28	BUS A01 L
J11- 25	BUS A02 L
J12- 25	BUS A02 L
J23- 10	BUS A02 L
J11- 26	BUS A03 L
J12- 26	BUS A03 L
J23- 30	BUS A03 L
J11- 27	BUS A04 L
J12- 27	BUS A04 L
J23- 11	BUS A04 L
J11- 28	BUS A05 L
J12- 28	BUS A05 L
J23- 12	BUS A05 L
J11- 29	BUS A06 L
J12- 29	BUS A06 L
J23- 31	BUS A06 L
J11- 30	BUS A07 L
J12- 30	BUS A07 L
J23- 13	BUS A07 L
J11- 31	BUS A08 L
J12- 31	BUS A08 L
J23- 33	BUS A08 L
J11- 32	BUS A09 L
J12- 32	BUS A09 L
J23- 14	BUS A09 L

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J11- 33	BUS A10 L
J12- 33	BUS A10 L
J23- 15	BUS A10 L
J11- 34	BUS A11 L
J12- 34	BUS A11 L
J23- 34	BUS A11 L
J11- 37	BUS A12 L
J12- 37	BUS A12 L
J23- 16	BUS A12 L
J11- 38	BUS A13 L
J12- 38	BUS A13 L
J23- 35	BUS A13 L
J11- 39	BUS A14 L
J13- 39	BUS A14 L
J23- 17	BUS A14 L
J11- 40	BUS A15 L
J13- 40	BUS A15 L
J23- 18	BUS A15 L
J11- 41	BUS A16 L
J13- 41	BUS A16 L
J23- 37	BUS A16 L
J11- 42	BUS A17 L
J13- 42	BUS A17 L
J23- 19	BUS A17 L
E 2	BUS ACLO L
J01- 75	BUS ACLO L
J03- 75	BUS ACLO L
J05- 75	BUS ACLO L
J11- 17	BUS ACLO L
J19- 17	BUS ACLO L
J23-8	BUS ACLO L
J11- 14	BUS BBSY L
J12- 14	BUS BBSY L
J23- 26	BUS BBSY L
J11-7	BUS BG4 H (1)
J20- 55	BUS BG4 H (1)
J11- 77	BUS BG4 H J2
J23-1	BUS BG4 H 2
J11-8	BUS BG5 H (1)
J12-8	BUS BG5 H (1)

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J11- 78	BUS BG5 H (2)
J23-2	BUS BG5 H (2
J11-9	BUS BG6 H
J20- 56	BUS BG6 H (1)
J11- 79	BUS BG6 H (2)
J23-3	BUS BG6 H (2)
J11- 10	BUS BG7 H (1)
J12- 10	BUS BG7 H (1)
J11- 80	BUS BG7 H (2)
J23-4	BUS BG7 H (2)
J11-3	BUS BR4 L
J13-3	BUS BR4 L
J20-3	BUS BR4 L
J23- 40	BUS BR4 L
J11-4	BUS BR5 L
J13-4	BUS BR5 L
J23- 56	BUS BR5 L
J11-5	BUS BR6 L
J135	BUS BR6 L
J20-5	BUS BR6 L
J23- 55	BUS BR6 L
J11-6	BUS BR7 L
J13-6	BUS BR7 L
J23- 23	BUS BR7 L
J11- 43	BUS C0 L
J12- 43	BUS C0 L
J23- 20	BUS C0 L
J11- 44	BUS C1 L
J12- 44	BUS C1 L
J23- 21	BUS C1 L
J07- 53	BUS D00 L
J11- 53	BUS D00 L
J13- 53	BUS D00 L
J23- 52	BUS D00 L
J07- 54	BUS D01 L
J11- 54	BUS D01 L
J13- 54	BUS D01 L
J23- 67	BUS D01 L

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J07- 55	BUS D02 L
J11- 55	BUS D02 L
J13- 55	BUS D02 L
J23- 51	BUS D02 L
J07- 56	BUS D03 L
J11- 56	BUS D03 L
J13- 56	BUS D03 L
J23- 49	BUS D03 L
J07- 57	BUS D04 L
J11- 57	BUS D04 L
J13- 57	BUS D04 L
J23- 65	BUS D04 L
J07- 58	BUS D05 L
J11- 58	BUS D05 L
J13- 58	BUS D05 L
J23- 48	BUS D05 L
J07- 59	BUS D06 L
J11- 59	BUS D06 L
J13- 59	BUS D06 L
J23- 47	BUS D06 L
J07- 60	BUS D07 L
J11- 60	BUS D07 L
J13- 60	BUS D07 L
J23- 63	BUS D07 L
J07- 61	BUS D08 L
J11- 61	BUS D08 L
J13- 61	BUS D08 L
J23- 46	BUS D08 L
J07- 62	BUS D09 L
J11- 62	BUS D09 L
J13- 62	BUS D09 L
J23- 62	BUS D09 L
J07- 63	BUS D10 L
J11- 63	BUS D10 L
J13- 63	BUS D10 L
J23- 45	BUS D10 L
J07- 64	BUS D11 L
J11- 64	BUS D11 L
J13- 64	BUS D11 L
J23- 44	BUS D11 L
J07- 65	BUS D12 L
J11- 65	BUS D12 L
J13- 65	BUS D12 L
J23- 60	BUS D12 L

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J07- 66	BUS D13 L
J11- 66	BUS D13 L
J13- 66	BUS D13 L
J23- 42	BUS D13 L
J07- 67	BUS D14 L
J11- 67	BUS D14 L
J13- 67	BUS D14 L
J23- 58	BUS D14 L
J07- 68	BUS D15 L
J11- 68	BUS D15 L
J13- 68	BUS D15 L
J23- 41	BUS D15 L
E 1	BUS DCLO L
J01- 61	BUS DCLO L
J03- 61	BUS DCLO L
J05- 61	BUS DCLO L
J07- 18	BUS DCLO L
J07-109	BUS DCLO L
J11- 18	BUS DCLO L
J18- 18	BUS DCLO L
J22- 17	BUS DCLO L
J23- 27	BUS DCLO L
J09- 15	BUS DIR
J10- 15	BUS DIR
J11- 15	BUS DIR
J11- 16	BUS INIT L
J19- 16	BUS INIT L
J20- 21	BUS INIT L
J23-7	BUS INIT L
J11- 49	BUS INTR L
J12- 49	BUS INTR L
J23- 69	BUS INTR L
J11- 45	BUS MSYN L
J12- 45	BUS MSYN L
J23- 22	BUS MSYN L
J11- 12	BUS NPG H (1)
J12- 12	BUS NPG H (1)
311- 82	BUS NPG H (2)
J23- 24	BUS NPG H (2)
311- 11	BUS NPR L
J12- 11	BUS NPR L
J23-5	BUS NPR L

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J11- 47	BUS PA L
J12- 47	BUS PA L
J23- 70	BUS PA L
J07- 48	BUS PB L
J11- 48	BUS PB L
J12- 48	BUS PB L
J15- 48	BUS PB L
J23- 53	BUS PB L
J11- 13	BUS SACK L
J12- 13	BUS SACK L
J20- 17	BUS SACK L
J23-6	BUS SACK L
J11- 46	BUS SSYN L
J12- 46	BUS SSYN L
J23- 38	BUS SSYN L
J13- 50	BUS STATUS ENAB L
J19- 38	BUS STATUS ENAB L
J20- 50	BUS STATUS ENAB L
J12-133	BUT SERVICE (1) H
J18- 63	BUT SERVICE 1) H
J21-133	BUT SERVICE (1) H
J17- 29	BUT Z BIT H
J18- 62	BUT Z BIT H
J17- 81	BX MODE 00 L
J18- 81	BX MODE 00 L
J17- 82	BX MODE 01 L
J18- 82	BX MODE 01 L
J17- 62	BX REG 00(1) H
J18- 92	BX REG 00(1) H
J17- 61	BX REG 01(1) H
J18- 29	BX REG 01(1 H
J12-6	BYTE H
J18-6	BYTE H
J19-6	BYTE H
J17- 15	BYTE L
J18- 15	BYTE L
J19- 15	BYTE L
J17- 12	C BIT (1) H
J18- 12	C BIT (1) H
J19- 12	C BIT (1) H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J17- 55	C1 H
J18-100	C1 H
J17- 56	C2 H
J18- 56	C2 H
J17- 57	C3 H
J18- 57	C3 H
J17- 58	C4 H
J18- 58	C4 H
J17- 59	C5-C7 H
J18- 59	C5-C7 H
J17- 54	C6 H
J18- 54	C6 H
J15- 85	CACHE BYPASS L
J16- 15	CACHE BYPASS L
J19- 85	CACHE BYPASS L
J12- 55	CACHE GATE H
J15- 55	CACHE GATE H
J14-103	CACHE GR TP1
J14-101	CACHE GR TP2
J15- 64	CACHE MATCH L (TP)
J12- 53	CACHE PE INTR L
J15- 53	CACHE PE INTR L
J12- 59	CACHE RESTART L
J14- 59	CACHE RESTART L
J18- 60	CACHE RESTART L
J19- 59	CACHE RESTART L
J17- 87	CC CODE 00 H
J19- 88	CC CODE 00 H
J17-3	CC CODE 01 H
J19-3	CC CODE 01 H
J17- 13	CC CODE 02 H
J19- 83	CC CODE 02 H
J17-107	CC N H
J18-107	CC N H
Jl1-125	CCA10 DISC 04 OUT
J27-8	CCA10 DISC 04 OUT

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
311-126	CCA10 DISC 05 OUT
J27- 26	CCA10 DISC 05 OUT
J11-135	CCA10 DISC 06 OUT
J28- 48	CCA10 DISC 06 OUT
J11- 50	CCA10 DISC 07 OUT
J28- 55	CCA10 DISC 07 OUT
J09- 54	CH0 CD H
J27-4	CH0 CD H
J09- 11	CH0 CTS H
J27- 41	CH0 CTS H
J09- 44	CH0 RTN
J27-5	CH0 RTN
J27- 13	CH0 RTN
J27- 40	CH0 RTN
J09- 34	CH0 RTS H
J27- 36	CH0 RTS H
J09- 27	CH0 RTXC H
J27- 14	CH0 RTXC H
J09- 26	CH0 RTXC L
J27- 15	CH0 RTXC L
J09-128	CH0 RXD H
J27- 38	CH0 RXD H
J09-110	CH0 RXD L
J27- 39	CH0 RXD L
J09-4	CH0 TRXC H
J27- 10	CH0 TRXC H
J09-3	CH0 TRXC L
J27- 11	CH0 TRXC L
J09-118	CH0 TXD H
J27- 42	CH0 TXD H
J09- 55	CH1 CD H
J27- 19	CH1 CD H
J09- 12	CH1 CTS H
J27- 52	CH1 CTS H
J09- 45	CH1 RTN
J27- 18	CH1 RTN
J27- 22	CH1 RTN
J27- 53	CH1 RTN

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J09- 37	CH1 RTS H
J27- 44	CH1 RTS H
J09- 29	CH1 RTXC H
J27- 20	CH1 RTXC H
J09- 28	CH1 RTXC L
J27- 21	CH1 RTXC L
J09-129	CH1 RXD H
J27- 51	CH1 RXD H
J09-111	CH1 RXD L
J27- 50	CH1 RXD L
J09-6	CH1 TRXC H
J27- 24	CH1 TRXC H
J09-5	CH1 TRXC L
J27- 25	CH1 TRXC L
J09-119	CH1 TXD H
J27- 49	CH1 TXD H
J09- 56	CH2 CD
J28- 40	CH2 CD
J09- 13	CH2 CTS H
J28- 12	CH2 CTS H
J09- 46	CH2 RTN
J28- 13	CH2 RTN
J28- 41	CH2 RTN
J28- 44	CH2 RTN
J09- 38	CH2 RTS H
J28-6	CH2 RTS H
J09- 31	CH2 RTXC H
J28- 42	CH2 RTXC H
J09- 30	CH2 RTXC L
J28- 43	CH2 RTXC L
J09-130	CH2 RXD H
J28- 11	CH2 RXD H
J09-112	CH2 RXD L
J28- 10	CH2 RXD L
J09-8	CH2 TRXC H
J28- 46	CH2 TRXC H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J09-7	CH2 TRXC L
J28- 47	CH2 TRXC L
J09-120	CH2 TXD H
J28-9	CH2 TXD H
J09- 57	CH3 CD
J28- 26	CH3 CD
J09- 14	CH3 CTS H
J28- 34	CH3 CTS H
J09- 47	CH3 RTN
J28- 27	CH3 RTN
J28- 35	CH3 RTN
J28- 57	CH3 RTN
J09- 39	CH3 RTS H
J28- 22	CH3 RTS H
J09- 33	CH3 RTXC H
J28- 58	CH3 RTXC H
J09- 32	CH3 RTXC L
J28- 59	CH3 RTXC L
J09-131	CH3 RXD H
J28- 52	CH3 RXD H
J09-113	CH3 RXD L
J28- 53	CH3 RXD L
J09- 10	CH3 TRXC H
J28- 25	CH3 TRXC H
J09-9	CH3 TRXC L
J28- 54	CH3 TRXC L
J09-123	CH3 TXD H
J28- 20	CH3 TXD H
J12-111	CIS ENAB L
J19- 41	CIS ENAB L
J16-113	CLEAR ERROR L
J19- 42	CLEAR ERROR L
J22- 14	CLEAR ERROR L
J18-117	CLK EB TP
J18-120	CLK OSC
J18-116	CLK TP

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J12-124	CLR MPC L
J18-124	CLR MPC L
J12-4	CPU DATO L
J17-4	CPU DATO L
J21-4	CPU DATO L
J21- 61	CPU ENAB ADRS H
J12-127	CPU HLT (1) H
J18-127	CPU HLT (1) H
J12- 17	CPU HLT RQST L
J15- 17	CPU HLT RQST L
J19- 87	CPU HLT RQST L
J21- 17	CPU HLT RQST L
J12- 42	CPU MSYN (1) H
J16- 42	CPU MSYN (1) H
J20- 32	CPU MSYN (1) H
J01- 72	CSR CLEAR L
J03- 72	CSR CLEAR L
J05- 72	CSR CLEAR L
J07- 21	CSR CLEAR L
J01- 73	CSR INITIATE H
J03- 73	CSR INITIATE H
J05- 73	CSR INITIATE H
J07-108	CSR INITIATE H
J09- 21	CTRL 16 MHZ
J10- 21	CTRL 16 MHZ
J11- 21	CTRL 16 MHZ
J09- 81	CTRL ALE
J10- 81	CTRL ALE
J11- 81	CTRL ALE
J09- 75	CTRL DEN
J10- 75	CTRL DEN
J11- 75	CTRL DEN
J09- 74	CTRL DTR
J10- 74	CTRL DTR
J11- 74	CTRL DTR
J09- 73	CTRL RESET
J10- 73	CTRL RESET
J11- 73	CTRL RESET
J10-109	CTRL WAIT 0
J11-115	CTRL WAIT 0

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J09-109	CTRL WAIT 1
J11-116	CTRL WAIT 1
310- 11	CTS-0
J25- 12	CTS-0
J10- 12	CTS-1
J25-4	CTS-1
J10- 13	CTS-2
J25-6	CTS-2
J10- 14	CTS-3
J25-8	CTS-3
J10- 22	CTS-4
J26- 14	CTS-4
J10- 23	CTS-5
J26-4	CTS-5
J10- 24	CTS-6
J26-6	CTS-6
J10- 25	CTS-7
J26- 16	CTS-7
J01- 35	CYCLE INIT H
J03- 35	CYCLE INIT H
J05- 35	CYCLE INIT H
J07- 99	CYCLE INIT H
J16-131	D SPACE H
J18-131	D SPACE H
J01-6	DATA 00 H
J01- 16	DATA 00 H
J03-6	DATA 00 H
J03- 16	DATA 00 H
J05-6	DATA 00 H
J05- 16	DATA 00 H
J07- 81	DATA 00 H
J01-4	DATA 01 H
J01- 38	DATA 01 H
J03-4	DATA 01 H
J03- 38	DATA 01 H
J05-4	DATA 01 H
J05- 38	DATA 01 H
J07-100	DATA 01 H

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J01- 10	DATA 02 H
J01- 34	DATA 02 H
J03- 10	DATA 02 H
J03- 34	DATA 02 H
J05- 10	DATA 02 H
J05- 34	DATA 02 H
J07-101	DATA 02 H
J01- 8	DATA 03 H
J01- 30	DATA 03 H
J03- 8	DATA 03 H
J03- 30	DATA 03 H
J05- 8	DATA 03 H
J05- 30	DATA 03 H
J07- 96	DATA 03 H
J01- 14	DATA 04 H
J01- 18	DATA 04 H
J03- 14	DATA 04 H
J03- 18	DATA 04 H
J05- 14	DATA 04 H
J05- 18	DATA 04 H
J07- 92	DATA 04 H
J01- 12	DATA 05 H
J01- 31	DATA 05 H
J03- 12	DATA 05 H
J03- 31	DATA 05 H
J05- 12	DATA 05 H
J05- 31	DATA 05 H
J07- 97	DATA 05 H
J01- 25	DATA 06 H
J01- 29	DATA 06 H
J03- 25	DATA 06 H
J03- 29	DATA 06 H
J05- 25	DATA 06 H
J05- 29	DATA 06 H
J07- 94	DATA 06 H
J01- 17	DATA 07 H
J01- 28	DATA 07 H
J03- 17	DATA 07 H
J03- 28	DATA 07 H
J05- 17	DATA 07 H
J05- 28	DATA 07 H
J07- 93	DATA 07 H

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J01- 70	DATA 08 H
J01- 79	DATA 08 H
J03- 70	DATA 08 H
J03- 79	DATA 08 H
J05- 70	DATA 08 H
J05- 79	DATA 08 H
J07-118	DATA 08 H
J01- 66	DATA 09 H
J01- 80	DATA 09 H
J03- 66	DATA 09 H
J03- 80	DATA 09 H
J05- 66	DATA 09 H
J05- 80	DATA 09 H
J07-120	DATA 09 H
J01- 68	DATA 10 H
J01- 81	DATA 10 H
J03- 68	DATA 10 H
J03- 81	DATA 10 H
J05- 68	DATA 10 H
J05- 81	DATA 10 H
J07-116	DATA 10 H
J01- 71	DATA 11 H
J01- 82	DATA 11 H
J03- 71	DATA 11 H
J03- 82	DATA 11 H
J05- 71	DATA 11 H
J05- 82	DATA 11 H
J07-117	DATA 11 H
J01- 65	DATA 12 H
J01- 84	DATA 12 H
J03- 65	DATA 12 H
J03- 84	DATA 12 H
J05- 65	DATA 12 H
J05- 84	DATA 12 H
J07-114	DATA 12 H
J01- 60	DATA 13 H
J01- 86	DATA 13 H
J03- 60	DATA 13 H
J03- 86	DATA 13 H
J05- 60	DATA 13 H
J05- 86	DATA 13 H
J07-110	DATA 13 H

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J01- 62	DATA 14 H
J01- 88	DATA 14 H
J03- 62	DATA 14 H
J03- 88	DATA 14 H
J05- 62	DATA 14 H
J05- 88	DATA 14 H
J07- 112	DATA 14 H
J01- 59	DATA 15 H
J01- 90	DATA 15 H
J03- 59	DATA 15 H
J03- 90	DATA 15 H
J05- 59	DATA 15 H
J05- 90	DATA 15 H
J07-111	DATA 15 H
J05- 40	DATA OUT CONT (1)L
J07-107	DATA OUT CONT (1)L
J03- 40	DATA OUT CONT (2)L
J07-138	DATA OUT CONT (2)
J01- 40	DATA OUT CONT (3)L
J07- 137	DATA OUT CONT (3)L
J05- 21	DATA RDY (1) L
J07- 77	DATA RDY (1) L
J03- 21	DATA RDY (2) L
J07- 78	DATA RDY (2) L
JO1- 21	DATA RDY (3) L
J07- 79	DATA RDY (3) L
J19- 80	DCLO H
J20-115	DCLO H
J18-115	DCLO H
J17- 76	DISABLE LOAD PSW H
J19- 76	DISABLE LOAD PSW H
J12-138	DISABLE MSYN L
J18- 68	DISABLE MSYN L
J19- 68	DISABLE MSYN L
J13- 23	DISABLE W BIT L
J16- 23	DISABLE W BIT L
J11-127	DISCIN-0
J26- 34	DISCIN-0
J11-128	DISCIN-1
J26- 35	DISCIN-1

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J11-129	DISCIN-2
J26- 36	DISCIN-2
J11-130	DISCIN-3
J26- 37	DISCIN-3
J11-119	DISCOUT 0
J26- 60	DISCOUT 0
J11-123	DISCOUT 2
J26- 59	DISCOUT 2
J11-124	DISCOUT 3
J26- 30	DISCOUT 3
J17- 49	DP BLEG 00 H
J19- 49	DP BLEG 00 H
J17- 50	DP BLEG 01 H
J19- 50	DP BLEG 01 H
J17-115	DP BLEG 02 H
J19-115	DP BLEG 02 H
J17-116	DP BLEG 03 H
J19-116	DP BLEG 03 H
J16-110	E22 BITS H
J19-110	E22 BITS H
J13- 33	EMAP H
J19-114	EMAP H
J12- 61	ENAB ADRS H
J14- 61	ENAB ADRS H
J15- 61	ENAB ADRS H
J12-137	ENAB GRANTS H
J18-137	ENAB GRANTS H
J16- 30	ENAB INT REG L
J19- 30	ENAB INT REG L
J16- 50	ENAB KT MUX L (TP)
J14- 86	ENAB MAINT (1) H
J16- 16	ENAB MAINT (1) H
J18- 86	ENAB MAINT (1) H
J19- 86	ENAB MAINT (1) H
J17- 17	ENAB OVX L
J18- 87	ENAB OVX L

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J13- 43	END TRAN TO MFM L
J16- 43	END TRAN TO MFM L
J19- 43	END TRAN TO MFM L
J21- 43	END TRAN TO MFM L
J16- 67	ERROR H
J19-113	ERROR H
J07- 23	EUB AOO L
J12- 93	EUB AOO L
J13- 93	EUB AOO L
J15- 93	EUB AOO L
J07- 24	EUB A01 L
J12- 94	EUB A01 L
J13- 94	EUB A01 L
J15- 94	EUB A01 L
J07- 25	EUB A02 L
J12- 95	EUB A02 L
J13- 95	EUB A02 L
J15- 95	EUB A02 L
J07- 26	EUB A03 L
J12- 96	EUB A03 L
J13- 96	EUB A03 L
J15- 96	EUB A03 L
J07- 27	EUB A04 L
J12- 97	EUB A04 L
J13- 97	EUB A04 L
J15- 97	EUB A04 L
J07- 28	EUB A05 L
J12- 98	EUB A05 L
J13- 98	EUB A05 L
J15- 98	EUB A05 L
J07- 29	EUB A06 L
J12- 99	EUB A06 L
J13- 99	EUB A06 L
J15- 99	EUB A06 L
J07- 30	EUB A07 L
J12-100	EUB A07 L
J13-100	EUB A07 L
J15-100	EUB A07 L
J07- 31	EUB A08 L
J12-101	EUB A08 L
J13-101	EUB A08 L
J15-101	EUB A08 L

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J07- 32	EUB A09 L
J12-102	EUB A09 L
J13-102	EUB A09 L
J15-102	EUB A09 L
J07- 33	EUB A10 L
J12-103	EUB A10 L
J13-103	EUB A10 L
J15-103	EUB A10 L
J07- 34	EUB All L
J12-104	EUB All L
J13-104	EUB All L
J15-104	EUB All L
J07- 37	EUB A12 L
J12-107	EUB A12 L
J13-107	EUB A12 L
J15-107	EUB A12 L
J07- 38	EUB A13 L
J12-108	EUB A13 L
J13-108	EUB A13 L
J15-108	EUB A13 L
J07- 39	EUB A14 L
J13-109	EUB A14 L
J15-109	EUB A14 L
J07- 40	EUB A15 L
J13-110	EUB A15 L
J15-110	EUB A15 L
J07- 41	EUB A16 L
J13-111	EUB A16 L
J15-111	EUB A16 L
J07- 42	EUB A17 L
J13-112	EUB A17 L
J15-112	EUB A17 L
J07- 3	EUB A18 L
J13- 73	EUB A18 L
J15- 73	EUB A18 L
J07- 4	EUB A19 L
J13- 74	EUB A19 L
J15- 74	EUB A19 L
J07- 5	EUB A20 L
J13- 75	EUB A20 L
J15- 75	EUB A20 L

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J07- 6	EUB A21 L
J13- 76	EUB A21 L
J15- 76	EUB A21 L
J07- 43	EUB CO L
J12-113	EUB CO L
J13-113	EUB CO L
J15-113	EUB CO L
J07- 44	EUB C1 L
J12-114	EUB C1 L
J13-114	EUB C1 L
J15-114	EUB C1 L
J07- 16	EUB INIT L
J19-111	EUB INIT L
J07- 45	EUB MSYN L
J12-115	EUB MSYN L
J15-115	EUB MSYN L
J07- 50	EUB SSYN L
J12-116	EUB SSYN L
J15-116	EUB SSYN L
J21- 60	EXIT CONSOLE L
J319- 25	EXIT CONSOLE L
J20- 25	EXIT CONSOLE L
J21-100	EXT CLK
J15- 30	EXT CLK A L
J18- 30	EXT CLK A L
J21- 30	EXT CLK A L
J17- 25	EXT CLK B1 L
J18- 25	EXT CLK B1 L
J17-114	EXT CLK B2 L
J18-114	EXT CLK B2 L
J16- 44	EXT CLK B3 L
J18- 44	EXT CLK B3 L
J12- 21	EXT CLK C L
J18- 21	EXT CLK C L
J21-101	EXT CLK RET
J12- 50	EXT TAP 30 H
J17-120	EXT TAP 30 H
J18- 50	EXT TAP 30 H
J20-120	EXT TAP 30 H

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J18- 43	EXT TAP 90 L
J12-125	FAULT H
J14-125	FAULT H
J13- 25	FORCE BUS DATA L
J20- 49	FORCE BUS DATA L
J15- 18	FORCE CACHE DATA L
J20- 18	FORCE CACHE DATA L
J20- 64	FORCE CIS DATA L
J20- 65	FORCE CPC L
J17- 42	FORCE CPU DATA L
J20- 42	FORCE CPU DATA L
J19- 63	FORCE CPU MPC L
J20- 63	FORCE CPU MPC L
J20- 67	FORCE FPP DATA L
J16-111	FORCE KERNEL (1) H
J17-111	FORCE KERNEL 1) H
J18- 65	FORCE KERNEL (1) H
J17- 43	FORCE SS DATA L
J20- 44	FORCE SS DATA L
J19- 84	FP11F ATTACHED L
J13- 22	FREE BUS H
J15- 92	FREE BUS H
J17- 92	FREE BUS H
J19- 92	FREE BUS H
J21- 92	FREE BUS H
J11-108	GND
J11-109	GND
J11-110	GND
J25- 3	GND
J25- 10	GND
J25- 15	GND
J25- 17	GND
J25- 18	GND
J25- 24	GND
J25- 35	GND
J25- 51	GND
J26- 3	GND
J26- 9	GND
J26- 11	GND
J26- 13	GND
J26- 41	GND

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J26- 46	GND
J26- 51	GND
J26- 57	GND
J27- 37	GND
J27- 43	GND
J27- 45	GND
J27- 48	GND
J27- 62	GND
J27- 63	GND
J27- 64	GND
J27- 65	GND
J28- 7	GND
J28- 8	GND
J28- 17	GND
J28- 21	GND
J28- 23	GND
J28- 32	GND
J28- 33	GND
E22	GND
J01- 1	GND
J01- 2	GND
J01- 22	GND
J01- 32	GND
J01- 36	GND
J01- 42	GND
J01- 44	GND
J01- 54	GND
J01- 58	GND
J01- 74	GND
J01- 95	GND
J01- 96	GND
J02- 35	GND
J02- 36	GND
J02- 71	GND
J02- 72	GND
J02- 89	GND
J02- 90	GND
J02-105	GND
J02-106	GND
J02-121	GND
J02-122	GND
J02-139	GND
J02-140	GND
J03- 1	GND
J03- 2	GND
J03- 22	GND
J03- 32	GND
J03- 36	GND
J03- 42	GND
J03- 44	GND
J03- 54	GND
J03- 58	GND
J03- 74	GND
J03- 95	GND

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J03- 96	GND
J04- 35	GND
J04- 36	GND
J04- 71	GND
J04- 72	GND
J04- 89	GND
J04- 90	GND
J04-105	GND
J04-106	GND
J04-121	GND
J04-122	GND
J04-140	GND
J05- 1	GND
J05- 2	GND
J05- 22	GND
J05- 32	GND
J05- 36	GND
J05- 42	GND
J05- 44	GND
J05- 54	GND
J05- 58	GND
J05- 74	GND
J05- 95	GND
J05- 96	GND
J06- 35	GND
J06- 36	GND
J06- 71	GND
J06- 72	GND
J06- 89	GND
J06- 90	GND
J06-105	GND
J06-106	GND
J06-121	GND
J06-122	GND
J06-140	GND
J07- 35	GND
J07- 36	GND
J07- 71	GND
J07- 72	GND
J07- 89	GND
J07- 90	GND
J07-105	GND
J07-106	GND
J07-121	GND
J07-122	GND
J07-139	GND
J07-140	GND
J08- 35	GND
J08- 36	GND
J08- 71	GND
J08- 72	GND
J08- 89	GND
J08- 90	GND
J08-105	GND

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J08-106	GND
J08-121	GND
J08-122	GND
J08-139	GND
J08-140	GND
J09- 35	GND
J09- 36	GND
J09- 71	GND
J09- 72	GND
J09- 89	GND
J09- 90	GND
J09-105	GND
J09-106	GND
J09-121	GND
J09-122	GND
J09-139	GND
J09-140	GND
J10- 35	GND
J10- 36	GND
J10- 71	GND
J10- 72	GND
J10- 89	GND
J10- 90	GND
J10-105	GND
J10-106	GND
J10-121	GND
J10-122	GND
J10-139	GND
J10-140	GND
J11- 35	GND
J11- 36	GND
J11- 71	GND
J11- 72	GND
J11- 89	GND
J11- 90	GND
J11-105	GND
Jl1-106	GND
J11-121	GND
J11-122	GND
J11-139	GND
J11-140	GND
J12- 35	GND
J12- 36	GND
J12- 71	GND
J12- 72	GND
J12- 89	GND
J12- 90	GND
J12-105	GND
J12-106	GND
J12-121	GND
J12-122	GND
J12-139	GND
J12-140	GND
J13- 35	GND

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J13- 36	GND
J13- 71	GND
J13- 72	GND
J13- 89	GND
J13- 90	GND
J13-105	GND
J13-106	GND
J13-121	GND
J13-122	GND
J13-139	GND
J13-140	GND
J14- 35	GND
J14- 36	GND
J14- 71	GND
J14- 72	GND
J14- 89	GND
J14- 90	GND
J14-105	GND
J14-106	GND
J14-121	GND
J14-122	GND
J14-139	GND
J14-140	GND
J15- 35	GND
J15- 36	GND
J15- 71	GND
J15- 72	GND
J15- 89	GND
J15- 90	GND
J15-105	GND
J15-106	GND
J15-121	GND
J15-122	GND
J15-139	GND
J15-140	GND
J16- 35	GND
J16- 36	GND
J16- 71	GND
J16- 72	GND
J16- 89	GND
J16- 90	GND
J16-105	GND
J16-106	GND
J16-121	GND
J16-122	GND
J16-139	GND
J16-140	GND
J17- 35	GND
J17- 36	GND
J17- 71	GND
J17- 72	GND
J17- 89	GND
J17- 90	GND
J17-105	GND

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J17-106	GND
J17-121	GND
J17-122	GND
J17-139	GND
J17-140	GND
J18- 35	GND
J18- 36	GND
J18- 71	GND
J18- 72	GND
J18- 89	GND
J18- 90	GND
J18-105	GND
J18-106	GND
J18-121	GND
J18-122	GND
J18-139	GND
J18-140	GND
J19- 35	GND
J19- 36	GND
J19- 71	GND
J19- 72	GND
J19- 89	GND
J19- 90	GND
J19-105	GND
J19-106	GND
J19-121	GND
J19-122	GND
J19-139	GND
J19-140	GND
J20- 35	GND
J20- 36	GND
J20- 71	GND
J20- 72	GND
J20- 89	GND
J20- 90	GND
J20-105	GND
J20-106	GND
J20-121	GND
J20-122	GND
J20-139	GND
J20-140	GND
J21- 35	GND
J21- 36	GND
J21- 71	GND
J21- 72	GND
J21- 89	GND
J21- 90	GND
J21-105	GND
J21-106	GND
J21-121	GND
J21-122	GND
J21-139	GND
J21-140	GND
J22- 35	GND

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J22- 36	GND
J22- 43	GND
J22- 45	GND
J22- 71	GND
J22- 72	GND
J22- 89	GND
J22- 90	GND
J22-106	GND
J22-112	GND
J22-121	GND
J22-122	GND
J22-139	GND
J22-140	GND
J23- 32	GND
J23- 36	GND
J23- 39	GND
J23- 43	GND
J23- 50	GND
J23- 54	GND
J23- 57	GND
J23- 59	GND
J23- 61	GND
J23- 64	GND
J23- 66	GND
J23- 68	GND
J24- 1	GND
J24- 2	GND
J24- 29	GND
J24- 32	GND
J25- 1	GND
J25- 66	GND
J26- 1	GND
J26- 64	GND
J26- 66	GND
J27- 1	GND
J27- 66	GND
J28- 1	GND
J28- 64	GND
J28- 66	GND
J29- 5	GND
J29- 6	GND
J29- 19	GND
J29- 20	GND
J29- 33	GND
J29- 34	GND
J20- 22	GR TEST
J20- 33	HALT H
J21- 34	HALT H
J22- 34	HALT H
J12-131	HLT GRANT H
J21-131	HLT GRANT H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J21- 65	INHIBIT CONSOLE L
J22- 65	INHIBIT CONSOLE L
J12- 16	INHIBIT L
J18- 16	INHIBIT L
J16- 46	INT SSYN L (TP)
J17- 53	INT VECTOR L
J18-123	INT VECTOR L
J16- 37	INTR H
J18- 37	INTR H
J19- 37	INTR H
J09- 87	IOADBUS 00
J10- 87	IOADBUS 00
J11- 87	IOADBUS 00
J09- 88	IOADBUS 01
J10- 88	IOADBUS 01
J11- 88	IOADBUS 01
J09- 91	IOADBUS 02
J10- 91	IOADBUS 02
J11- 91	IOADBUS 02
J09- 92	IOADBUS 03
J10- 92	IOADBUS 03
J11- 92	IOADBUS 03
J09- 93	IOADBUS 04
J10- 93	IOADBUS 04
J11- 93	IOADBUS 04
J09- 94	IOADBUS 05
J10- 94	IOADBUS 05
J11- 94	IOADBUS 05
J09- 95	IOADBUS 06
J10- 95	IOADBUS 06
J11- 95	IOADBUS 06
J09- 96	IOADBUS 07
J10- 96	IOADBUS 07
J11- 96	IOADBUS 07
J09- 97	IOADBUS 08
J10- 97	IOADBUS 08
J11- 97	IOADBUS 08
J09- 98	IOADBUS 09
J10- 98	IOADBUS 09
J11- 98	IOADBUS 09

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J09- 99	IOADBUS 10
J10- 99	IOADBUS 10
J11- 99	IOADBUS 10
J09-100	IOADBUS 11
J10-100	IOADBUS 11
J11-100	IOADBUS 11
J09-101	IOADBUS 12
310-101	IOADBUS 12
J11 101	IOADBUS 12
J09-102	IOADBUS 13
J10-102	IOADBUS 13
J11-102	IOADBUS 13
J09-103	IOADBUS 14
J10-103	IOADBUS 14
J11-103	IOADBUS 14
J09-104	IOADBUS 15
J10-104	IOADBUS 15
J11-104	IOADBUS 15
J16-104	KT DISABLE MSYN L
J18-104	KT DISABLE MSYN L
J12-109	KT FAULT L
J16-109	KT FAULT L
J16- 17	KT MUX SO L (TP)
J12-118	KTE (1) H
J19-118	KTE (1) H
J10-107	LED 0
J11-111	LED 0
J09-107	LED 1
J11-112	LED 1
J16- 34	LOAD BAR H
J18- 34	LOAD BAR H
J17- 6	LOAD CC L
J18- 7	LOAD CC L
J17- 73	LOAD IR L
J18- 3	LOAD IR L
J19- 73	LOAD IR L
J16- 3	LOAD PARH L (TP)
J16- 4	LOAD PARL L (TP)

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J16- 5	LOAD PDRH L (TPI
J16- 6	LOAD PDRL L TP
J16-137	LOAD PIRH L
J19- 26	LOAD PIRH L
J17- 88	LOAD PSW L
J18- 88	LOAD PSW L
J16- 27	LOAD SROH L (TP)
J16- 47	LOAD SR3 L
J19-117	LOAD SR3 L
J16- 38	LOAD VBA H
J18- 38	LOAD VBA H
J01- 33	LSB BYTE CONTROL H
J03- 33	LSB BYTE CONTROL H
J05- 33	LSB BYTE CONTROL H
J07- 98	LSB BYTE CONTROL H
J21- 11	LTC
J22- 63	LTC
J22- 68	LTC TP
J15- 31	MAN CLK ENAB L
J18- 31	MAN CLK ENAB L
J21- 31	MAN CLK ENAB L
J18- 10	MAN CLK L
J21- 10	MAN CLK L
J10- 83	MCS 0 LCK
J11- 83	MCS 0 LCK
J09- 83	MCS 1 LCK
J11- 84	MCS 1 LCK
E 9	MEMLCK 1
J02- 40	MEMLCK 1
E18	MEMLCK 10
J06- 41	MEMLCK 10
E19	MEMLCK 11
J06- 42	MEMLCK 11
E20	MEMLCK 12
J06- 43	MEMLCK 12
E10	MEMLCK 2
J02- 41	MEMLCK 2

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
E11	MEMLCK 3
J02- 42	MEMLCK 3
E12	MEMLCK 4
J02- 43	MEMLCK 4
E13	MEMLCK 5
J04- 40	MEMLCK 5
E14	MEMLCK 6
J04- 41	MEMLCK 6
E15	MEMLCK 7
J04- 42	MEMLCK 7
E16	MEMLCK 8
J04- 43	MEMLCK 8
E17	MEMLCK 9
J06- 40	MEMLCK 9
J05- 56	MEMORY BUSY (1) H
J07-115	MEMORY BUSY (1) H
J03- 56	MEMORY BUSY (2) H
J07- 73	MEMORY BUSY (2) H
J01- 56	MEMORY BUSY (3) H
J07- 74	MEMORY BUSY (3) H
J05- 46	MEMORY ENABLE (1) L
J07-104	MEMORY ENABLE (1) L
J03- 46	MEMORY ENABLE (2) L
J07-135	MEMORY ENABLE (2) L
J01- 46	MEMORY ENABLE (3 L
J07-134	MEMORY ENABLE (3) L
J12- 41	MFM CLK INH L
J21- 41	MFM CLK INH L
J13- 27	MFM HLT RQST L
J21- 27	MFM HLT RQST L
J19- 61	MFM LOAD MPC L
J20- 61	MFM LOAD MPC L
J21-129	MFM SER IN H
J22-129	MFM SER IN H
J21-119	MFM SER OUT H
J22-119	MFM SER OUT H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J16- 40	MODE 00 H
J18- 40	MODE 00 H
J16- 53	MODE 01 H
J18- 53	MODE 01 H
J18- 13	MPC 00 L
J19- 13	MPC 00 L
J17- 14	MPC 01 L
J18- 14	MPC 01 L
J19- 14	MPC 01 L
J18- 93	MPC 02 L
J19- 93	MPC 02 L
J18- 94	MPC 03 L
J19- 94	MPC 03 L
J18- 95	MPC 04 L
J19- 95	MPC 04 L
J18- 96	MPC 05 L
J19- 96	MPC 05 L
J18- 97	MPC 06 L
J19- 97	MPC 06 L
J18- 98	MPC 07 L
J19- 98	MPC 07 L
J18- 26	MPC 08 L
J18- 27	MPC 09 L
J18- 28	MPC 10 L
J01- 43	MSB BYTE CONTROL H
J03- 43	MSB BYTE CONTROL H
J05- 43	MSB BYTE CONTROL H
J07-103	MSB BYTE CONTROL H
J17-8	N BIT (1) H
J19-8	N BIT (1) H
J17-9	P.C. USER H
J19-9	P.C. USER H
J12-135	P1A 0 H
J19-107	P1A 0 H
J12- 67	P1A 1 H
J19-108	P1A 1 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J12- 68	P1A 2 H
J19-109	P1A 2 H
J16-100	PAGE FAULT H
J22- 5	PAN BOOT H
J24- 13	PAN BOOT H
J22- 6	PAN HALT H
J24- 28	PAN HALT H
J16- 54	PAR+PDR L (TP)
J01- 26	PARITY LSB H
J01- 41	PARITY LSB H
J03- 26	PARITY LSB H
J03- 41	PARITY LSB H
J05- 26	PARITY LSB H
J05- 41	PARITY LSB H
J07-102	PARITY LSB H
J01- 63	PARITY MSB H
J01- 92	PARITY MSB H
J03- 63	PARITY MSB H
J03- 92	PARITY MSB H
J05- 63	PARITY MSB H
J05- 92	PARITY MSB H
J07-113	PARITY MSB H
J12- 73	PAX A00 H
J15- 3	PAX A00 H
J16- 73	PAX A00 H
J18- 73	PAX A00 H
J20- 73	PAX A00 H
J12- 74	PAX A01 H
J15- 4	PAX A01 H
J16- 74	PAX A01 H
J18- 74	PAX A01 H
J20- 74	PAX A01 H
J12- 75	PAX A02 H
J15- 5	PAX A02 H
J16- 75	PAX A02 H
J18- 75	PAX A02 H
J20- 75	PAX A02 H
J12- 76	PAX A03 H
J15- 6	PAX A03 H
J16- 76	PAX A03 H
J18- 76	PAX A03 H
J20- 76	PAX A03 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J12- 77	PAX A04 H
J15- 7	PAX A04 H
J16- 77	PAX A04 H
J20- 77	PAX A04 H
J12- 78	PAX A05 H
J15- 8	PAX A05 H
J16- 78	PAX A05 H
J20- 78	PAX A05 H
J12- 79	PAX A06 H
J15- 9	PAX A06 H
J16- 79	PAX A06 H
J20- 79	PAX A06 H
J12- 80	PAX A07 H
J15- 10	PAX A07 H
J16- 80	PAX A07 H
J20- 80	PAX A07 H
J12- 81	PAX A08 H
J15- 11	PAX A08 H
J16- 81	PAX A08 H
J20- 81	PAX A08 H
J12- 82	PAX A09 H
J15- 12	PAX A09 H
J16- 82	PAX A09 H
J20- 82	PAX A09 H
J12- 83	PAX A10 H
J15- 13	PAX A10 H
J16- 83	PAX A10 H
J20- 83	PAX A10 H
J12- 84	PAX A11 H
J15- 14	PAX A11 H
J16- 84	PAX A11 H
J20- 84	PAX A11 H
J12- 85	PAX A12 H
J15- 15	PAX A12 H
J16- 85	PAX A12 H
J20- 85	PAX A12 H
J12- 86	PAX A13 H
J15- 16	PAX A13 H
J16- 86	PAX A13 H
J20- 86	PAX A13 H
J13- 77	PAX A14 H
J15- 77	PAX A14 H
J16- 7	PAX A14 H
J20- 7	PAX A14 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J13- 78	PAX A15 H
J15- 78	PAX A15 H
J16-8	PAX A15 H
J20-8	PAX A15 H
J13- 79	PAX A16 H
J15- 79	PAX A16 H
J16-9	PAX A16 H
J20-9	PAX A16 H
J13- 80	PAX A17 H
J15- 80	PAX A17 H
J16- 10	PAX A17 H
J20- 10	PAX A17 H
J13- 81	PAX A18 H
J15- 81	PAX A18 H
J16- 11	PAX A18 H
J20- 11	PAX A18 H
J13- 82	PAX A19 H
J15- 82	PAX A19 H
J16- 12	PAX A19 H
J20- 12	PAX A19 H
J13- 83	PAX A20 H
J15- 83	PAX A20 H
J16- 13	PAX A20 H
J20- 13	PAX A20 H
J13- 84	PAX A21 H
J15- 84	PAX A21 H
J16- 14	PAX A21 H
J20- 14	PAX A21 H
J12- 87	PAX C0 H
J16- 87	PAX C0 H
J20- 87	PAX C0 H
J12- 88	PAX C1 H
J16- 88	PAX C1 H
J20- 88	PAX C1 H
J13-123	PAX D00 H
J15-123	PAX D00 H
J17-123	PAX D00 H
J19-123	PAX D00 H
J20-123	PAX D00 H
J13-124	PAX D01 H
J15-124	PAX D01 H
J17-124	PAX D01 H
J19-124	PAX D01 H
J20-124	PAX D01 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J13-125	PAX D02 H
J15-125	PAX D02 H
J17-125	PAX D02 H
J19-125	PAX D02 H
J20-125	PAX D02 H
J13-126	PAX D03 H
J15-126	PAX D03 H
J17-126	PAX D03 H
J19-126	PAX D03 H
J20-126	PAX D03 H
J13-127	PAX D04 H
J15-127	PAX D04 H
J17-127	PAX D04 H
J19-127	PAX D04 H
J20-127	PAX D04 H
J13-128	PAX D05 H
J15-128	PAX D05 H
J17-128	PAX D05 H
J19-128	PAX D05 H
J20-128	PAX D05 H
J13-129	PAX D06 H
J15-129	PAX D06 H
J17-129	PAX D06 H
J19-129	PAX D06 H
J20-129	PAX D06 H
J13-130	PAX D07 H
J15-130	PAX D07 H
J17-130	PAX D07 H
J19-130	PAX D07 H
J20-130	PAX D07 H
J13-131	PAX D08 H
J15-131	PAX D08 H
J17-131	PAX D08 H
J19-131	PAX D08 H
J20-131	PAX D08 H
J13-132	PAX D09 H
J15-132	PAX D09 H
J17-132	PAX D09 H
J19-132	PAX D09 H
J20-132	PAX D09 H
J13-133	PAX D10 H
J15-133	PAX D10 H
J17-133	PAX D10 H
J19-133	PAX D10 H
J20-133	PAX D10 H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J13-134	PAX D11 H
J15-134	PAX D11 H
J17-134	PAX D11 H
J19-134	PAX D11 H
J20-134	PAX D11 H
J13-135	PAX D12 H
J15-135	PAX D12 H
J17-135	PAX D12 H
J19-135	PAX D12 H
J20-135	PAX D12 H
J13-136	PAX D13 H
J15-136	PAX D13 H
J17-136	PAX D13 H
J19-136	PAX D13 H
J20-136	PAX D13 H
J13-137	PAX D14 H
J15-137	PAX D14 H
J17-137	PAX D14 H
J19-137	PAX D14 H
J20-137	PAX D14 H
J13-138	PAX D15 H
J15-138	PAX D15 H
J17-138	PAX D15 H
J19-138	PAX D15 H
J20-138	PAX D15 H
J12-119	PAX INTR L
J18- 49	PAX INTR L
J20-119	PAX INTR L
J12-117	PAX SSYN L
J15-117	PAX SSYN L
J16-117	PAX SSYN L
J20-117	PAX SSYN L
J12-128	PE (1) H
J19- 58	PE (1) H
J12-130	PE+BG+PIRQ+HLT+PFAIL H
J319- 27	PE+BG+PIRQ+HLT+PFAIL H
J12-129	PFAIL (1) H
J18-129	PFAIL (1) H
J12- 15	PFAIL BR PEND H
J12-120	PFAIL H
J19-100	PFAIL H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J12-132	PIRQ GRANT L
J18-132	PIRQ GRANT L
J17-101	PLUS ONE H
J18-101	PLUS ONE H
J19- 55	POWER FAILURE H
J22- 24	POWER FAILURE H
J16-135	PREVIOUS MODE (1) L
J18-135	PREVIOUS MODE (1) L
J12- 22	PROC INIT L
J14- 22	PROC INIT L
J17- 22	PROC INIT L
J19- 22	PROC INIT L
J21- 22	PROC INIT L
J22- 22	PROC INIT L
J12- 64	PSW 05 (1) H
J17- 64	PSW 05 (1) H
J12- 65	PSW 06 (1) H
J17- 65	PSW 06 (1) H
J12- 66	PSW 07 (1) H
J17- 66	PSW 07 (1) H
J17- 24	PSW 14 (1) H
J18- 24	PSW 14 (1) H
J19- 24	PSW 14 (1) H
J17- 23	PSW 15 (1) H
J18- 23	PSW 15 (1) H
J19- 23	PSW 15 (1)H
J20- 6	PULLUP A
J21- 6	PULLUP A
J09- 76	R/W
J10- 76	R/W
J11- 76	R/W
J12- 57	RCD INIT L
J16- 57	RCD INIT L
J19- 57	RCD INIT L
J16- 41	READ SR2 L (TP)
J22-115	RECEIVE COMMON
J24- 25	RECEIVE COMMON
J22-116	RECEIVE DATA
J24- 7	RECEIVE DATA

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J01- 23	REF SYNC H
J03- 23	REF SYNC H
J05- 23	REF SYNC H
J16- 39	RELOCATE H
J18- 39	RELOCATE H
J21- 67	REMOTE H
J22- 67	REMOTE H
J22- 7	REMOTE L
J24- 11	REMOTE L
J12- 18	RESET (1) H
J19- 18	RESET (1) H
J17- 91	ROT C BIT (1) H
J19- 21	ROT C BIT (1) H
J12- 54	RST INST H
J10- 44	RTN-0
J25- 13	RTN-0
J10- 45	RTN-1
J25- 5	RTN-1
J10- 46	RTN-2
J25- 7	RTN-2
J10- 47	RTN-3
J25- 9	RTN-3
J10- 62	RTN-4
J26- 15	RTN-4
J10- 63	RTN-5
J26- 5	RTN-5
J10- 64	RTN-6
J26- 7	RTN-6
J10- 65	RTN-7
J26- 17	RTN-7
J10- 34	RTS-0
J25- 11	RTS-0
J10- 37	RTS-1
J25- 16	RTS-1
J10- 38	RTS-2
J25- 2	RTS-2

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J10- 39	RTS-3
J25- 14	RTS-3
J10- 40	RTS-4
J26- 2	RTS-4
J10- 41	RTS-5
J26- 8	RTS-5
J10- 42	RTS-6
J26- 10	RTS-6
J10- 43	RTS-7
J26- 12	RTS-7
J22-113	RTS/DSR-1
J24- 47	RTS/DSR-1
J22-114	RTS/DSR-2
J24- 36	RTS/DSR-2
J20- 94	RUN H
J22- 94	RUN H
J22- 8	RUN L
J24- 22	RUN L
J10-110	RXD-0
J25- 39	RXD-0
J10-111	RXD-1
J25- 47	RXD-1
J10-112	RXD-2
J25- 53	RXD-2
J10-113	RXD-3
J25- 59	RXD-3
J10-114	RXD-4
J25- 28	RXD-4
J10-115	RXD-5
J25- 30	RXD-5
J10-116	RXD-6
J26- 18	RXD-6
J10-117	RXD-7
J26- 24	RXD-7
J10-128	RXDH-0
J25- 38	RXDH-0

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J10-129	RXDH-1
J25- 48	RXDH-1
J10-130	RXDH-2
J25- 54	RXDH-2
J10-131	RXDH-3
J25- 60	RXDH-3
J10-132	RXDH-4
J25- 29	RXDH-4
J10-133	RXDH-5
J25- 31	RXDH-5
J10-134	RXDH-6
J26- 19	RXDH-6
J10-135	RXDH-7
J26- 25	RXDH-7
J22-109	SEND COMMON
J24- 10	SEND COMMON
J22-110	SEND DATA
J24- 9	SEND DATA
J17- 41	SERIAL SHIFT H
J18- 41	SERIAL SHIFT H
J12-136	SET BE L
J18-136	SET BE L
J17- 84	SEX H
J18- 84	SEX H
J17- 85	SHIFT MUX 00 L
J18- 85	SHIFT MUX 00 L
J17-103	SHIFT MUX 01 L
J18- 8	SHIFT MUX 01 L
J09- 77	SMA14 DISC IN 0
J27- 12	SMA14 DISC IN 0
J09- 78	SMA14 DISC IN 1
J27- 23	SMA14 DISC IN 1
J09- 79	SMA14 DISC IN 2
J28- 45	SMA14 DISC IN 2
J09- 80	SMA14 DISC IN 3
J28- 56	SMA14 DISC IN 3

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J17-113	SP WRITE H
J18-113	SP WRITE H
J17- 45	SPA 00 H
J18- 45	SPA 00 H
J19- 45	SPA 00 H
J17- 46	SPA 01 H
J18- 46	SPA 01 H
J19- 46	SPA 01 H
J17- 47	SPA 02 H
J18- 47	SPA 02 H
J19- 47	SPA 02 H
J17- 48	SPA 03 H
J18- 48	SPA 03 H
J16- 97	SR SEL L
J21- 97	SR SEL L
J12- 39	START RESET H
J19- 39	START RESET H
J12-110	START TRAN H
J18-110	START TRAN H
J12- 60	START TRAN L
J15- 60	START TRAN L
J17- 60	START TRAN L
J16- 31	STATUS REG SO L
J19- 31	STATUS REG SO L
J16- 33	STATUS REG S1 L
J19- 34	STATUS REG S1 L
J12- 58	STROBE CACHE H
J14- 58	STROBE CACHE H
J15- 58	STROBE CACHE H
J17- 83	SWAP H
J18- 83	SWAP H
J17-110	T BIT (1) H
J18- 42	T BIT (1) H
J13- 29	TO (1) L
J19- 29	TO (1) L
J12- 40	TAKE BUS H
J19- 40	TAKE BUS H

Backplane Node List
Sorted by Connector Name

Connector Pin Number	Signal Name
J22-111	TERMINAL READY
J24- 37	TERMINAL READY
J18- 32	TRAN TO MFM L
J16- 32	TRAN TO MFM L
J19- 32	TRAN TO MFM L
J21- 32	TRAN TO MFM L
J17- 16	TRI STATE AMUX L
J10-118	TXD-O
J25- 41	TXD-O
J10-119	TXD-1
J25- 46	TXD-1
J10-120	TXD-2
J25- 52	TXD-2
J10-123	TXD-3
J25- 58	TXD-3
J10-124	TXD-4
J25- 26	TXD-4
J10-125	TXD-5
J25- 32	TXD-5
J10-126	TXD-6
J25- 34	TXD-6
J10-127	TXD-7
J26- 23	TXD-7
J12- 7	UBI BG4 H
J20- 15	UBI BG4 H
J12- 9	UBI BG6 H
J20- 16	UBI BG6 H
J12- 62	UBUS C0 (1) H
J16- 62	UBUS C0 (1) H
J12- 63	UBUS C1 (1) H
J16- 63	UBUS C1 (1) H
J17- 63	UBUS C1 (1) H
J12- 56	UPPER 128K L
J15- 56	UPPER 128K L
J16-103	UPPER 128K L
J19-103	UPPER 128K L
J17- 21	UPPER BYTE L
J18- 22	UPPER BYTE L

Backplane Node List

Sorted by Connector Name

Connector Pin Number	Signal Name
J17-5	**V BIT (1) H**
J19-5	**V BIT (1) H**
J16-125	**VBA 00 1) H**
J18-125	**VBA O0 (1) H**
J21- 68	**WAIT (TP)**
J17-7	**Z BIT (1) H**
J19-7	**Z BIT 1) H**

J-93/(J-94 blank)

GLOSSARY

Section I. ABBREVIATIONS AND ACRONYMS

Uncommon or nonstandard abbreviations used repetitively in this manual are defined below. Abbreviations used only once are defined in parentheses at the point of use.

B

BOOT	Bootstrap
BIT	Built In Test

C

CCA	Circuit Card Assembly
CIM	Console Interface Module
CIS	Commercial Instruction Set
CIU	FT Control Interface Unit
CPU	Central Processor Unit
CR	Carriage Return

D

DEC	Digital Equipment Corporation
DIP	Dual In-line Package
DMA	Direct Memory Access

E

ECC	Error Correcting Code
ETM	Elapsed Time Meter
EIS	Extended Instruction Set
EUB	Extended UNIBUS

F

FT	Force Terminal AN/TRC-179(V)l

G

GMB	Grandmother Board

I

I/O	Input/Output
IF or I/F	Interface

L

LED ..... Light Emitting Diode
LVPS ..... Low Voltage Power Supply

M

MFM ..... Multifunction Module
MOS ..... Metal Oxide Semiconductor
MTU ..... Magnetic Tape Unit

N

NPR ..... Non-Processor Requests

P

PAR ..... Parity
PAX ..... Physical Address Extension
PC ..... Program Counter
P/S ..... Power Supply (see LVPS)

R

RAM ..... Random Access Memory
RN ..... Regency Net

S

SMA ..... Serial Multiplexed Asynchronous
SMI ..... Serial Multiplexed Interface
SMS ..... Serial Multiplexed Synchronous
SPST ..... Single Pole Single Throw (switch)

U

UBI ..... UNIBUS Interface module
UBT ..... UNIBUS Terminator
UART ..... Universal Asynchronous Receiver-Transmitter

V

VBA ..... Virtual Bus Address

Section II. DEFINITION OF UNUSUAL TERMS

Acronyms and expressions which are not in common use are explained below.

Access Time. The time interval between the instant at which data is called for (read operation) or requested to be stored (write operation), and the instant at which it is delivered or completely stored, respectively.

Arithmetic and Logic Unit(ALU). A portion of the Central Processor Unit which performs mathematical operations for calculations and logical operations to make decisions.

Bootstrap. A program always resident in the computer which enables it to accept an operational program.

Byte. A sequence of usually eight adjacent binary digits operated upon as a unit.

Cache. A very high-speed memory that resides logically between the processor and main memory, and holds data and/or instructions the processor is most likely to need soon.

Central Processor Unit(CPU). Part of a computer system which contains the arithmetic and logic unit, the control unit and special register groups. It performs arithmetic operations, controls instruction processing, and provides timing signals.

Cycle Time. The time between the instant memory is accessed and the instant at which it may validly be accessed again.

Direct Addressing. A basic addressing procedure designed to reach any point in main storage directly. Also, a method of programming that has the address of data contained in the instruction that is to be used.

Dynamic RAM(DRAM). A RAM that uses a single transistor-capacitor pair, or cell, to store each bit of information. It is called dynamic because the capacitor must be charged periodically (i.e. refreshed) for the information to remain in place.

Indirect Addressing. A form of computer mass-referencing where one memory location stores the correct address of the data sought.

Interleaving. A method of distributing consecutive memory addresses among a number of memory banks so as to increase the rate at which data may be made available to the requester.

Program Counter. A register that holds the address of the memory location containing the instruction word to be executed next in the time sequence, following the current operation.

Random Access Memory(RAM). A storage arrangement in which each byte of information may be retrieved within the same amount of time as any other byte.

Read Only Memory(ROM). A type of memory whose locations can be accessed directly and read, but cannot be written into.

Static RAM. A RAM that uses a flip-flop or latch as a cell to store each bit of information. The cell can adopt one of two states that will remain unchanged, or static,until it is intentionally altered.

TEMPEST. Study and Control of Classified Data Emissions from a device.

UNIBUS. A trade name of Digital Equipment Corporation referring to a 56-line parallel bus which carries data, address, and control in-formation.

Universal Asynchronous Receiver/Transmitter(UART). A device which translates the parallel data that the CPU uses into serial data that is sent out the serial port.

SUBJECT INDEX

SUBJECT INDEX (CONT.)

SUBJECT INDEX (CONT.)

SUBJECT PAGE

D (Cont.)

E

F

SUBJECT INDEX (CONT.)

SUBJECT INDEX (CONT.)

SUBJECT INDEX (CONT.)

SUBJECT INDEX (CONT.)

SUBJECT INDEX (CONT.)

TEAR ALONG PERFORATED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE

BE EXACT. . .PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.

IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME, GRADE OR TITLE, AND TELEPHONE NUMBER

SIGN HERE:

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE.

P.S.—IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

By Order of the Secretary of the Army:

GORDON R. SULLIVAN
General, United States Army
Chief of Staff

Official:

MILTON H. HAMILTON
Administrative Assistant to the Secretary of the Army
07590

By Order of the Secretary of the Navy:

ROBERT AILES
Rear Admiral, United States Navy
Commander, Space and Naval Warfare Systems Command

By Order of the Secretary of the Air Force:

MERRILL A. MCPEAK
General, United States Air Force
Chief of Staff

Official:

RONALD W. YATES
General, United States Air Force
Commander, AFMC

DISTRIBUTION:

To be distributed in accordance with DA Form 12-36-E, block 9714 requirements for TM 11-5895-1308-24.

U.S. GOVERNMENT PRINTING OFFICE: 1995 - 610-115/20030

PIN: 073321-000